Data Sheet

LTM4732

16V_{IN}, 4A Ultralow Noise Silent Switcher 3 µModule Regulator

FEATURES

- Complete solution in <1cm² (single-sided PCB) or 0.5cm² (dual-sided PCB)
- Low-noise Silent Switcher®3 architecture
  - Ultralow EMI emissions
  - Ultralow RMS noise (10Hz to 100kHz): 4µV_{RMS}
- ±1.5% maximum total DC output voltage error over line, load, and temperature
- Input voltage range: 3V to 16V
- Output voltage range: 0.3V to 6V
- 4A maximum continuous output current
- Adjustable and synchronizable: 400kHz to 4MHz
- Current mode control, fast transient response
- Forced continuous mode capability
- Multiphase parallel with current sharing
- Programmable power good
- Available in a tiny *28-Pin 6.25mm × 4mm × 1.92mm* BGA package

APPLICATIONS

- Telecom, networking, and industrial equipment
- RF power supplies: PLLs, VCOs, mixers, LNAs, PAs
- Low-noise instrumentation
- High speed/high precision data converters

GENERAL DESCRIPTION

The *LTM4732* is a complete 4A step-down *Silent Switcher 3* power µModule® (micromodule) regulator in a tiny 6.25mm × 4mm × 1.92mm ball grid array (BGA) package. The package includes the switching controller, the power MOSFETs, an inductor, and the supporting components. Operating over an input voltage range of 3V to 16V, the LTM4732 supports an output range of 0.3V to 6V. A single resistor sets the output voltage, enabling unity-gain operation over the output range and resulting in virtually constant output noise independent of the output voltage. Only the bulk input and output capacitors are required to complete the design.

The LTM4732 employs the Silent Switcher 3 architecture with internal hot loop bypass capacitors to achieve low electromagnetic interference (EMI) and high efficiency. Additionally, the LTM4732 has an ultralow noise architecture to obtain exceptional low-frequency (<100kHz) output noise. The low electromagnetic interference (EMI) and the low-noise features make the LTM4732 ideal for noise-sensitive applications with a high-efficiency synchronous switching regulator. The LTM4732 is available with a RoHS-compliant terminal finish.

TYPICAL APPLICATION

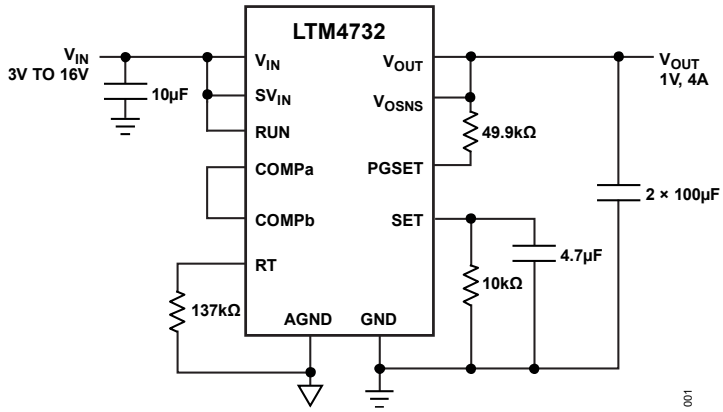

Figure 1. 3V to 16V Input to 1V, 4A Output

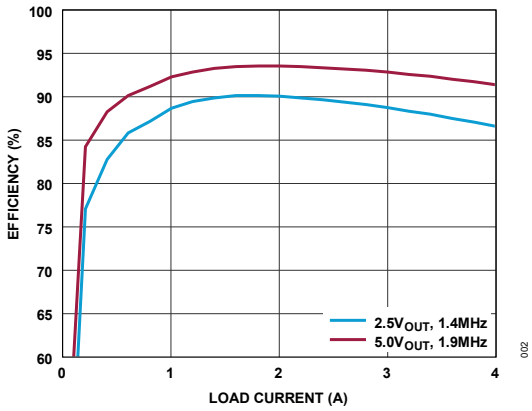

Figure 2. Efficiency, V_{IN} = 12V

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	04/25	Initial release.	—
A	08/25	Updated Figure 34.	26

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C, V_{IN} = 12V, per the typical application[4].)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Power input DC voltage	V_{IN}		–40°C ≤ T_J ≤ 125°C	3		16	V
Signal input DC voltage[7]	SV_{IN}		–40°C ≤ T_J ≤ 125°C	3		16	V
Output voltage range	$V_{OUT(RANGE)}$	V_{PGSET} = 0.5V	–40°C ≤ T_J ≤ 125°C	0.3		6	V
Output voltage, total variation with line and load	$V_{OUT(DC)}$	C_{IN} = 10µF, C_{OUT} = 200µF ceramic, R_{SET} = 10kΩ, Forced continuous mode (FCM), V_{IN} = 3V to 16V, SV_{IN} = 12V, I_{OUT} = 100mA to 4A	–40°C ≤ T_J ≤ 125°C	0.985	1	1.015	V
SET pin current	I_{SET}	V_{SET} = 1V		99.5	100	100.5	µA
Fast startup set pin current	I_{SET_START}	V_{SET} = 1V, V_{PGSET} = 0V		2	2.5	3	mA
Startup time[2,8]	t_{START}	V_{OUT} = 1V, C_{SET} = 1µF, V_{PGSET} = 0.5V			25		ms
		V_{OUT} = 1V, C_{SET} = 4.7µF, V_{PGSET} = 0.5V			120		ms
		V_{OUT} = 1V, C_{SET} = 1µF, R_{PGSET} = 49.9kΩ			1		ms
		V_{OUT} = 1V, C_{SET} = 4.7µF, R_{PGSET} = 49.9kΩ			2.5		ms
RUN pin ON threshold	V_{RUN}	V_{RUN} rising			1.32	1.37	V
RUN pin hysteresis	V_{RUN}				50		mV
Internal V_{CC} voltage	V_{INTVCC}			3.2	3.4	3.6	V
SV_{IN} quiescent current	I_{Q_SVIN}	SV_{IN} = 12V, V_{RUN} = 0V, shutdown			50		µA
		SV_{IN} = 12V, R_T = 47kΩ, FCM			10	17	mA
Output noise spectral density (2kHz)[2,3,5,6]	$V_{OUT\_SPOTNOISE}$	SV_{IN} = 12V, V_{OUT} = 1V, C_{OUT} = 200µF, R_{SET} = 10kΩ, C_{SET} = 4.7µF, f_{SW} = 2MHz			4		nV/√Hz

(T_A = 25°C, V_{IN} = 12V, per the typical application[4].)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Output RMS noise (10Hz to 100kHz)[2,3,5,6]	$V_{OUT\_RMSNOISE}$	SV_{IN} = 12V, V_{OUT} = 1V, BW = 10Hz to 100kHz, I_{OUT} = 0.5A, C_{OUT} = 200µF, R_{SET} = 10kΩ, C_{SET} = 4.7µF, f_{SW} = 2MHz			4		$µV_{RMS}$
Output continuous current	$I_{OUT(DC)}$	V_{OUT} = 1V				4	A
Output voltage line regulation	$ΔV_{OUT}$ (LINE)/V_{OUT}	V_{OUT} = 1V, V_{IN} = 3V to 16V, SV_{IN} = 12V, I_{OUT} = 100mA	–40°C ≤ T_J ≤ 125°C		0.025	±0.15	%/V
Output voltage load regulation	$ΔV_{OUT}$ (LOAD)/V_{OUT}	V_{OUT} = 1V, V_{IN} = 12V, SV_{IN} = 12V, I_{OUT} = 100mA to 4A	–40°C ≤ T_J ≤ 125°C			±1	%
V_{OSNS} output current	I_{VOSNS}			80	160	240	nA
Output ripple voltage[2]	$V_{OUT(AC)}$	I_{OUT} = 100mA, C_{OUT} = 200µF, V_{OUT} = 1V, R_T = 137kΩ			8		mV
Output current limit	I_{OUT_PK}				7		A
Minimum on-time	t_{ON_MIN}				15		ns
PGSET upper threshold	V_{PGSET}	PGSET rising		525	540	550	mV
PGSET upper threshold hysteresis	V_{PGSET}	PGSET rising			5		mV
PGSET lower threshold	V_{PGSET}	PGSET falling		455	465	475	mV
PGSET lower threshold hysteresis	V_{PGSET}	PGSET falling			5		mV
PGSET pin current	I_{PGSET}	V_{PGSET} = 0.5V			10		µA
PG leakage	I_{PG}	V_{PG} = 3.3V, SV_{IN} = 0V		–40		40	nA
PG pull-down resistance	R_{PG}	V_{PG} = 0.5V			380	650	Ω
Oscillator frequency	f_{OSC}	R_T = 392kΩ			300		kHz
		R_T = 47kΩ			2		MHz
		R_T = 18kΩ			4		MHz
SYNC threshold	SYNC_LEVEL	SYNC DC and clock low level voltage		0.7			V
		SYNC DC and clock high level voltage				1.5	V
PHMODE thresholds	V_{PHMODE}	180° phase shift				0.7	V
		90° phase shift		2.7			V

1 The LTM4732 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4732E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and the correlation with statistical process controls. The LTM4732I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 Not subject to production test.

3 V_{OSNS} connects directly to V_{OUT}.

4 The EC table's test circuits and test conditions could be different than the typical applications.

5 Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise and the reference current's noise. Using a SET pin bypass capacitor also increases startup time.

6 See the output current derating curves for different V_{IN}, V_{OUT}, and T_A conditions in the *Typical Performance Characteristics* section.

7 The SV_{IN} supplies current to the internal circuitry and regulator. The SV_{IN} should be above 4V to achieve a regulation of ±1.5% maximum total DC output voltage error over line, load, and temperature. Additionally, to provide sufficient headroom for the SET pin current reference, the SV_{IN} must be 0.4V higher than the desired V_{OUT}.

8 The startup time is defined as the time it takes for the RUN pin to rise above the RUN threshold when V_{OUT} has reached 90% of its final values.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings[1]

PARAMETER	RATING
V_{IN}, SV_{IN}, RUN, PG	18V
SYNC, V_{OUT}, V_{OSNS}, SET, PGSET	6V
PHMODE, COMPa, RT	4V
Internal operating junction temperature range e-grade, I-grade	–40°C to 125°C
Storage temperature range	–55°C to 125°C
Peak solder reflow body temperature	250°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to Printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings

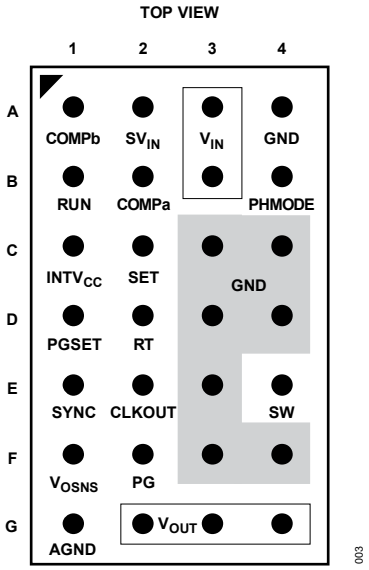
Table 3. LTM4732 ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	3A
CDM	±1250	C3

ESD Caution

Electrostatic discharge (ESD) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



BGA PACKAGE
28-PIN (6.25mm × 4.00mm × 1.92mm)
T_{JMAX} = 125°C, θ_{JA} = 27.5°C/W, θ_{JCtop} = 26.6°C/W,
θ_{JCbot} = 9.4°C/W, WEIGHT = 0.13g

θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
θ_{JA} VALUE IS OBTAINED WITH THE EVALUATION BOARD.
SEE THE TYPICAL PERFORMANCE CHARACTERISTICS SECTION FOR LAB MEASUREMENT AND DERATING CURVES.

Figure 3. Pin Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Descriptions

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
CFG 1		
A1	COMPb	Internal Compensation Network. Connect it to the COMPa pin to use the internal compensation for most applications.
A2	SV_{IN}	Signal V_{IN}. This pin supplies current to the LTM4732's internal circuitry and regulator. If connected to a different supply other than the V_{IN}, place a 1µF local bypass capacitor on this pin.
A3, B3	V_{IN}	Power Input Pins. Apply input voltage between these pins and the GND pins. It is recommended to place the input decoupling capacitor directly between the V_{IN} pins and the GND pins.

PIN CFG 1	NAME	DESCRIPTION
A4, C3, C4, D3, D4, E3, F3, F4	GND	Power ground pins for input and output returns.
B1	RUN	Run Control Input. Enables device operation by connecting RUN above 1.32V (typical). Connecting RUN below 0.4V shuts down the device.
B2	COMPa	Output of the Internal Error Amplifier. The voltage on this pin controls the peak switch current. Connect all the COMPa pins from different channels together for a parallel operation. Connect to COMPb to use the internal compensation. Otherwise, connect to an external RC network to use customized compensation.
B4	PHMODE	The PHMODE pin sets the phase shift of the clock signal of the CLKOUT pin. Connect the PHMODE pin to the ground for a 180° phase shift, float the pin for a 120° phase shift, and connect it high to $INTV_{CC}$ (~3.4V), or to an external supply of >3V for a 90° phase shift.
C1	$INTV_{CC}$	Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered by this voltage. Do not load the $INTV_{CC}$ pin with an external circuitry. This pin should be left floated.
C2	SET	Output Voltage Set. This pin is the noninverting input of the error amplifier and the regulation setpoint for the LTM4732. The SET pin sources a precision 100µA current that flows through an external resistor connected between the SET and GND pins. The LTM4732's output voltage is determined by $V_{SET} = I_{SET} \times R_{SET}$. The output voltage ranges from 0.3V to 6V. Adding a capacitor from the SET pin to the GND pin improves noise at the expense of increased startup time. For optimum load regulation, Kelvin connects the ground side of the SET pin resistor directly to the load.
D1	PGSET	Power Good Set. The PG pin pulls low if PGSET increases above 540mV or decreases below 465mV. Connecting a pull-up resistor between V_{OUT} and PGSET sets the programmable power good threshold using Equation *1*. $R_{PGSET} = (2 \times V_{OUT} - 1) \times 49.9k\Omega$ (1) PGSET activates the fast startup circuitry. See the *Applications Information* section for more details. If the power is good and fast startup functionalities are not needed, the PGSET pin must be connected to an external 0.5V. Do not float the PGSET pin.
D2	RT	This pin sets the oscillator frequency with an external resistor to the AGND.
E1	SYNC	This pin programs three different operating modes: 1) Pulse-skipping mode (PSM). Connect this pin to GND for PSM for improved efficiency at light loads. 2) Forced continuous mode (FCM). The FCM offers fast transient response and full-frequency operation over a wide load range. Connect this pin high to $INTV_{CC}$ (~3.4V) or to an external supply >3V for FCM. The device operates in FCM by default if this pin is left floating. 3) Synchronization mode. Drive this pin with a clock source synchronized to an external clock and put the device in FCM.

PIN CFG 1	NAME	DESCRIPTION
E2	CLKOUT	Output Clock Signal for PolyPhase® Operation. The CLKOUT pin provides a 50% duty-cycle square wave of the switching frequency. The phase of CLKOUT for the LTM4732's internal clock is determined by the state of the PHMODE pin. The CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. Float this pin if the CLKOUT function is not used.
E4	SW	Switching node of the LTM4732. This pin is for test purposes only. Do not load the SW pin with an external circuitry.
F1	V_{OSNS}	Output Voltage Sense. This pin is the inverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connects V_{OSNS} directly to the output capacitor and the load. Also, connect all the GND connections of the output capacitor and the SET pin capacitor directly together.
F2	PG	Output Power Good Indicator. The PG pin is the open-drain output of an internal comparator. The PG pin remains low until the V_{OSNS} pin is within ±7.5% of the final regulation voltage, and until no fault conditions are present. The PG pin is also pulled low when the RUN pin is below 1V, when the $INTV_{CC}$ has fallen too low, when SV_{IN} is too low, or during the thermal shutdown. The PG pin is valid when the SV_{IN} is above 3V.
G1	AGND	Analog Ground. Ground return for SYNC, RT, and COMP pins. The AGND pin is internally connected to the GND pins within the LTM4732 module.
G2, G3, G4	V_{OUT}	Power Output Pins. Apply the output load between these pins and the GND pins. Placing the output decoupling capacitor directly between the V_{OUT} pins and the GND pins is recommended.

Pin Configuration Description

Table 5. LTM4732 Component BGA Pinout (Sorted by Pin Number)

PIN ID	PIN NAME	PIN ID	PIN NAME	PIN ID	PIN NAME	PIN ID	PIN NAME
A1–D4							
A1	COMPb	B1	RUN	C1	$INTV_{CC}$	D1	PGSET
A2	SV_{IN}	B2	COMPa	C2	SET	D2	RT
A3	V_{IN}	B3	V_{IN}	C3	GND	D3	GND
A4	GND	B4	PHMODE	C4	GND	D4	GND
E1–G4							
E1	SYNC	F1	V_{OSNS}	G1	AGND		
E2	CLKOUT	F2	PG	G2	V_{OUT}		
E3	GND	F3	GND	G3	V_{OUT}		
E4	SW	F4	GND	G4	V_{OUT}		

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

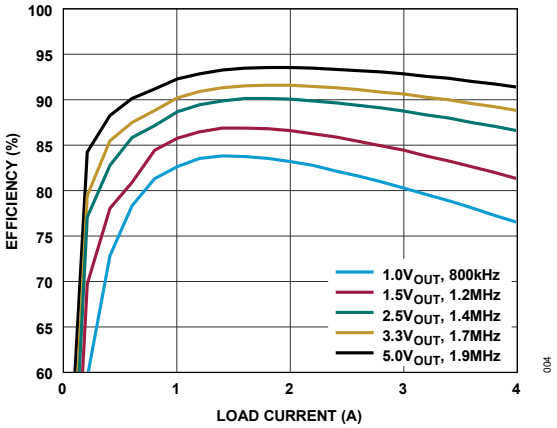


Figure 4. Efficiency vs. Load, V_{IN} = 12V

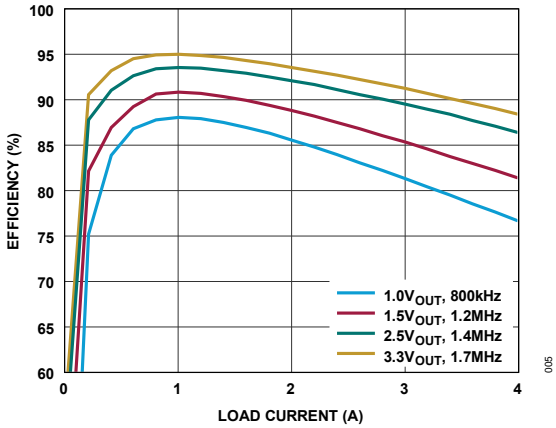


Figure 5. Efficiency vs. Load, V_{IN} = 5V

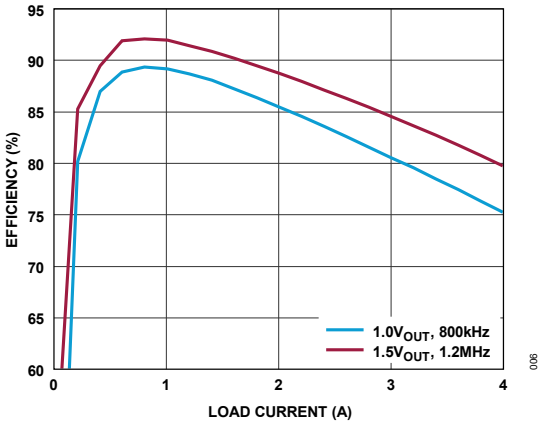


Figure 6. Efficiency vs. Load, V_{IN} = 3.3V

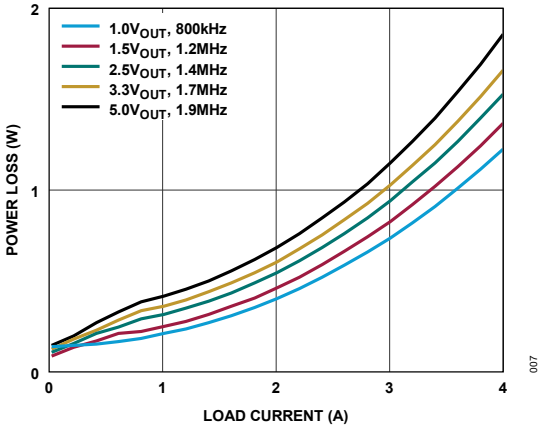


Figure 7. Power Loss vs. Load, V_{IN} = 12V

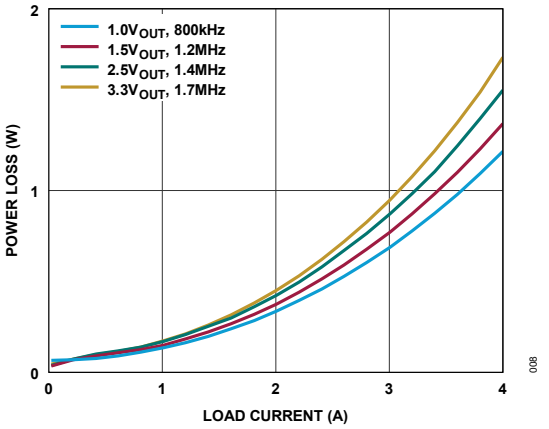


Figure 8. Power Loss vs. Load, V_{IN} = 5V

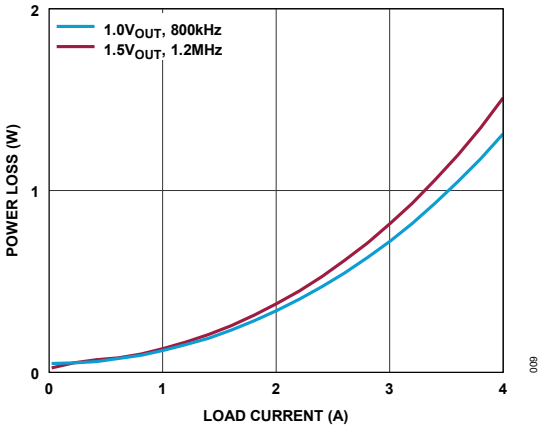


Figure 9. Power Loss vs. Load, V_{IN} = 3.3V

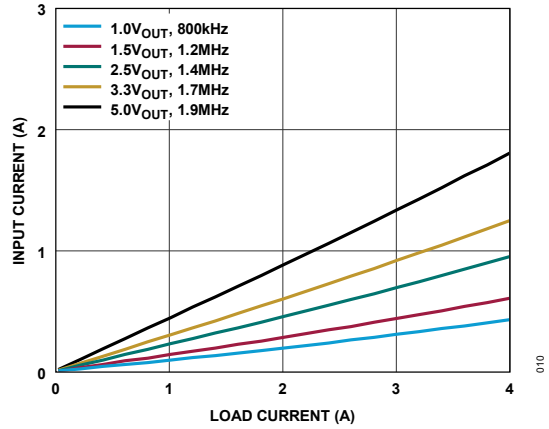


Figure 10. Input vs. Load Current, V_{IN} = 12V

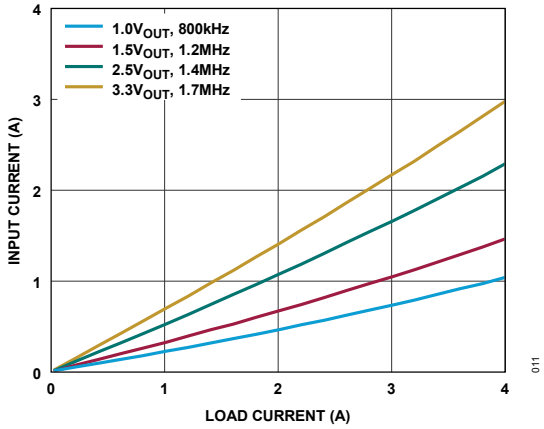


Figure 11. Input vs. Load Current, V_{IN} = 5V

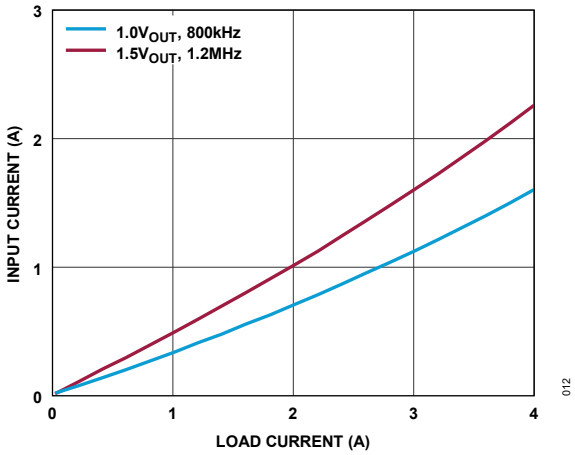


Figure 12. Input vs. Load Current, V_{IN} = 3.3V

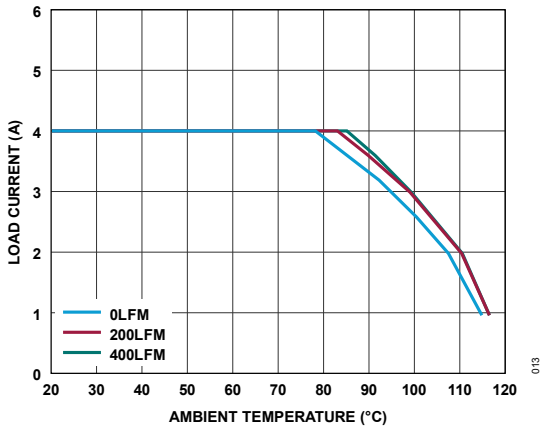


Figure 13. Derating Curve V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 800kHz

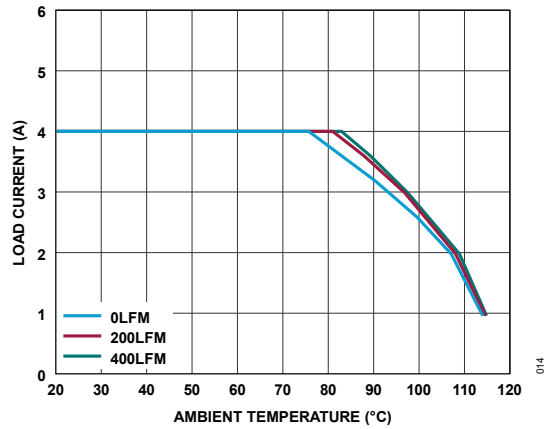


Figure 14. Derating Curve, V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 1.2MHz

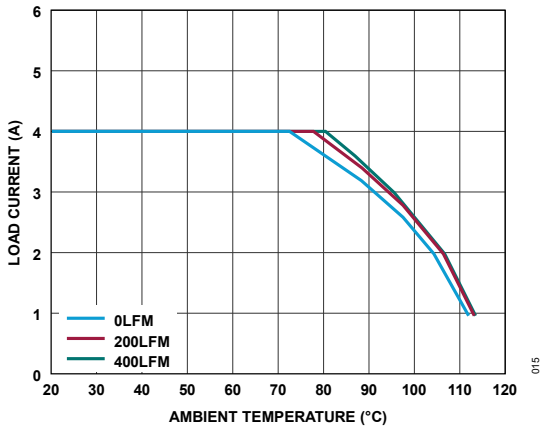


Figure 15. Derating Curve, V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 1.4MHz

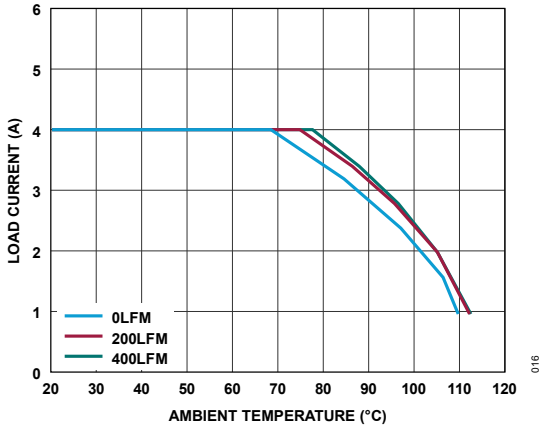


Figure 16. Derating Curve, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1.7MHz

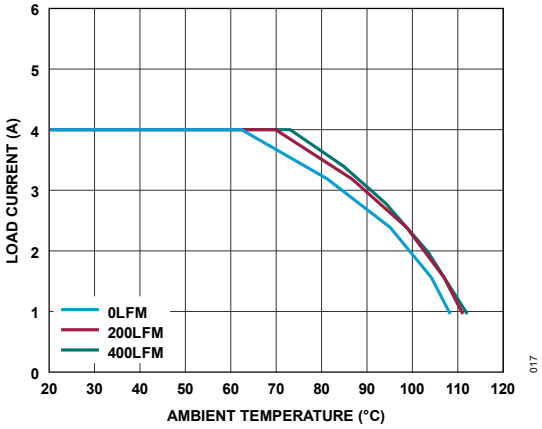


Figure 17. Derating Curve, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2MHz

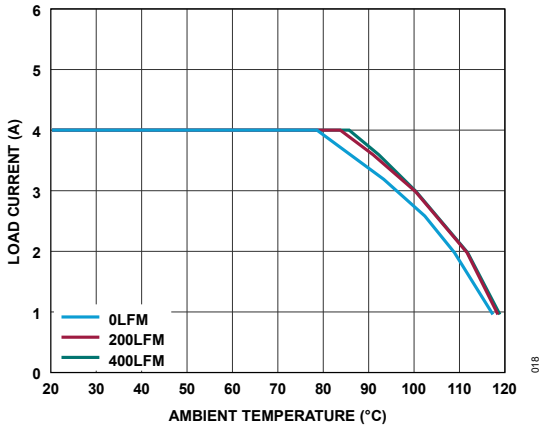


Figure 18. Derating Curve, V_{IN} = 5V, V_{OUT} = 1V, f_{SW} = 800kHz

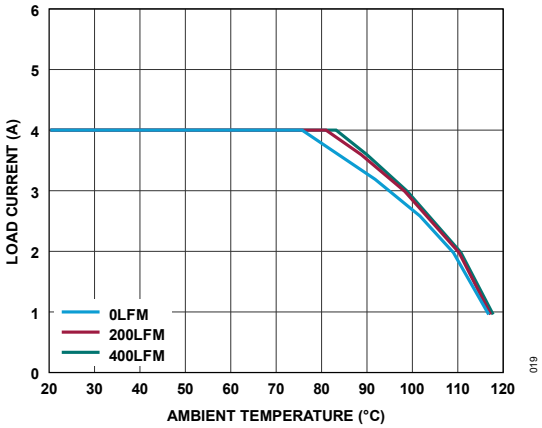


Figure 19. Derating Curve, V_{IN} = 5V, V_{OUT} = 1.5V, f_{SW} = 1.2MHz

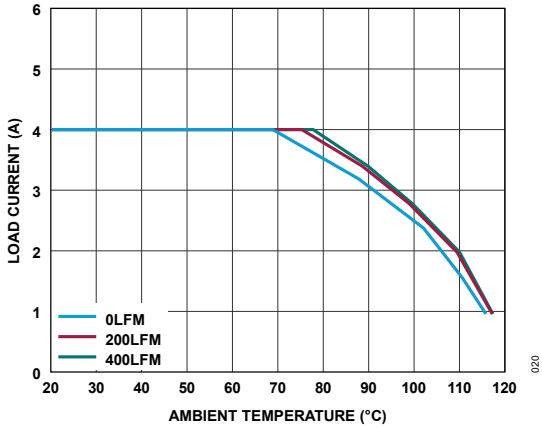


Figure 20. Derating Curve, V_{IN} = 5V, V_{OUT} = 2.5V, f_{SW} = 1.4MHz

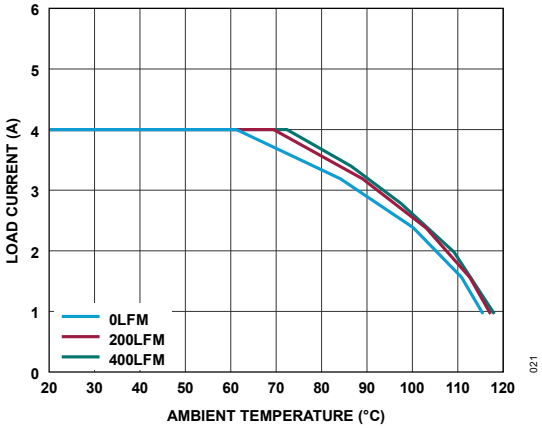


Figure 21. Derating Curve, V_{IN} = 5V, V_{OUT} = 3.3V, f_{SW} = 1.7MHz

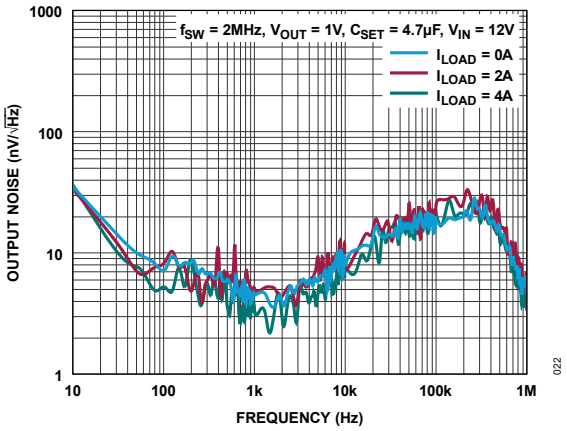


Figure 22. Noise Spectral Density vs. Load

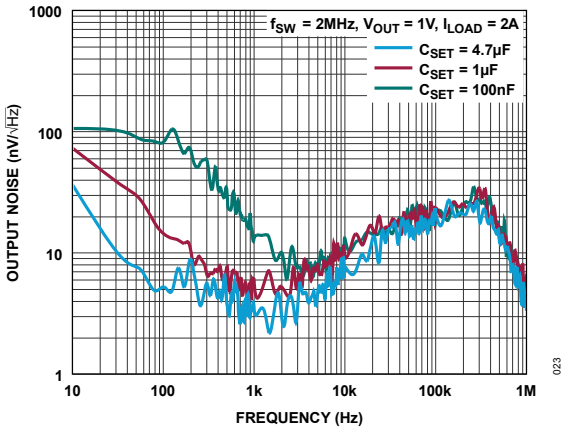


Figure 23. Noise Spectral Density vs. C_{SET}

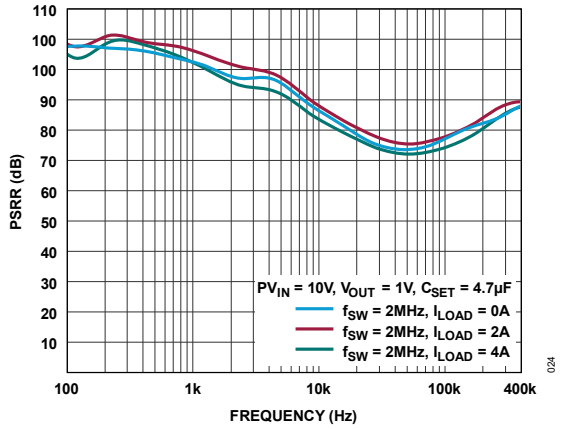
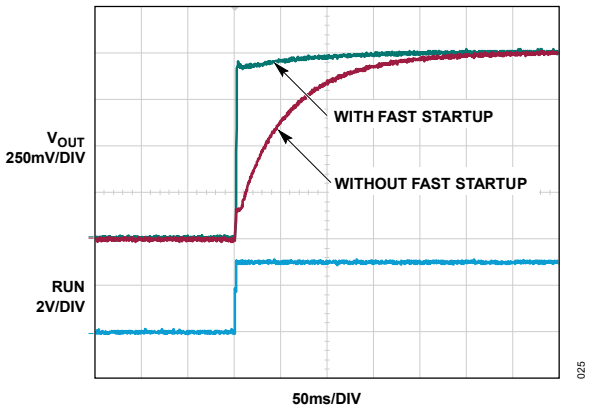
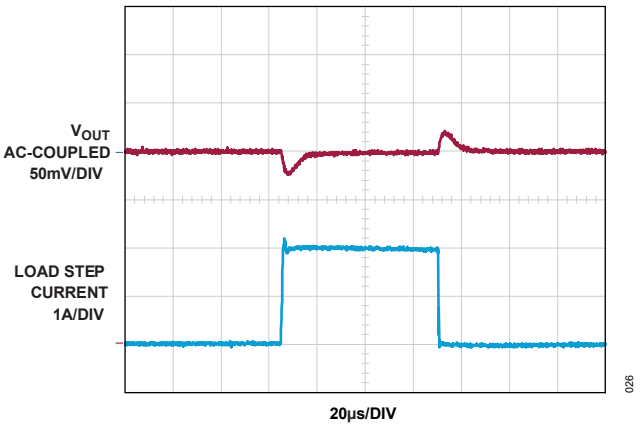


Figure 24. Power Supply Ripple Rejection



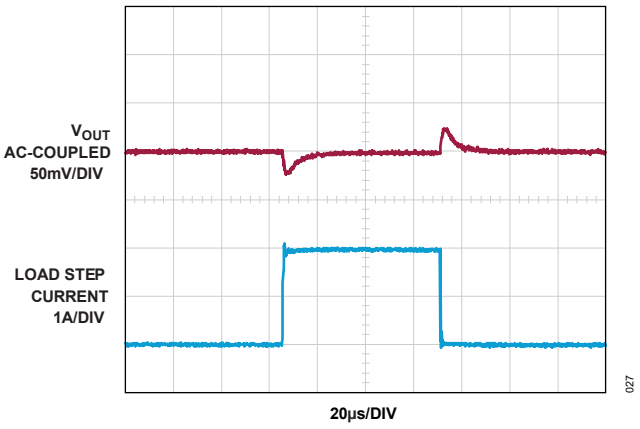
SV_{IN} = 5V, R_{SET} = 10kΩ, C_{SET} = 4.7µF
f_{SW} = 2MHz, R_L = 1Ω

Figure 25. Startup Time with/without Fast Startup Circuitry (Large C_{SET})



V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 2A TO 4A
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR
INTERNAL COMPENSATION
CONNECT COMPa TO COMPb

Figure 26. 1V Output Transient Response



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A TO 4A
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR
INTERNAL COMPENSATION
CONNECT COMPa TO COMPb

Figure 27. 5V Output Transient Response

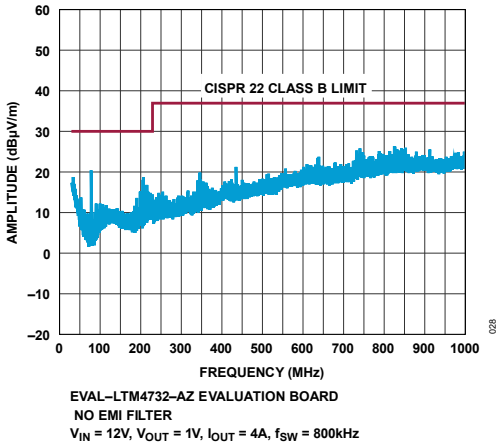


Figure 28. CISPR 22 Class B Emissions

THEORY OF OPERATION

LTM4732 Overview

The LTM4732 is a standalone, non-isolated switching DC-to-DC power supply that can deliver up to 4A. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable through an external resistor from 0.3V to 6V. The input voltage range is 3V to 16V. Since the LTM4732 is a step-down regulator, ensure that the input voltage is high enough to support the desired output voltage and load current. See the Simplified Block Diagram in *Figure 29*.

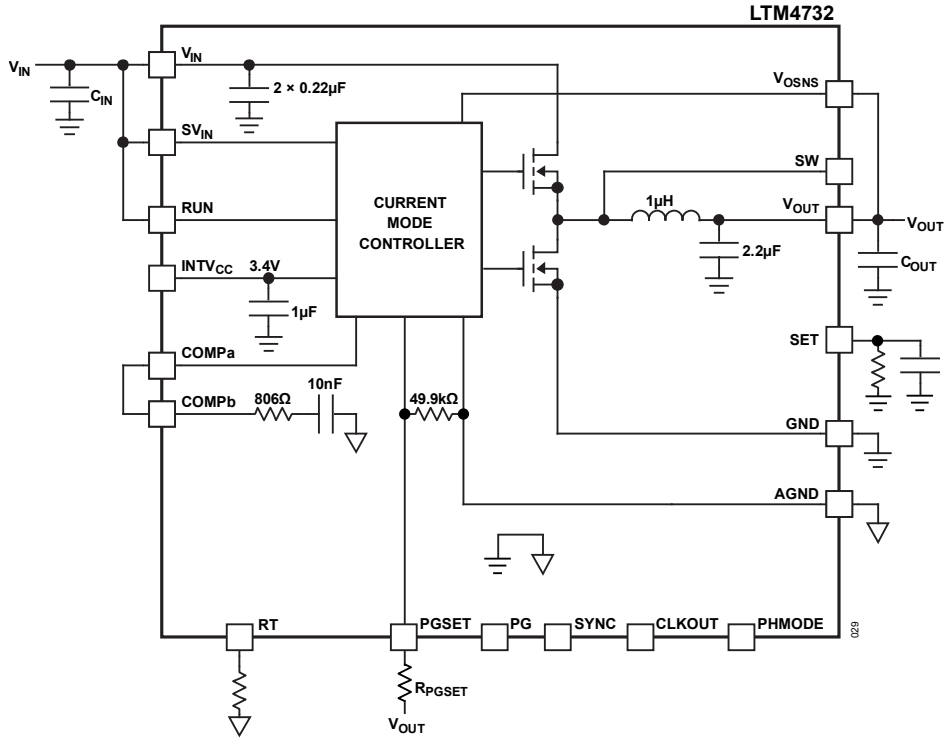


Figure 29. LTM4732 Simplified Block Diagram

The LTM4732 contains a current mode controller, power switching elements, a power inductor, and a modest amount of input and output capacitance. The LTM4732 is a fixed-frequency pulse-width modulation (PWM) regulator. The switching frequency is set by simply connecting a resistor from the RT pin to AGND.

An internal regulator provides power to the control circuitry. To improve efficiency across all loads, the SV_{IN} pin can be powered by an independent supply at a voltage lower than V_{IN}. If the RUN pin is below 0.4V, the LTM4732 is shut down and draws 50µA from the input. When the RUN pin rises above 1.32V (typical), LTM4732 becomes active.

In applications where low output ripple and high efficiency at light load conditions are desired, the pulse-skipping mode (PSM) should be used by connecting the SYNC pin to GND. At light loads, the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

In applications where a fixed-frequency operation is more critical than low current efficiency and where the lowest output ripple is desired, the forced continuous mode (FCM) operation should be used. The FCM operation is enabled by connecting the SYNC pin to the $INTV_{CC}$ pin. In this mode, the inductor current can reverse during low output loads, the COMP voltage controls the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During startup, the FCM is disabled, and the inductor current is prevented from reversing until the LTM4732's output voltage is regulated.

The LTM4732 incorporates fast startup circuitry that allows the device to startup in a shorter time while using a larger value SET pin capacitor for ultralow noise applications. See the *Applications Information* section for more details.

The LTM4732 contains a power good comparator, which trips when the PGSET pin is between 465mV and 540mV. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG signal is valid when SV_{IN} is above 3V. If SV_{IN} is above 3V and the RUN pin is low, PG remains low.

The LTM4732 has a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above 125°C to avoid interfering with normal operation, prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

Two or more LTM4732 modules may be operated in parallel to produce higher currents. The COMPa and CLKOUT pins enable multiple LTM4732 to run out-of-phase, reducing the required amount of input and output capacitors. The PHMODE pin selects the phasing of CLKOUT for different multiphase applications. The COMPa pin allows the loop compensation of the LTM4732 to be optimized for a fast transient response.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward, and it is summarized as follows.

1. See *Table 6* for the row with the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{SET}, and R_T values.
3. Apply the C_{SET} (from SET to GND).

While the component values in *Table 6* have been tested for proper operation, the user must verify proper operation over the intended system's line, load, and environmental conditions. Remember that the maximum output current is limited by the junction temperature, the relationship between the input and output voltage magnitude, and the polarity, among other factors. See the graphs in the *Typical Performance Characteristics* section for more details.

The maximum frequency (and attendant R_T value) at which the LTM4732 should be allowed to switch is shown in *Table 6* in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over a given input condition is in the f_{SW} column. Additional conditions must be satisfied if the synchronization function is used. See the *Synchronization* section for more details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in *Table 6* are the minimum recommended values for the associated operating conditions. Applying capacitor values below the values, shown in *Table 6* is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and they can yield improved dynamic response if necessary. Again, the user must verify the proper operation over the intended system's line, load, and environmental conditions.

The ceramic capacitors are small, robust, and have very low effective series resistance (ESR). However, not all ceramic capacitors are suitable. The X5R and X7R types are stable over temperature and applied voltage, and they provide dependable service. Other types, including Y5V and Z5U, have very large temperature and voltage coefficients of capacitance. In an application circuit, they may have only a small fraction of their nominal capacitance, resulting in a much higher output voltage ripple than expected. The ceramic capacitors are also piezoelectric. Since the LTM4732 operates at a lower current limit during the PSM operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high-performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low-cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4732. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM4732 circuit is plugged into a live supply, the input voltage can ring twice its nominal value, possibly exceeding the device's rating. This situation can be easily avoided (see the *Hot-Plugging Safely* section for more details).

Table 6. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}[1] (V)	V_{OUT} (V)	R_{SET} (kΩ)	C_{IN}[2]	C_{OUT}	f_{SW} (kHz)	R_T (kΩ)	MAX f_{SW} (kHz)	MIN R_T (kΩ)
3 to 16	1	10	10µF X7R 25V 1210	2 × 100µF X7R 6.3V 1210	800	137	2500	35.7
3.3 to 16	1.5	15	10µF X7R 25V 1210	2 × 100µF X7R 6.3V 1210	1200	86.6	2500	35.7
3.9 to 16	2.5	24.9	10µF X7R 25V 1210	2 × 100µF X7R 6.3V 1210	1400	71.5	3000	28.7
4.5 to 16	3.3	33.2	10µF X7R 25V 1210	2 × 100µF X7R 6.3V 1210	1700	57.1	3500	23.2
7.5 to 16	5	49.9	10µF X7R 25V 1210	2 × 100µF X7R 10V 1210	1900	49.9	4000	18

[1] The LTM4732 may be capable of operating at a lower input voltage, but it may skip switching cycles.

[2] A bulk capacitor is required.

Frequency Selection

The LTM4732 uses a constant-frequency pulse-width modulation (PWM) architecture that can be programmed to switch from 300kHz to 4MHz using a resistor connected from the RT pin to the ground. See *Table 7* for a list of R_T resistor values and their resultant frequencies.

Table 7. Switching Frequency vs. R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	392
0.4	287
0.5	226
0.6	187
0.7	154
0.8	137
0.9	118
1.0	105
1.2	86.6
1.4	71.5
1.6	61.9
1.8	53.6
2	47
2.5	35.7
3	28.7
3.5	23.2
4	18

Operating Frequency Trade-Offs

It is recommended to apply the optimal R_T values, as shown in *Table 7*, for the input and output operating conditions. However, it may necessitate another operating frequency for system-level or other considerations. While the LTM4732 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat, or even damage the LTM4732 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple, or too large of an output capacitor.

Maximum Load

The maximum practical continuous load that the LTM4732 can drive, while rated at 4A, depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM4732 in the case of an overload or a short-circuit. The internal temperature of the LTM4732 depends upon operating conditions such as the ambient temperature, the power delivered, and the system's heat-sinking capability. For example, if the LTM4732 is configured to regulate at 1V, it may continuously deliver 4A from $12V_{IN}$ if the ambient temperature is controlled to less than 73°C with no airflow. See *Figure 13* for the $12V_{IN}$ and $1V_{OUT}$ derating curves in the *Typical Performance Characteristics* section. Similarly, if the output voltage is 5V and the ambient temperature is 85°C, the LTM4732 delivers at most 2.97A from $12V_{IN}$, which is less than the 4A continuous rating.

Load Sharing

Two or more LTM4732 modules may be paralleled to produce higher currents. To do this, connect the V_{IN}, V_{OUT}, V_{OSNS}, COMPa, and COMPb pins of all the paralleled LTM4732 modules together. Examples of multiple LTM4732 modules configured for load sharing are shown in the *Typical Applications* section (See *Figure 39* and *Figure 40*).

The CLKOUT signal can connect to the SYNC pin of the following LTM4732 to line up the frequency and the phase of the entire system. Connecting the PHMODE pin to GND, $INTV_{CC}$, or floating the pin generates a phase difference between the LTM4732's internal clock and CLKOUT of a 180°, 90°, or 120°, respectively, which corresponds to a 2-phase, 4-phase, or 3-phase operation. A total of 12 phases can be paralleled to run simultaneously out-of-phase to each other by programming the PHMODE pin of each LTM4732 to different voltage levels. *Figure 30* shows a 4-phase application where four LTM4732 modules are paralleled to get one output capable of up to 16A. During FCM and synchronization mode, all devices operate at the same frequency. When load sharing among a number (n) of units and using a single R_{SET} resistor, the value of the resistor is given by Equation *2*.

$$R_{SET} = \frac{V_{OUT}}{\mathrm{n} \times 100\mu\mathrm{A}} \qquad (2)$$

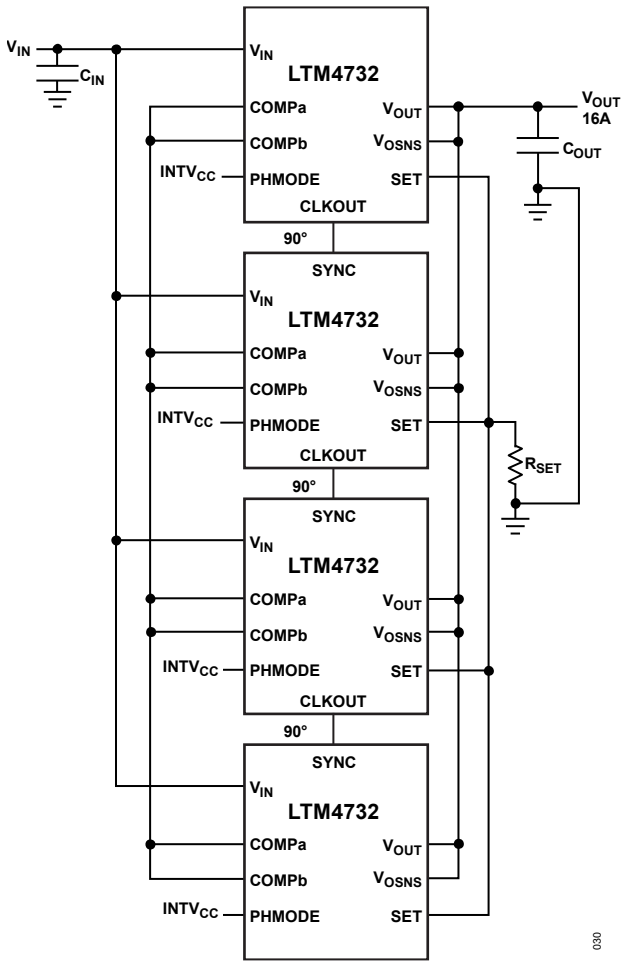


Figure 30. Paralleling Four LTM4732 Modules

Minimum Input Voltage

The LTM4732 is a step-down regulator, so a minimum amount of headroom is required to regulate the output. Keep V_{IN} above 3V to ensure proper operation. If the SV_{IN} and V_{IN} are powered by different sources, keep the SV_{IN} above 4V to maintain $INTV_{CC}$ = 3.4V and ensure optimum regulation. The voltage transients or the ripple valleys that cause the SV_{IN} to fall below 3V may turn-off the LTM4732.

SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft Start

In addition to reducing output noise, using the SET pin bypass capacitor reduces sensitivity to any parasitic coupling of voltage spikes onto the SET pin. Note that any bypass capacitor leakage deteriorates the LTM4732 DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, it is recommended to use a good quality, low-leakage ceramic capacitor.

A SET pin bypass capacitor also soft-starts the output and limits inrush current. Soft-starting the output prevents a current surge in the input supply. The SET pin capacitor and resistor values set the ramp-up time of the reference voltage, and the output voltage tracks this voltage. The SET pin resistance is determined by the application's desired output voltage; however, the capacitance may be selected to achieve the desired ramp-up time.

Without fast startup enabled, the RC time constant, formed by the SET pin resistor and the capacitor, controls the soft start time. Connect the PGSET pin to 0.5V to disable fast startup. The ramp-up rate from 0% to 90% of nominal V_{OUT} is shown in Equation 5.

$$t_{START\_NO\_FAST\_STARTUP} = 2.3 \times R_{SET} \times C_{SET} \quad (3)$$

With fast startup enabled, the startup time can be significantly reduced with the ramp-up time from 0% to 90% of the nominal V_{OUT} given by Equation 4.

$$t_{START\_FAST\_STARTUP} = \frac{100\mu A \times R_{SET} \times C_{SET}}{2.5mA} \quad (4)$$

In most applications, the fast startup is enabled, in which case a minimum 1µF SET capacitor is recommended to prevent reference voltage overcharge and ensure good noise performance.

Soft Start and Power Sequencing

As discussed in the *SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft Start* section, a soft start is achieved through the controlled ramp-up time of the SET pin voltage. A soft start is guaranteed when V_{IN} and SV_{IN} are connected.

When V_{IN} and SV_{IN} are powered by independent supplies, power sequencing must be considered to guarantee a soft start. The SET pin voltage should start at 0V when V_{IN} is applied. To ensure a soft start, do not power V_{IN} last when sequencing V_{IN}, SV_{IN}, and RUN. An example of a specific case to avoid is having SV_{IN} and RUN powered up before V_{IN}; in this instance, the SET pin voltage rises to some voltage exceeding 0V when V_{IN} is applied, and the LTM4732 does not soft start properly.

Fast Startup

For ultralow-noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. A larger value capacitor can be used, but care should be taken regarding leakage. While normally larger capacitors would significantly increase the regulator's startup time, the LTM4732 incorporates fast startup circuitry that increases the SET pin current to about 2.5mA during startup.

Upon startup, a 2.5mA current source remains engaged while PGSET is below the power good threshold of 465mV, unless the regulator is in thermal shutdown, SV_{IN} is too low, or $INTV_{CC}$ has fallen too low.

The fast startup circuit is permanently disabled once PGSET rises above the power good threshold, until either the part is powered down or the part is placed into SHDN by pulling the RUN pin to GND.

There is one more condition under which the 2.5mA current source is disabled during startup. The purpose of this is to prevent overcharging V_{SET}. Since the device assumes that the PGSET pin is an accurate indication of the voltage on the SET pin, it assumes that V_{OSNS} follows V_{SET} closely. However, this may not always be the case—for example, if the output capacitance is very large or when, for some reason, the output is shorted to GND. Therefore, fast charge is also disabled whenever the COMPa pin has railed at its maximum value (when V_{SET} has risen significantly about V_{OSNS}). This prevents incorrect behavior where the 2.5mA current sources stay on even if the V_{SET} has risen above its intended value.

This means that there is also a minimum SET capacitor requirement for using a fast startup without overcharging the reference voltage. This depends on the compensation network, as the part depends on the COMPa pin voltage rising to its maximum value to inform the part to pause fast charge.

The recommended minimum SET capacitance value to prevent overcharging the reference voltage is shown in Equation 5.

$$Minimum\ C_{SET} = 27 \times \frac{C_{COMP}}{V_{SET}} \qquad (5)$$

If programmable power good and fast startup capabilities are not required, the PGSET pin must be connected to 0.5V. This 0.5V could be an external voltage reference for PGSET. *Figure 37* circuit shows an example.

Forced Continuous Mode

The LTM4732 can operate in forced continuous mode (FCM) for a fast transient response and a full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive switching transitions are aligned to the clock. The negative inductor current is allowed at light loads or under large transient conditions. The FCM improves a load step transient response (see *Figure 31*). At light loads, the FCM operation is less efficient than the pulse-skipping operation, but FCM may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. The FCM must be used if the output is required to sink current. To enable FCM, connect the SYNC pin to the $INTV_{CC}$ or > 3V, or float the pin.

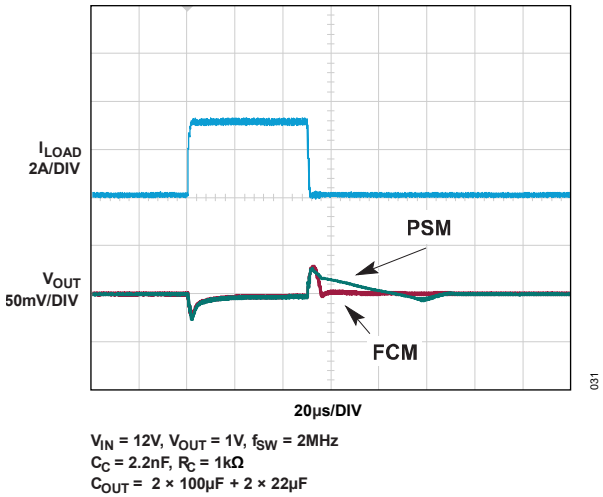


Figure 31. 0.1A to 3.1A Load Step Transient Response with and without FCM

The FCM is disabled under V_{IN} overvoltage conditions (the V_{IN} pin is held above 18V) if V_{OUT} is too high (the PGSET pin is held greater than 540mV) and is also disabled during startup until the voltage on V_{OUT} has charged up to 92.5% of its final value (as indicated when the PGSET pin rises to above 465mV). For the latter two conditions, the PGSET pin is assumed to be connected to the output voltage through an appropriate resistor. When FCM is disabled in these methods, the negative inductor current cannot be allowed, and the LTM4732 operates in PSM.

Pulse-Skipping Mode

When not operating in forced continuous mode (FCM), the LTM4732 operates in pulse-skipping mode (PSM). The negative inductor current cannot operate in this mode. Additionally, in PSM, the LTM4732 may also skip switching cycles at very light loads for improved efficiency or at very high duty cycles to achieve better dropout. To enable PSM, connect the SYNC pin to GND.

Synchronization

To synchronize the LTM4732's oscillator to an external frequency, connect a square wave to the SYNC pin. The square wave amplitude should have valleys below 0.4V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

The LTM4732 runs in FCM to maintain regulations while synchronized to an external clock. The LTM4732 may be synchronized over a 400kHz to 4MHz range. The R_T resistor should be chosen to set the LTM4732 switching frequency below the lowest synchronization input by approximately 20%. For example, if the synchronization signal is 500kHz and higher, the R_T should be selected for 400kHz.

Programmable Power Good

The LTM4732 features a programmable power good using a single resistor across the V_{OUT} and PGSET pins, as shown in Equation 6.

$$V_{OUT(PGTHRESHOLD)} = 0.5V \times \left(1 + \frac{R_{PGSET}}{49.9k\Omega}\right) + I_{PGSET} \times R_{PGSET} \quad (6)$$

If the PGSET pin increases above 540mV or decreases below 465mV, the open-drain PG pin de-asserts and becomes low impedance. The power good comparator has 5mV hysteresis. The PGSET pin current (I_{PGSET}) from the *Electrical Characteristics* table must be considered when determining the resistor. Note that the programmable power good and fast startup capabilities are disabled when PGSET is connected to 0.5V or when the device is shut down. *Table 8* suggests some 1% R_{PGSET} resistor values for common V_{OUT} configurations.

Table 8. Suggested R_{PGSET} Resistor Values

V_{OUT} (V)	R_{PGSET} (kΩ)
0.8	30.1
0.9	40.2
1	49.9
1.2	69.8
1.5	100
1.8	130
2.5	200
3.3	280
5	453

Shorted or Reversed Input Protection

Care must be taken in systems where the output is held high when the power input of the LTM4732 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM4732's output. If the V_{IN} pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is connected to V_{IN}), then the LTM4732's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN pin, the internal current drops to zero. However, if the V_{IN} pin is grounded while the output is held high, parasitic diodes inside the LTM4732 can pull large currents from the output through the V_{IN} pin. *Figure 32* shows a connection of V_{IN}

and RUN pins that allow LTM4732 to run only when the input voltage is present, thus protecting against a shorted or reversed input.

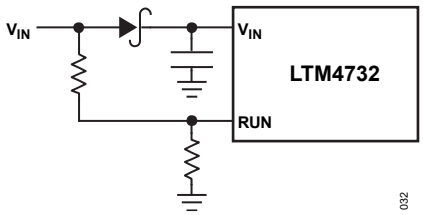


Figure 32. Reverse Input Protection

Hot-Plugging Safely

The small size, robustness, and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of the LTM4732. However, these capacitors can cause problems if the LTM4732 is plugged into a live supply (refer to the Analog Devices *Application Note 88* for a complete discussion). The low-loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pins of the LTM4732 can ring to more than twice the nominal input voltage, possibly exceeding the LTM4732's rating and damaging the device. If the input supply is poorly controlled or the LTM4732 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is by adding an electrolytic bulk capacitor to the V_{IN} network. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves the low-frequency ripple filtering, and it can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM4732 output current may need to be derated if it is required to operate at a high ambient temperature. The amount of current derating depends upon the input voltage, output power, and ambient temperature. The derating curves shown in the *Typical Performance Characteristics* section can be used as a guide. These curves were generated by the LTM4732 mounted to a 50cm^2 6-layer FR4 PCB. Boards of other dimensions and layer counts can exhibit different thermal behaviors, the user must verify proper operation over the intended system's line, load, and environmental operating conditions. *Figure 33* shows a temperature plot of the LTM4732 with 12V input, 1V output at 4A without heat sink and a no airflow condition.

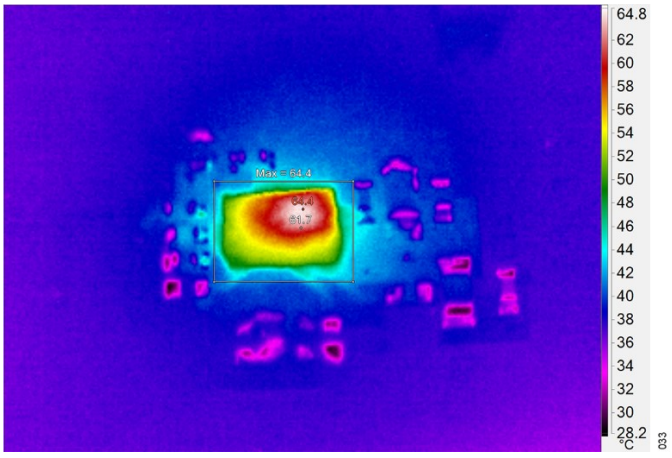


Figure 33. Thermal Image at 12V_{IN}, 1V, 4A Output, No Airflow and Heat Sink, T_A = 25°C

For increased accuracy and fidelity to the actual application, many designers use finite element analysis (FEA) to predict thermal performance. To that end, below are the thermal coefficients.

1. θ_{JA} – Thermal resistance from the junction to ambient.
2. θ_{JCbot} – Thermal resistance from the junction through the bottom of the package case to the board, see *Figure 34*.
3. θ_{JCtop} – Thermal resistance from the junction to the top of the product case.

While the meaning of each of these coefficients may be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD5112 and are quoted or paraphrased as follows.

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes called “still air”, although natural convection causes the air to move. This value is determined with the part mounted to a JESD519-defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with the component power dissipation flowing through the bottom of the package. In a typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions do not generally match the user’s application.
3. θ_{JCtop} is determined with nearly all the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate in such a way in which most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions do not generally match the user’s application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of these thermal coefficients can be individually used to predict the product's thermal performance accurately. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs. load graphs shown in the product’s data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all thermal resistances simultaneously.

A graphical representation of these thermal resistances is shown in *Figure 34*. Some thermal resistance elements, such as the heat flowing out the side of the package, are not defined by the JEDEC standard and are not shown. The blue resistances are contained within the µModule regulator, and the green is outside.

The die temperature of the LTM4732 must be lower than the maximum rating, and care should be taken in the layout of the circuit to ensure good heat sinking of the LTM4732. The bulk of the heat flow from the LTM4732 is through the bottom of the package and the pads into the printed circuit board (PCB). Consequently, a poor PCB design can cause excessive heating, impairing performance or reliability. See the *PCB Layout* section for the PCB design suggestions.

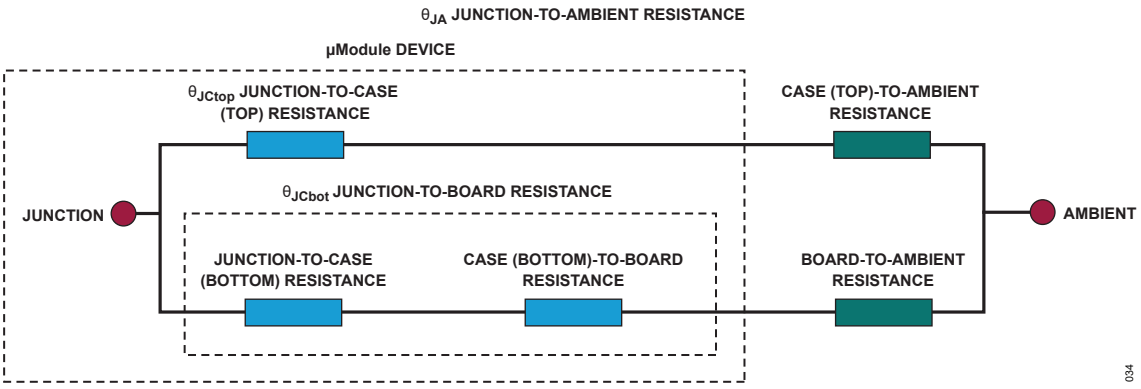


Figure 34. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

PCB Layout

Most of the headaches associated with the PCB layout have been alleviated, or even eliminated by the high level of integration of the LTM4732. The LTM4732 is, nevertheless, a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with a high level of integration, it might not be possible to achieve the specified operation with a haphazard or poor layout. See *Figure 35* for a suggested layout. Ensure that the grounding and the heat sinking conditions are acceptable.

When designing the PCB layout, the following rules must be implemented to ensure a good PCB layout design.

1. Place C_{SET}, R_{SET}, and R_T as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN}/SV_{IN} and GND connection of the LTM4732.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM4732.
4. Place the C_{IN} and C_{OUT} capacitors so that their ground current flows directly adjacent to or underneath the LTM4732.
5. Connect all the GND connections to a large copper pour or to the plane area as close as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM4732.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the PCB. Pay attention to the location and density of the thermal vias, as shown in *Figure 35*. The LTM4732 can benefit from the heat sinking afforded by vias that connect to the internal GND planes at these locations because of their proximity to the internal power handling components. The optimum number of thermal vias depends upon the PCB design. For example, if a board uses very small through holes, then it should use more thermal vias than a board that uses larger holes.

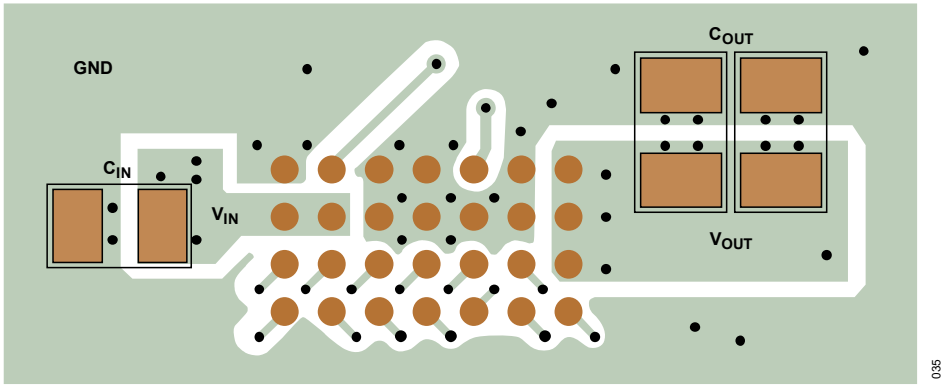


Figure 35. Layout Showing Suggested External Components, GND Plane and Thermal Vias (Top Layer)

Typical Applications

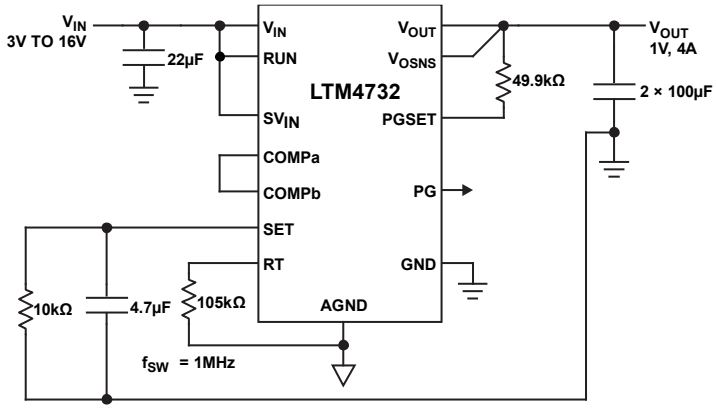


Figure 36. 1V, 4A from 3V to 16V_{IN}, 1MHz with Soft Start, Fast Startup and Power Good

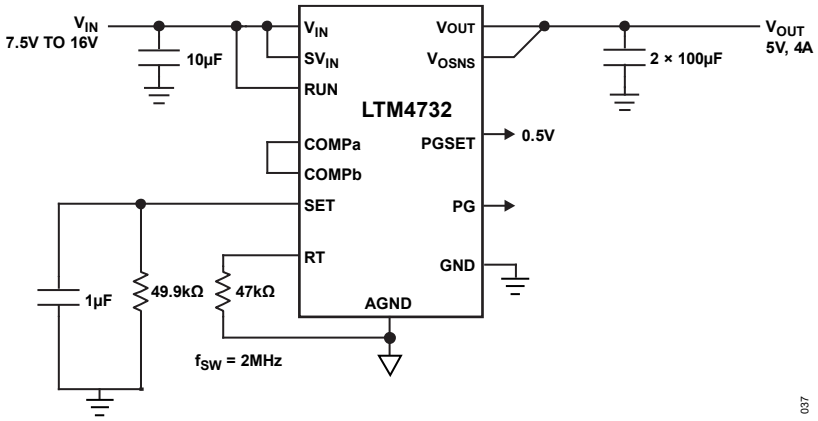
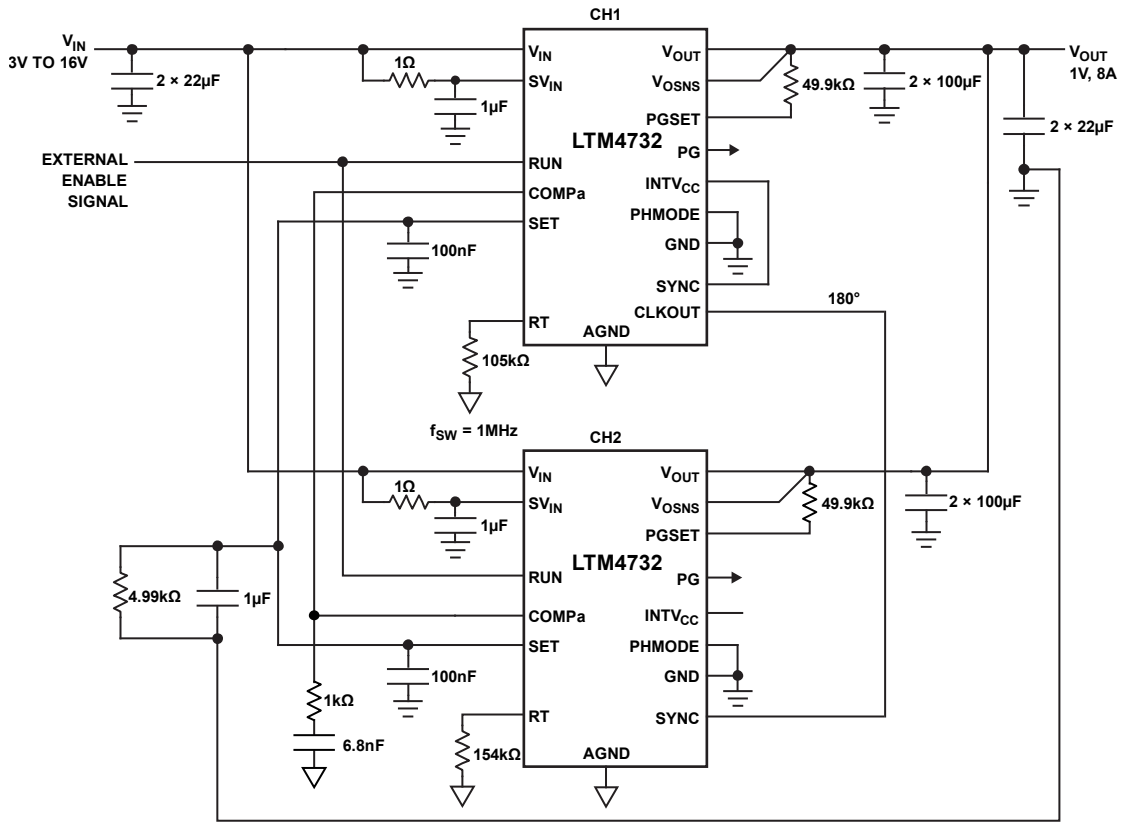


Figure 37. 5V, 4A from 7.5V to 16V_{IN}, 2MHz with Soft Start, Power Good and Fast Startup Disabled

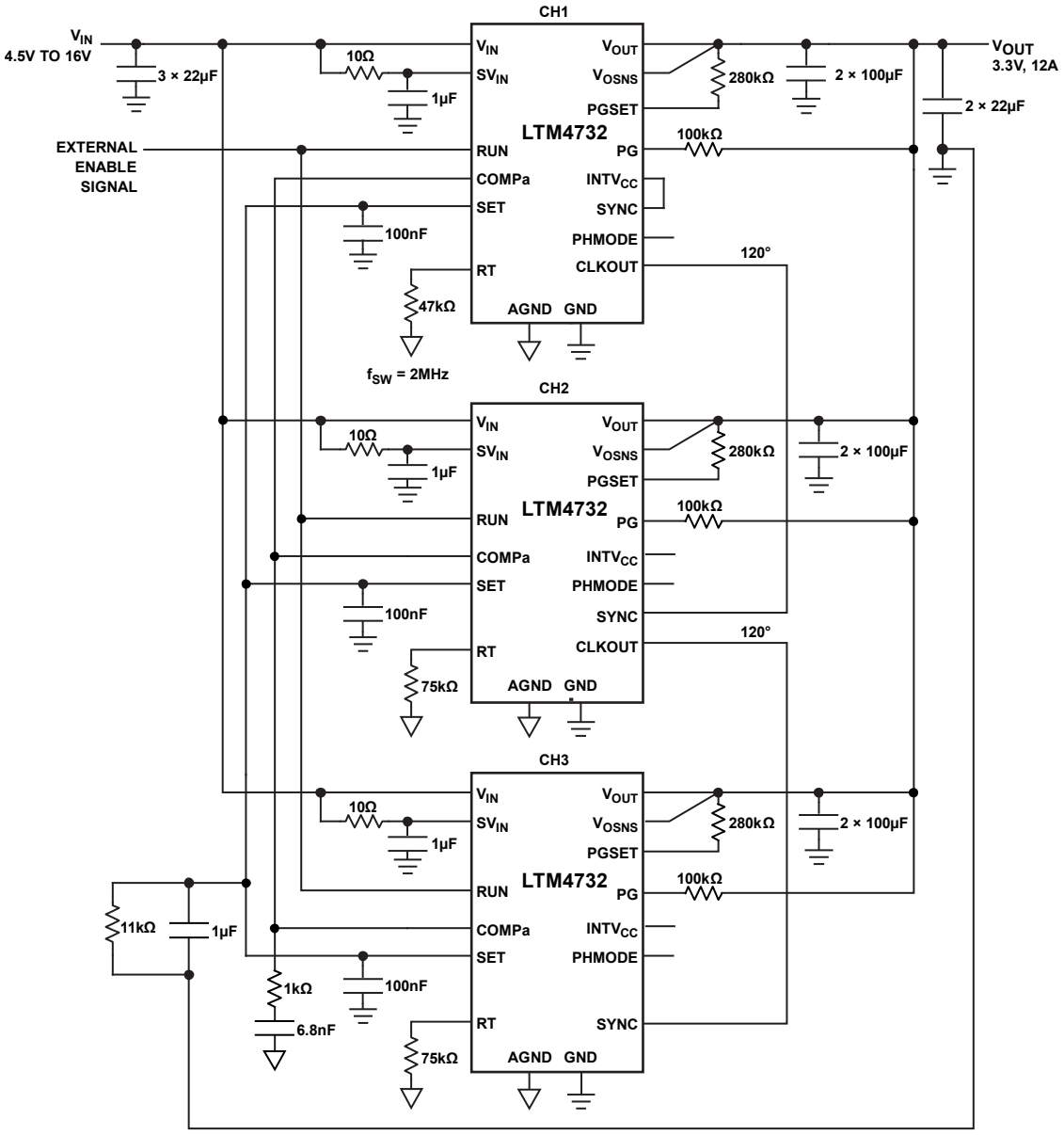


PINS NOT USED: COMPb, SW.

CH2 IS SYNCHRONIZED TO 1MHz THROUGH THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <0.8MHz (80% OF 1MHz).
COMPa PINS ARE CONNECTED TOGETHER.
PHMODE IS CONNECTED TO GND FOR 180°. PHASE SHIFT AT CLKOUT.
THE SET PINS CAN BE CONNECTED TOGETHER FOR 200µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

038

Figure 38. 2-Phase 1V, 8A from 3V to 16V_{IN}, 1MHz with Soft Start, Fast Startup and Power Good

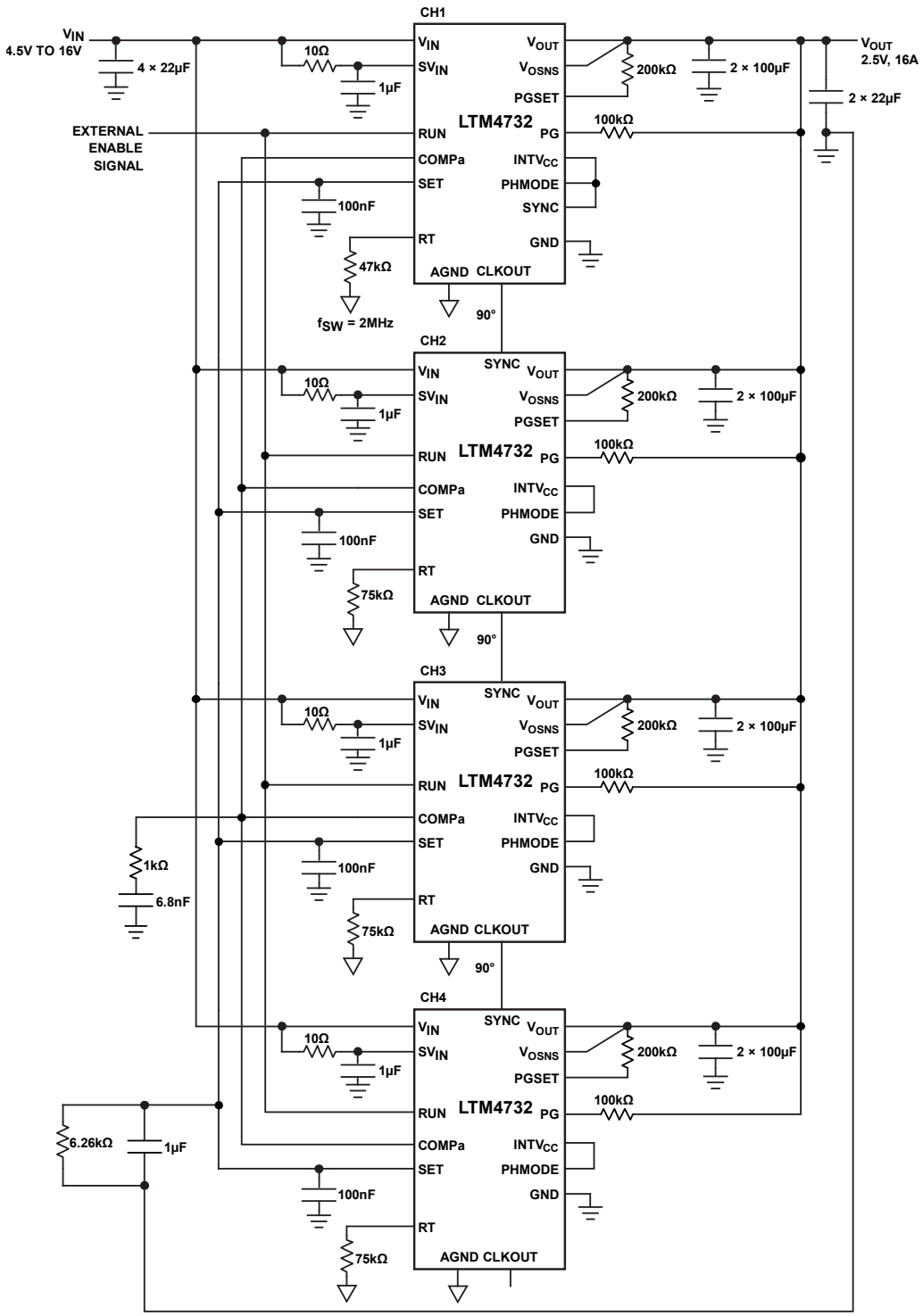


PINS NOT USED: COMPb, SW.

CH2 AND CH3 ARE SYNCHRONIZED TO 2MHz THROUGH THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET THE INTERNAL OSCILLATOR TO <1.6MHz (80% OF 2MHz).
COMPa PINS ARE CONNECTED TOGETHER.
PHMODE IS FLOATING FOR 120˚. PHASE SHIFT AT CLKOUT.
THE SET PINS CAN BE CONNECTED TOGETHER FOR 300µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

039

Figure 39. 3-Phase 3.3V, 12A from 4.5V to 16V_{IN}, 2MHz with Soft Start, Fast Startup and Power Good



PINS NOT USED: COMPb, SW.

CH2 AND CH3 ARE SYNCHRONIZED TO 2MHz THROUGH THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET THE INTERNAL OSCILLATOR TO <1.6MHz (80% OF 2MHz).
COMPa PINS ARE CONNECTED TOGETHER.
PHMODE IS CONNECTED TO $INTV_{CC}$ FOR 90˚. PHASE SHIFT AT CLKOUT.
THE SET PINS CAN BE CONNECTED TOGETHER FOR 400µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

040

Figure 40. 4-Phase 2.5V, 16A from 4.5V to 16V_{IN}, 2MHz with Soft Start, Fast Startup and Power Good

Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM8053	40V, 3.5A low EMI Silent Switcher µModule regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA
LTM8065	40V, 2.5A low EMI Silent Switcher µModule regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA
LTM8063	40V, 2A low EMI Silent Switcher µModule regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 15V, 4mm × 6.25mm × 2.22mm BGA
LTM8074	40V, 1.2A low EMI Silent Switcher µModule regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 12V, 4mm × 4mm × 1.82mm BGA
LTM8024	40V, dual 3.5A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 9mm × 11.25mm × 3.32mm BGA
LTM8078	40V, dual 1.4A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 10V, 6.25mm × 6.25mm × 2.32mm BGA
LTM8060	40V, quad 3A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 16mm × 11.9mm × 3.32mm BGA
LTM8060F	40V, quad 3A Silent Switcher µModule regulator with package-level EMI shield	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 16mm × 11.9mm × 2.9mm PSGA
LTM8051	40V, quad 1.2A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 6.25mm × 11.25mm × 2.32mm BGA
LTM8080	40V_{IN}, dual 500mA or single 1A ultralow noise, ultrahigh PSRR µModule regulator	3.5V ≤ V_{IN} ≤ 40V, 0V ≤ V_{OUT} ≤ 8V, 6.25mm × 9mm × 3.32mm BGA
LTM4657	8A µModule regulator, pin compatible with LTM4626, LTM4638 and LTM4640	3.1V ≤ V_{IN} ≤ 20V, 0.5V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule regulator, pin compatible with LTM4638, LTM4640, and LTM4657	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule regulator, pin compatible with LTM4626, LTM4640, andLTM4657	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 5.02mm BGA
LTM4640	20V_{IN}, 20A step-down DC-to-DC µModule regulator, pin compatible with LTM4626, LTM4638, and LTM4657	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 3.3V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4702	16V_{IN} 8A ultralow noise Silent Switcher 3 µModule regulator, pin compatible with LTM4703 and LTM4707	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 5.7V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4703	16V_{IN} 12A ultralow noise Silent Switcher 3 µModule regulator, pin compatible with LTM4702 and LTM4707	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 6V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4707	16V_{IN} 16A ultralow noise Silent Switcher 3 µModule regulator, pin compatible with LTM4702 and LTM4703	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 6V, 6.25mm × 6.25mm × 5.07mm BGA

OUTLINE DIMENSIONS

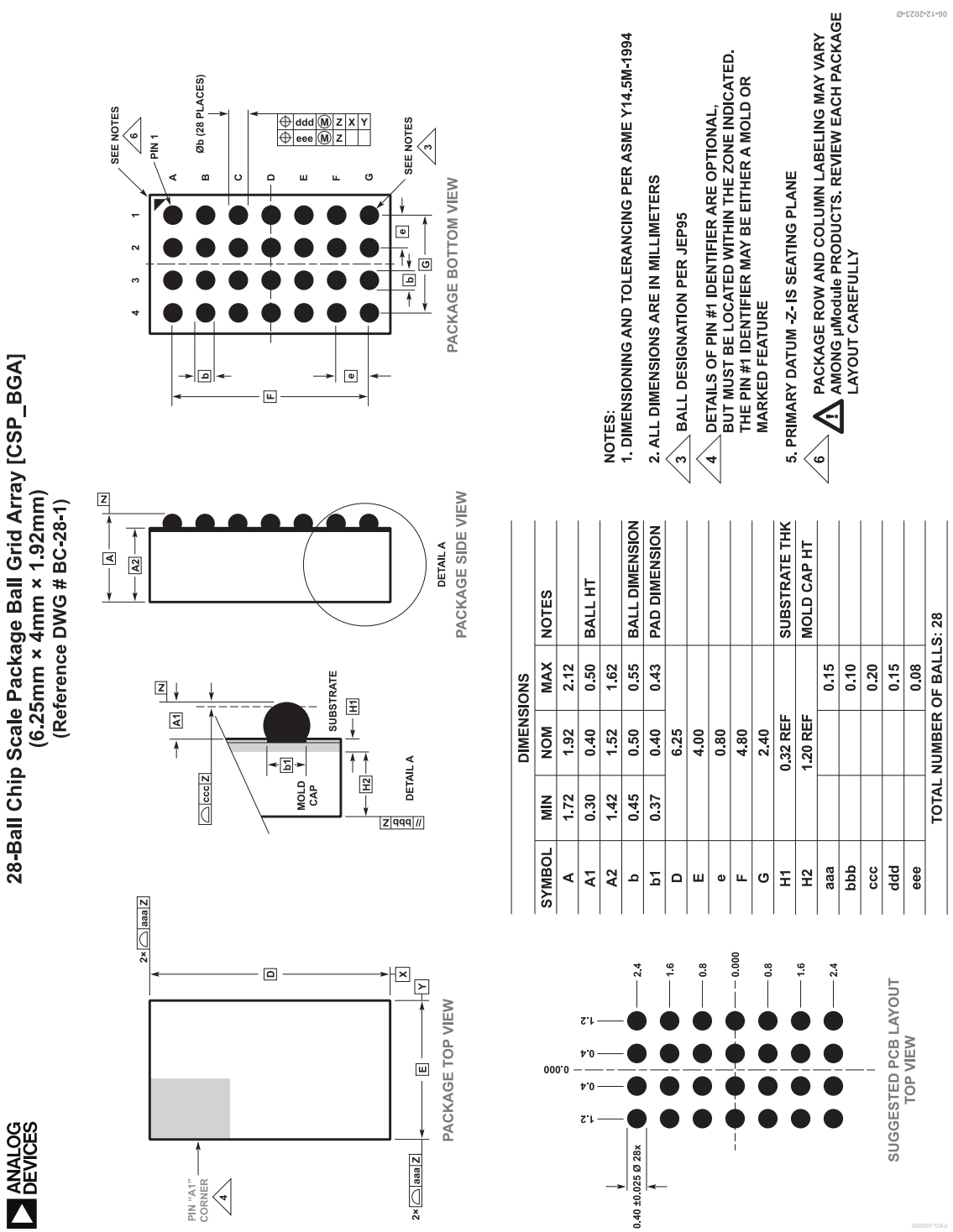


Figure 41. 28-Pin 6.25mm × 4mm × 1.92mm BGA

ORDERING GUIDE

Table 9. Ordering Guide

MODEL	TEMPERATURE RANGE[1]	PACKAGE DESCRIPTION	PACKAGE OPTION
LTM4732EY#PBF	–40°C to 125°C	Part marking: 4732 SAC305 (RoHS) pad finish* e1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*28-Pin 6.25mm × 4mm × 1.92mm* BGA
LTM4732IY#PBF	–40°C to 125°C	Part marking: 4732 SAC305 (RoHS) pad finish* e1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*28-Pin 6.25mm × 4mm × 1.92mm* BGA

1 The LTM4732 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4732E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and the correlation with statistical process controls. The LTM4732I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Contact the factory for parts specified with wider operating temperature ranges. *Pad finish code is per IPC/JEDEC J-STD-609. The device temperature grade is indicated by a label on the shipping container.This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to *Recommended LGA and BGA PCB assembly and manufacturing procedures.*

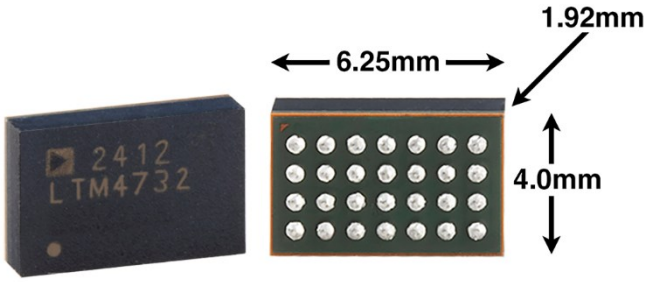
LGA and BGA package and tray drawings.

Table 10. Evaluation Boards

PART NUMBER	DESCRIPTION
EVAL-LTM4732-AZ	16V, 4A ultralow noise Silent Switcher 3 µModule regulator.

SELECTOR GUIDE

Package Photos



(Part Marking Is Laser Mark)

Design Resources

	SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	**Design** ▶ Selector guides ▶ Evaluation (demo) boards and Gerber files ▶ Free design tools, including LTspice® and LTpowerCAD®	**Manufacturing** ▶ Quick start guide ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Sort table of products by parameters and download the result as a spread sheet. ▶ Search using the Quick Power Search parametric table. Quick Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Features ☐ Low EMI ☐ Ultrathin ☐ Internal Heat Sink Multiple Outputs	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	