

2.0-7.2 GHz SPDT Switch

Features

- Broadband frequency range: 2.0 to 7.2 GHz
- Low insertion loss: 0.50dB typical @ 2.4 GHz
- Low insertion loss: 0.58dB typical @ 5.8 GHz
- High isolation: 40 dB @ 5.8 GHz
- High $P_{0.1dB}$ of 32 dBm
- Wide 1.6 to 5 V supply voltage range
- Integrated DC blocking capacitors
- Small DFN (6-pin, 1.0 mm x 1.0 mm x 0.45 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

Applications

- IEEE 802.11a/b/g/n/ac/ax/be WLAN Networks
- ISM band radios
- WLAN repeaters
- Low power transmit receive systems
- Smartphones

General Description

The AW13112DNR is a Silicon-On-Insulator(SOI) SPDT switch with low insertion loss, high isolation and high linearity at low supply voltage. It can be used to support mode switching in WLAN applications.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

The AW13112DNR has integrated DC blocking capacitors, so no external DC blocking capacitors are required.

The AW13112DNR is provided in a compact DFN 1.0 mm x 1.0 mm x 0.45 mm-6L package.

Typical Application Circuit

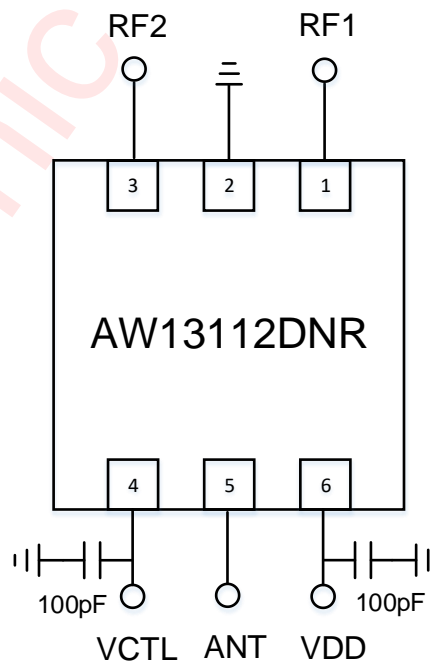


Figure 1 Typical Application Circuit of AW13112DNR

Pin Configuration And Top Mark

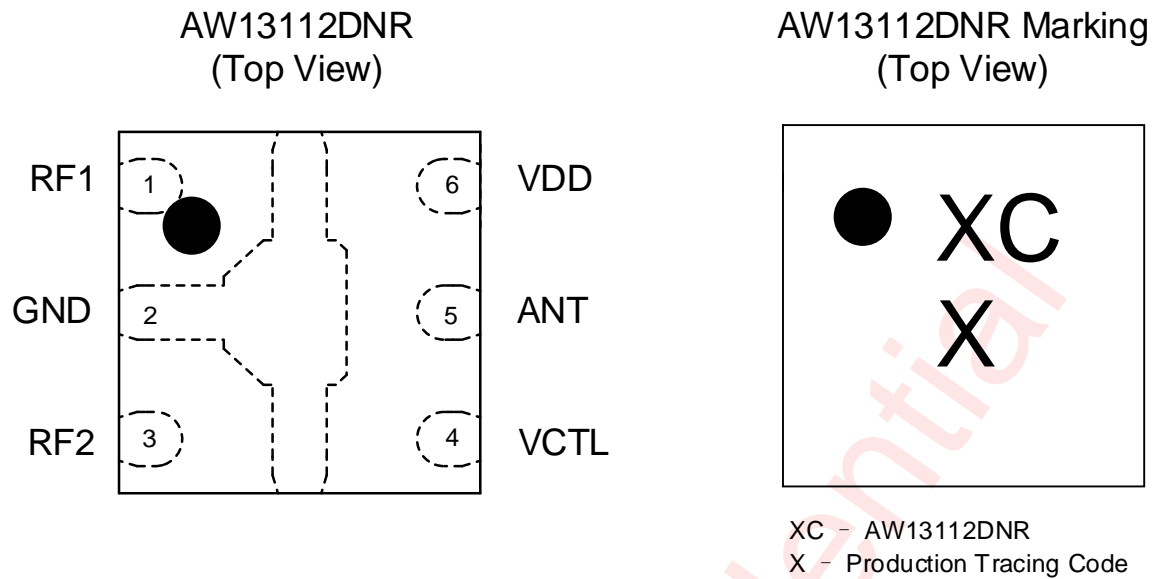


Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	RF1	RF I/O path 1
2	GND	Ground
3	RF2	RF I/O path 2
4	VCTL	DC control voltage
5	ANT	Antenna port
6	VDD	DC power supply

Functional Block Diagram

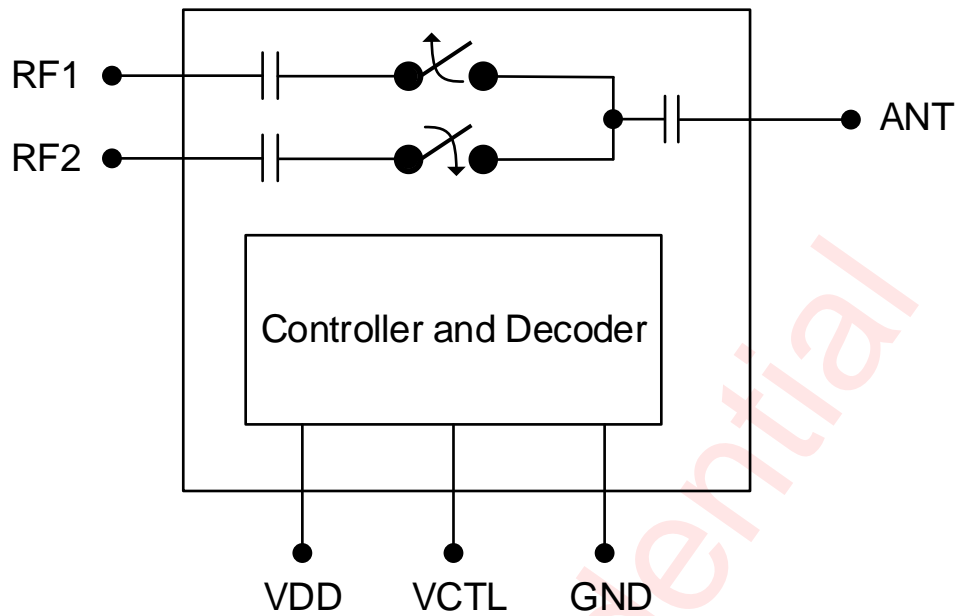


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13112DNR	-40°C~90°C	DFN 1.0mmX1.0mm -6L	XC	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range VDD		0 V to 5.5 V
Control Voltage Range	VCTL	0 V to 4.5 V
RF input power(RF1/RF2)		33 dBm
Operating Free-air Temperature Range		-40°C to 90°C
Storage Temperature T _{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD (NOTE 2)		
HBM (ESDA/JEDEC JS-001)		±1000V
CDM (ESDA/JEDEC JS-002)		±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001.

Electrical Characteristics

VDD=3.3V, VCTL=0/3.3V, PIN=0dBm, T_A=+25°C, Z₀=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
VDD	Supply Voltage		1.6	3.3	5.0	V
IDD	Supply Current			6	20	μA
VCTL_H VCTL_L	Control Voltage High Low		1.6 0		3.6 0.3	V
ICTL	Control Current	VCTL = 3.3V		0.1	1	μA
RF Specifications						
IL	Insertion loss(ANT pin to RF1/RF2)	2.0-3.0GHz 3.0-6.0GHz 6.0-7.2GHz		0.50 0.58 1.00	0.75 0.90 1.40	dB dB
ISO	Isolation (ANT pin to RF1/RF2)	2.0-3.0GHz 3.0-6.0GHz 6.0-7.2GHz	25 30 25	30 40 30		dB dB
RL	Input return loss (ANT pin to RF1/RF2)	2.0-3.0GHz 3.0-6.0GHz 6.0-7.2GHz	10 14 10	17 20 15		dB dB
P _{0.1dB}	0.1dB Compression Point (ANT pin to RF1/RF2)	0.5GHz–6GHz		32		dBm
2f ₀	Second Harmonics	f ₀ =2.4GHz, PIN=+24dBm,CW		-68		dBm
3f ₀	Third Harmonics	f ₀ =2.4GHz, PIN=+24dBm,CW		-58		dBm
t _{ON}	Turn-on Switching Time	50% of final control voltage to 90% of final RF power, switching between RF1/2		180	380	nS

Timing Diagram (Power On And Off Sequence)

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal VCTL should be set to 0V unless VDD is set in the operating voltage range.

Power ON:

- 1) Apply voltage supply --- VDD
- 2) Set Controls---VCTL
- 3) Apply RF input

Change switch position from one RF port to another:

- 1) Remove RF input
- 2) Change control voltages VCTL to set the switch to desired RF port
- 3) Apply RF input

Power OFF:

- 1) Remove RF input
- 2) Remove control voltages-VCTL
- 3) Remove VDD input

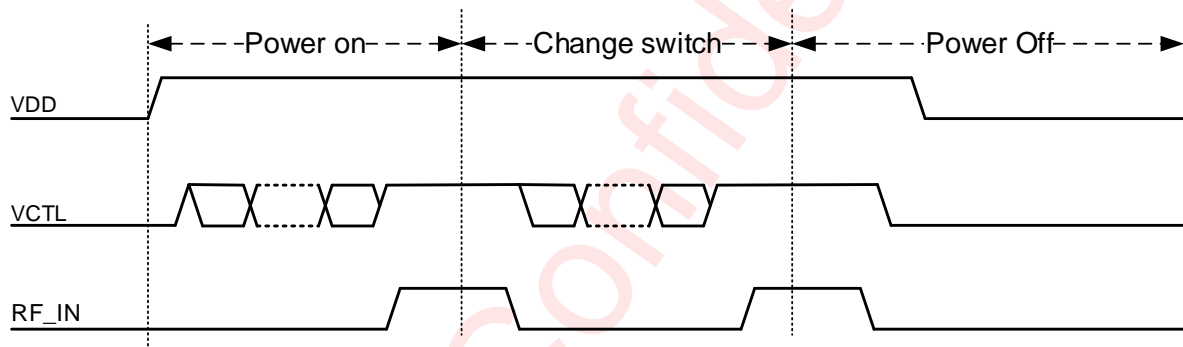
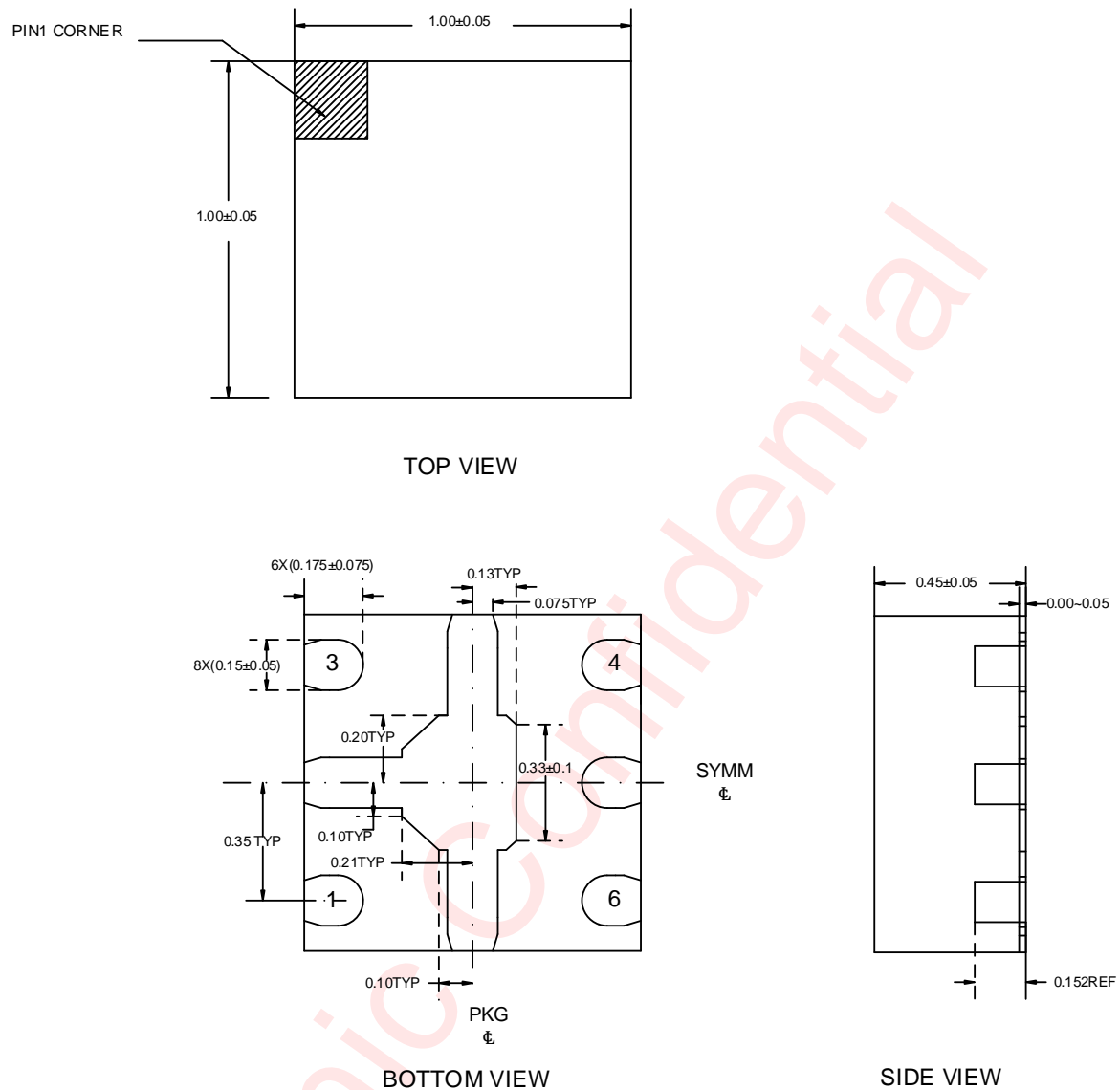


Figure 4 Power on/Change switch/Power off sequence

CONTROL LOGIC

State	Active Path	VCTL
0	ANT to RF2	0
1	ANT to RF1	1

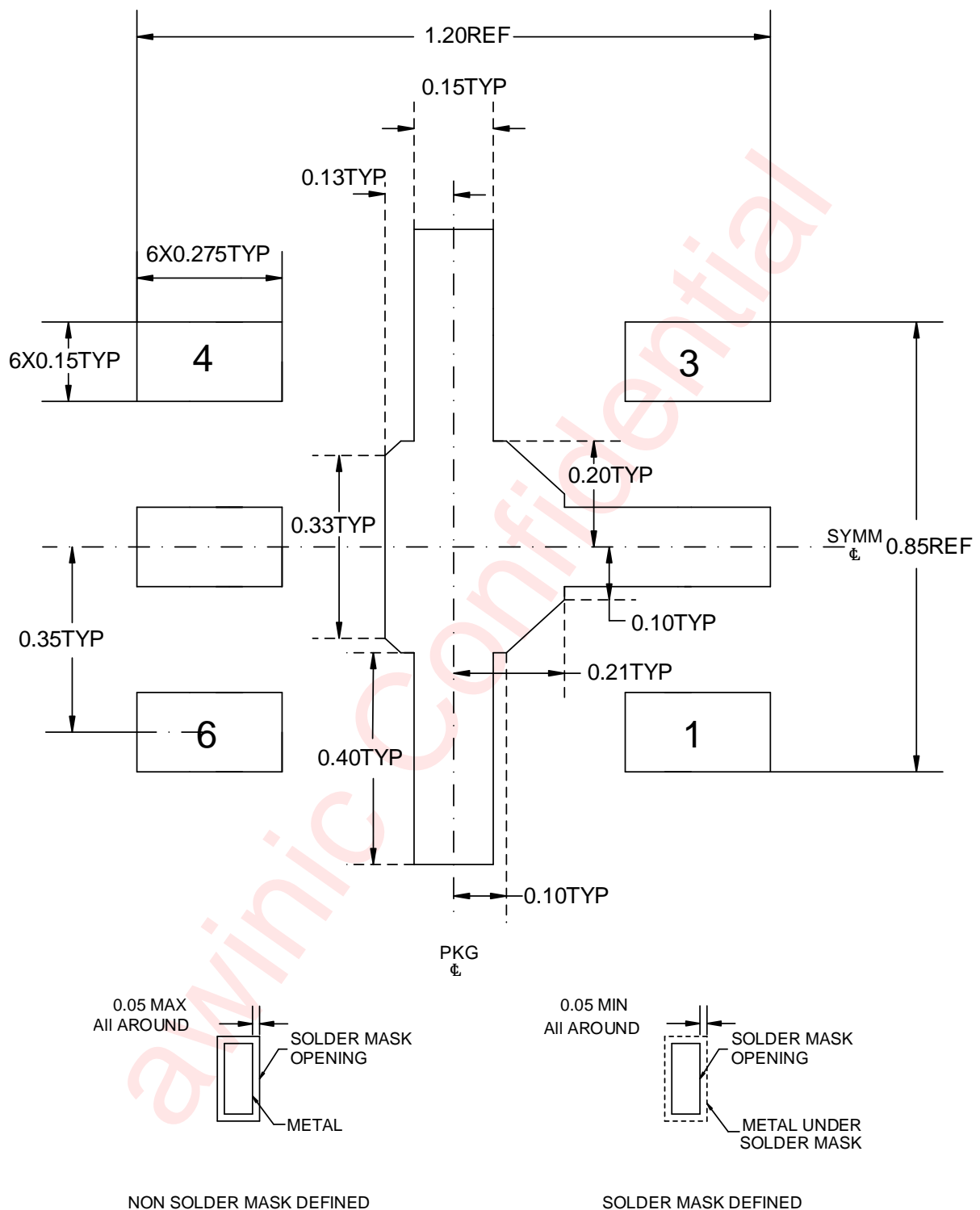
Package Outline Dimensions



Unit: mm

Figure 5 Package Outline

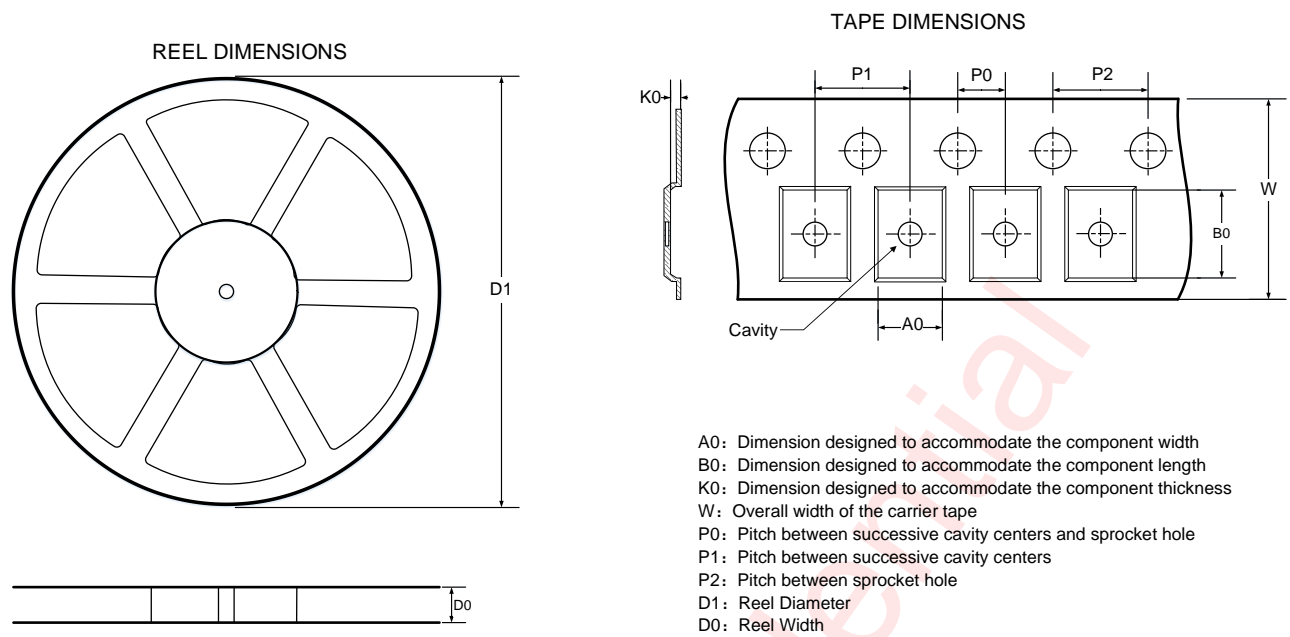
Land Pattern Data



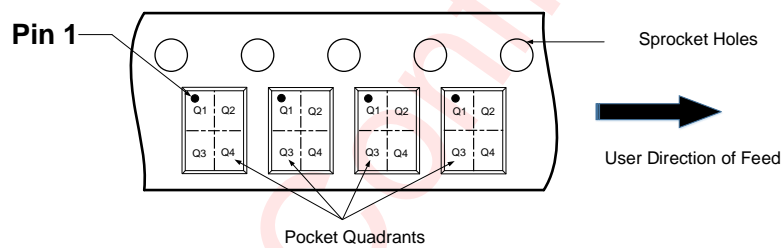
Unit: mm

Figure 6 Land Pattern

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.14	1.17	0.56	2	4	4	8	Q1

All dimensions are nominal

Figure 7 Tape and Reel

Revision History

Vision	Date	Change Record
V1.0	August 2020	Officially Released
V1.1	October 2020	Add the spec IL, ISO, RL and tON
V1.2	December 2020	Change minimum VDD to 1.6 V
V1.3	April 2021	Update spec RL , ISO and frequency
V1.4	December 2021	Support Ax
V1.5	April 2023	Update package outline
V1.6	June 2023	Update the description of applications

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