0.1-3.8GHz SP8T Diversity Switch with MIPI

Features

- Broadband frequency range: 0.1 to 3.8 GHz
- Low insertion loss: 0.76dB typical @ 2.7 GHz
- High isolation: 24dB typical @ 2.7 GHz
- P0.1dB @ 28dBm
- MIPI RFFE V2.1 interface
- Small QFN 2.0mm x 2.0mm x 0.55mm - 14L package
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

Applications

- 2G/3G/4G antenna diversity
- Cellular modems , tablets and USB Devices
- Other RF front-end modules

General Description

The AW13508 is a SP8T switch with low insertion loss and high isolation. It can be used to support band switching and mode switching in antenna diversity systems for 2G/3G/4G, data cards and tablets.

The AW13508 is perfectly compatible with MIPI RFFE V2.1 control interface. It is provided in a compact 2.0mm x 2.0mm, 14-pin QFN package.

Typical Application Circuit

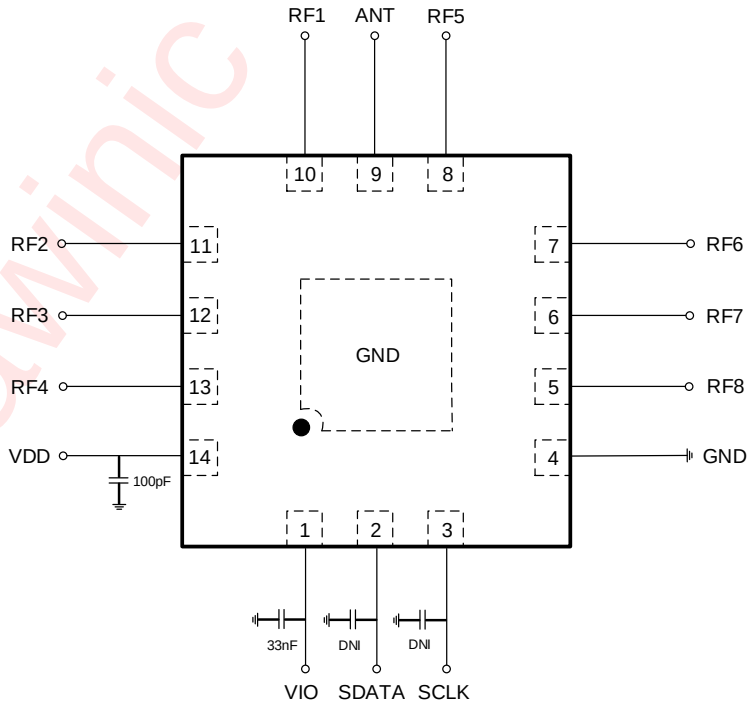
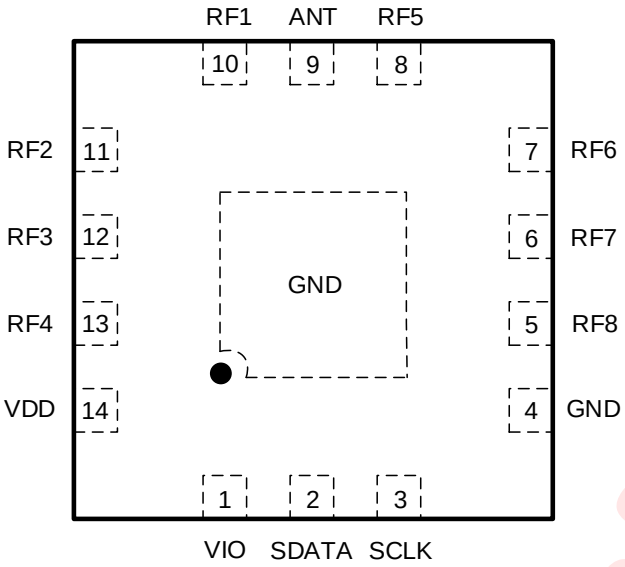


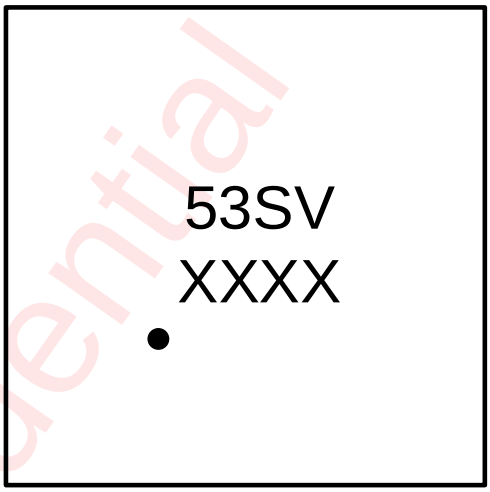
Figure 1 Typical Application Circuit of AW13508

Pin Configuration And Top Mark

AW13508QNR
(Top View)



AW13508QNR Marking
(Top View)



53SV – AW13508QNR

XXXX – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	VIO	Supply voltage for MIPI
2	SDATA	MIPI data input/output
3	SCLK	MIPI clock
4	GND	Ground
5	RF8	RF8 port
6	RF7	RF7 port
7	RF6	RF6 port
8	RF5	RF5 port
9	ANT	Antenna port
10	RF1	RF1 port

11	RF2	RF2 port
12	RF3	RF3 port
13	RF4	RF4 port
14	VDD	Power supply

Functional Block Diagram

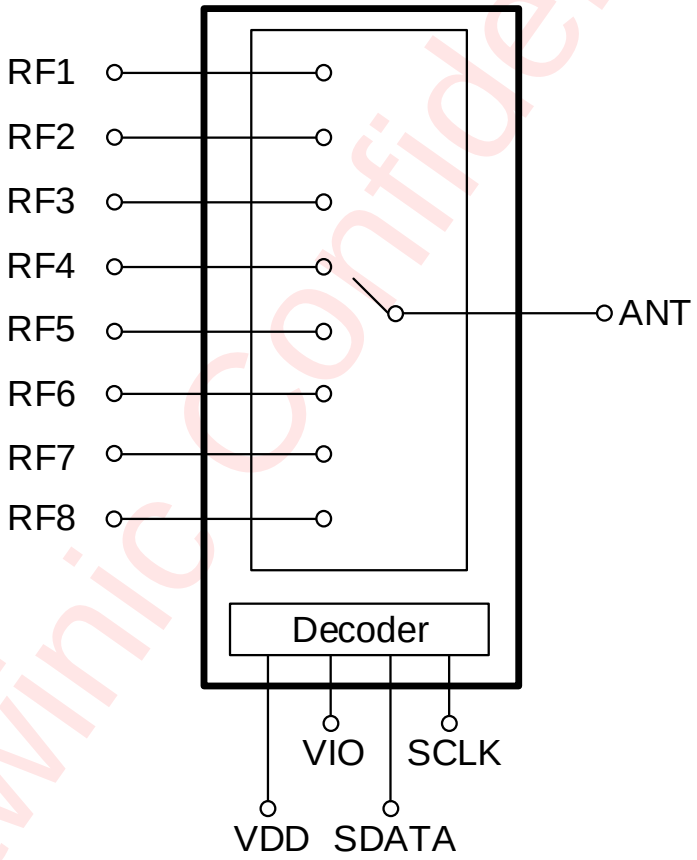


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13508QNR	-40°C～85°C	QFN 2.0mm x 2.0mm x 0.55mm -14L	53SV	MSL1	ROHS+HF	3000 units/Tape and Reel

Absolute Maximum Ratings (NOTE 1)

PARAMETERS	RANGE
Interface Supply Voltage Range V_{DD}	-0.3V to 3.3V
Supply Voltage VIO for MIPI	-0.3V to 2.0V
Interface Control Voltage Range SDATA, SCLK	-0.3V to 2.0V
RF input power (RF1 to RF8)	30dBm
Operating Free-air Temperature Range	-40°C to 85°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM(Human Body Model)(NOTE 2)	±1000V
CDM (Charged Device Model) (NOTE 3)	±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

Electrical Characteristics

V_{DD}=2.8V,V_{IO}=1.8V, P_{IN}=0dBm, VSWR=1:1,Temp=25°C. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
V_{DD}	Power supply		2.4	2.8	3.0	V
V_{IO}	Supply voltage for MIPI		1.65	1.8	1.95	V
I_{DD}	V_{DD} Supply Current	Active Mode		37	65	μA
		Low Power Mode		22	35	μA
I_{IO}	V_{IO} Supply Current			4	10	μA
V_{CTL_H}	SDATA,SCLK Control Voltage High	Must not exceed V_{IO} voltage	0.8* V_{IO}	V_{IO}	1.95	V
V_{CTL_L}	SDATA,SCLK Control Voltage Low	Must not exceed V_{IO} voltage	0	0	0.3*V_{IO}	V
T_{SW}	Switching Speed One RF port to another	10% to 90% RF		0.5	1.5	μs
RF Specifications						
IL	Insertion loss (ANT pin to RF1/2/3/4/5/6/7/8 pins)	0.1-1.0GHz		0.53	0.75	dB
		1.0-2.0GHz		0.58	0.80	dB
		2.0-2.7GHz		0.76	0.98	dB
		3.3-3.8GHz		0.88	1.23	dB
RL	Return loss (ANT pin to RF1/2/3/4/5/6/7/8 pins)	0.1-1.0GHz	18	25		dB
		1.0-2.0GHz	15	20		dB
		2.0-2.7GHz	12	15		dB
		3.3-3.8GHz	9	12		dB
ISO	Isolation (ANT pin to RF1/2/3/4/5/6/7/8 pins)	0.1-1.0GHz	28	35		dB
		1.0-2.0GHz	24	30		dB
		2.0-2.7GHz	20	24		dB
		3.3-3.8GHz	16	21		dB
2f0	Second Harmonics (ANT pin to RF1/2/3/4/5/6/7/8 pins)	Freq=900MHz, PIN=+26dBm,CW		-58		dBm
3f0	Third Harmonics (ANT pin to RF1/2/3/4/5/6/7/8 pins)	Freq=900MHz, PIN=+26dBm,CW		-59		dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
2f0	Second Harmonics (ANT pin to RF1/2/3/4/5/6/7/8 pins)	Freq=1900MHz, PIN=+26dBm,CW		-54		dBm
3f0	Third Harmonics (ANT pin to RF1/2/3/4/5/6/7/8 pins)	Freq=1900MHz, PIN=+26dBm,CW		-58		dBm
P0.1dB	0.1dB Compression Point (ANT pin to RF1/2/3/4/5/6/7/8 pins)	0.1-3.8GHz		28		dBm

Power ON and OFF Sequence

It is important that the user observes the correct power on and off sequence to avoid damaging the device.

Power ON –

(1) Apply voltage supply - V_{DD}

(2) Wait 100μs or greater and then apply logic supply - V_{IO}

(3) Wait 10μs or greater and then apply MIPI bus signals – SCLK and SDATA

(4) Wait 5μs or greater after MIPI Trigger falling edge and then apply the RF Signal

Power OFF –

(1) Remove the RF Signal

(2) Remove MIPI bus signals – SCLK and SDATA

(3) Remove logic supply - V_{IO}

(4) Remove voltage supply - V_{DD}

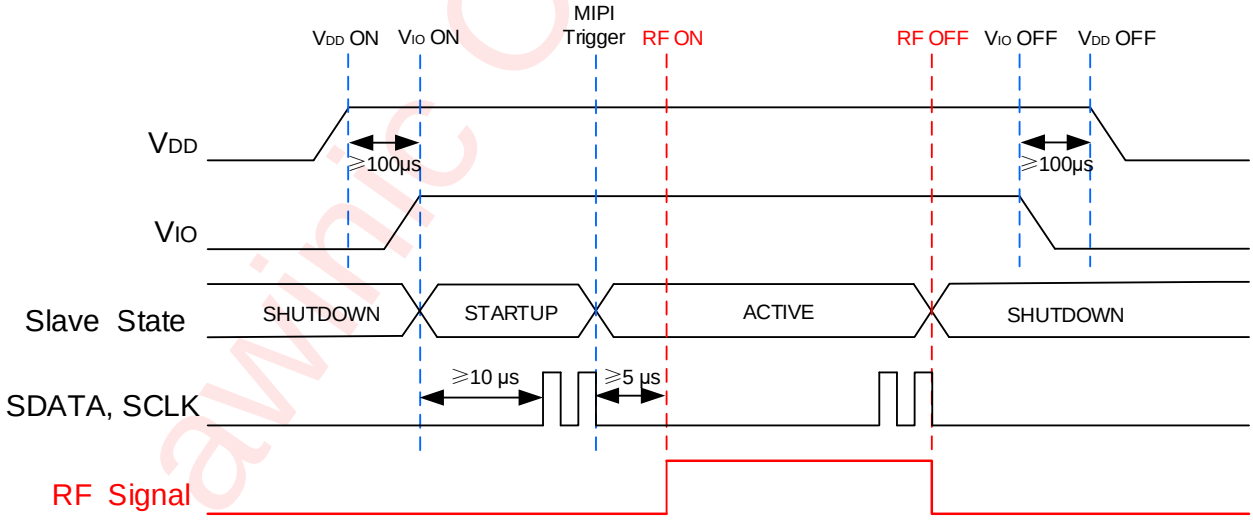


Figure 4 Power ON and OFF Sequence

MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1.

TABLE1: MIPI FEATURES

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	No	

TABLE2: Start-up Behavior

Feature	State	Comment
Power status	Low power mode	Low power mode after start-up
Trigger function	Enable	Enable after start-up. Programmable via register

MIPI Read and Write Timing

Register 0 Write:

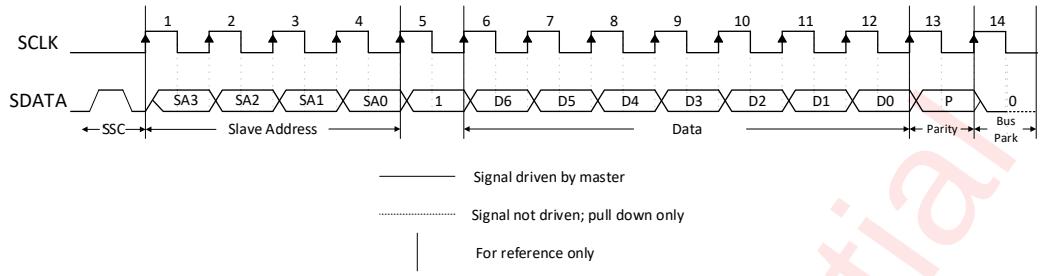


Figure 5 Register 0 Write Command Sequence

Register Write:

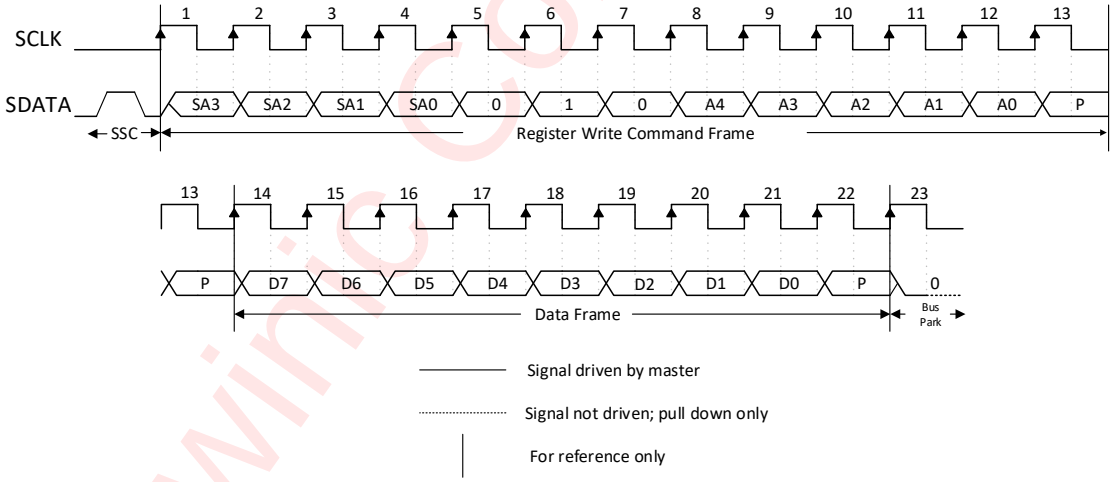


Figure 6 Register Write Command Sequence

Register Read:

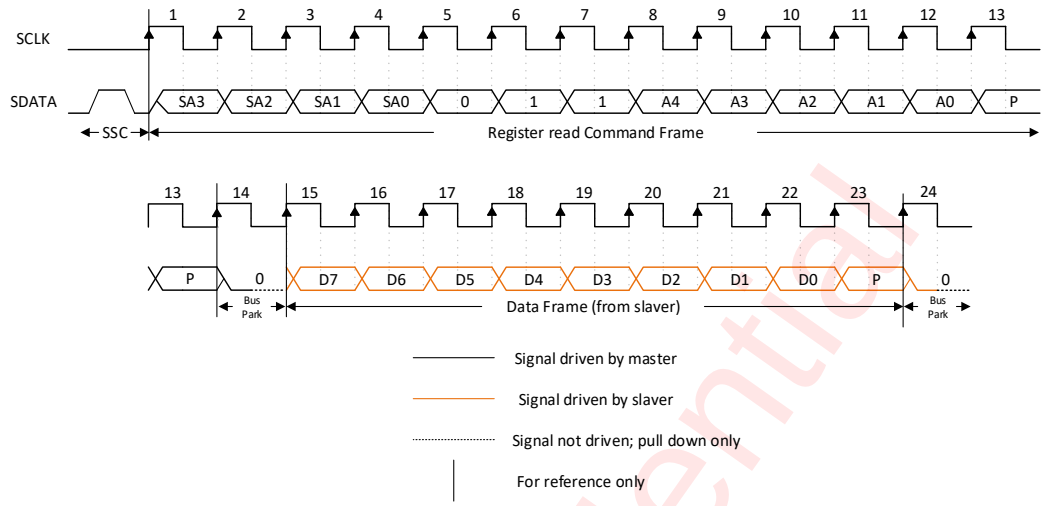


Figure 7 Register Read Command Sequence

Extended Register Write:

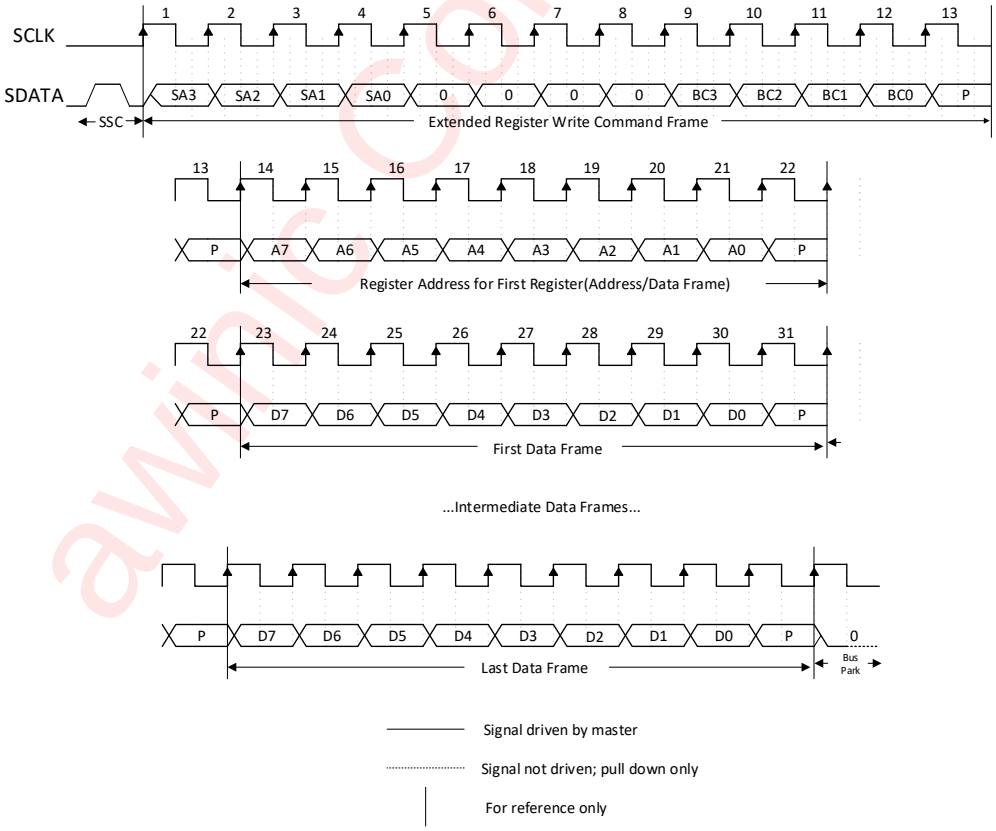


Figure 8 Extended Register Write Command Sequence

Extended Register Read:

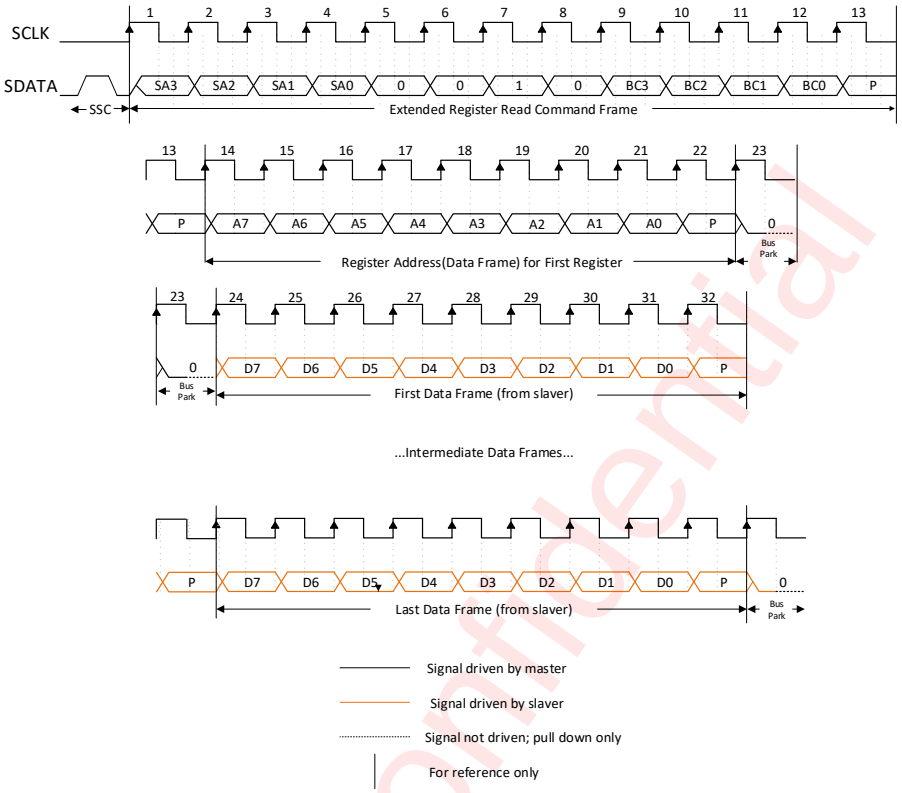


Figure 9 Extended Register Read Command Sequence

Masked Write:

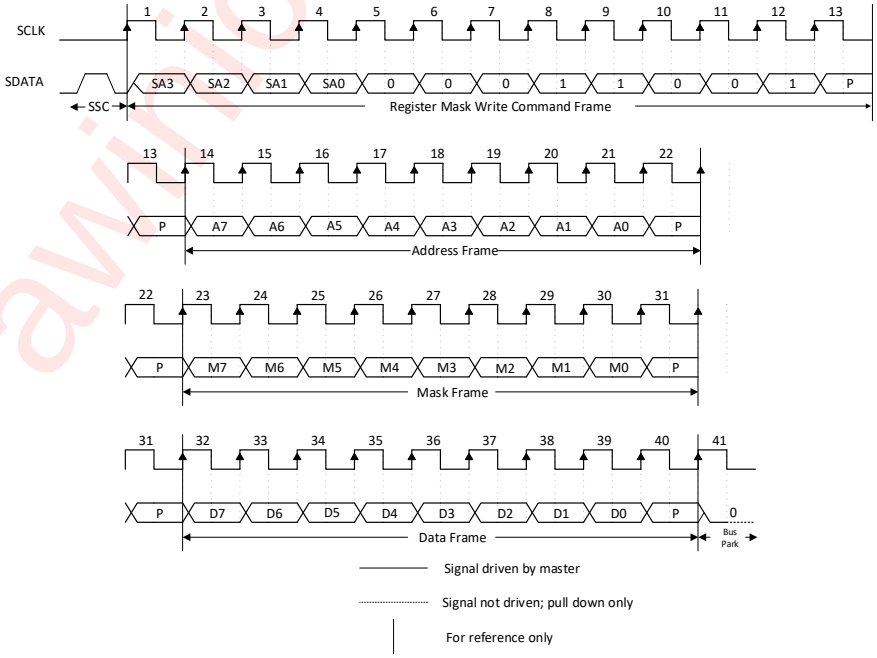


Figure 10 Masked Write Command Sequence

Register Configuration

Register Detailed Description

REGISTER_0：Mode Control Register(Address 0000h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	Reserved	Reserved	RW	No	0-10	0
6:0	MODE_CTRL	0000000: RF4 on 0000001: RF8 on 0000010: RF3 on 0000011: RF7 on 0000100: RF2 on 0000101: RF6 on 0000110: RF1 on 0000111: RF5 on 0001000: ISOLATION …… 1111111: ISOLATION	RW MW	No	Yes 0-10	0000000

RFFE_STATUS：RFFE Status Register(Address 001Ah)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal operation 1: software reset	W	No	No	0
6	CMD_FR_P_ERR	Command Frame received with a parity error	RW	No	No	0
5	CMD_LEN ERR	Command Sequence received with an incorrect length	RW	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	RW	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	RW	No	No	0
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	RW	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	RW	No	No	0
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	RW	No	No	0

GSID0_1：Group ID 0-1 Register(Address 001Bh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID0	Group Slave ID0	RW	No	No	0000
3:0	GSID1	Group Slave ID1	RW	No	No	0000

PM_TRIG：Pwr_mode and Trig Register(Address 001Ch)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	PWR_MODE[1]	0: normal operation 1: low power	RW MW	Yes	No	1
6	PWR_MODE[0]	0: active 1: start up – Reset all register to default	RW MW	Yes	No	0
5:3	TRIGGER_MASK	Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register	RW MW	No	No	000
2:0	TRIGGER	Setting bit TRIGGER[n] loads TRIGGER[n]'s associated register	RW MW	Yes	No	000

PRODUCT_ID：Product ID Register(Address 001Dh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Lower eight bits of Product ID	R	No	No	0x03

MANUFACTURER_ID：Manufacture ID Register(Address 001Eh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	MFG_ID	Lower eight bits of Manufacturer ID	R	No	No	0x49

MAN_USID：User ID Register(Address 001Fh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	MFG_ID	Upper four bits of Manufacturer ID	R	No	No	0100
3:0	USID	Unique Slave ID	RW	No	No	1011

EXT_PRODUCT_ID：Extend Product ID Register(Address 0020h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	PROD_ID	Upper eight bits of Product ID	R	No	No	0x00

REVISION_ID：Revision ID Register(Address 0021h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	REV_ID	Revision ID	R	No	No	0x00

GSID2_3：Group ID 2-3 Register(Address 0022h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:4	GSID2	Group Slave ID2	R/W	No	No	0000
3:0	GSID3	Group Slave ID3	R/W	No	No	0000

UDR_RST：UDR Reset Register(Address 0023h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	UDR_RST	Reset all configurable non-RFFE reserved register to default values 0: normal 1: software reset	R/W	Yes	No	0
6:0	RESERVED	Reserved	R/W	No	No	0x00

ERR_SUM：Error Command Status Register(Address 0024h)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7	SPARE	Reserved for future use	R/W	No	No	0
6	COM_FR_P_ERR	Command Frame received with a parity error	R/W	No	No	0
5	COM_LEN_ERR	Command Sequence received with an incorrect length	R/W	No	No	0
4	ADDR_FR_P_ERR	Address Frame received with a parity error	R/W	No	No	0
3	DATA_FR_P_ERR	Data Frame received with a parity error	R/W	No	No	0
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	R/W	No	No	0
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	R/W	No	No	0

0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	R/W	No	No	0

BUS_LD：SDATA Driver Strength Register(Address 002Bh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:1	reserved	reserved	R/W	No	No	0x00
0	BUS_LD	SDATA drive strength 0: 50pf 1: 80pf	R/W	No	No	0

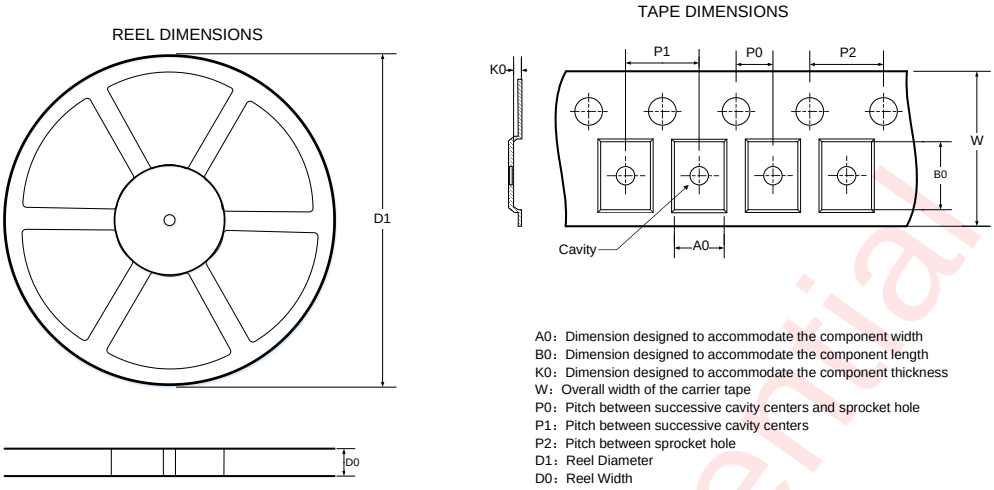
EXT_TRIG_MASK：Extend Trig Mask Register(Address 002Dh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	EXT_TRIG_MASK	Setting bit EXT_TRIG_MASK[n] disables EXT_TRIG[n]	R/W MW	No	No	0xFF

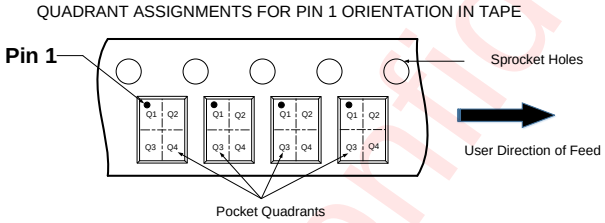
EXT_TRIG：Extend Trig Register(Address 002Eh)

Bit	Symbol	Description	R/W	B/G	Trig	Default
7:0	EXT_TRIG	Setting bit EXT_TRIG[n] loads EXT_TRIG[n]'s associated register	R/W MW	Yes	No	0x00

Tape And Reel Information



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



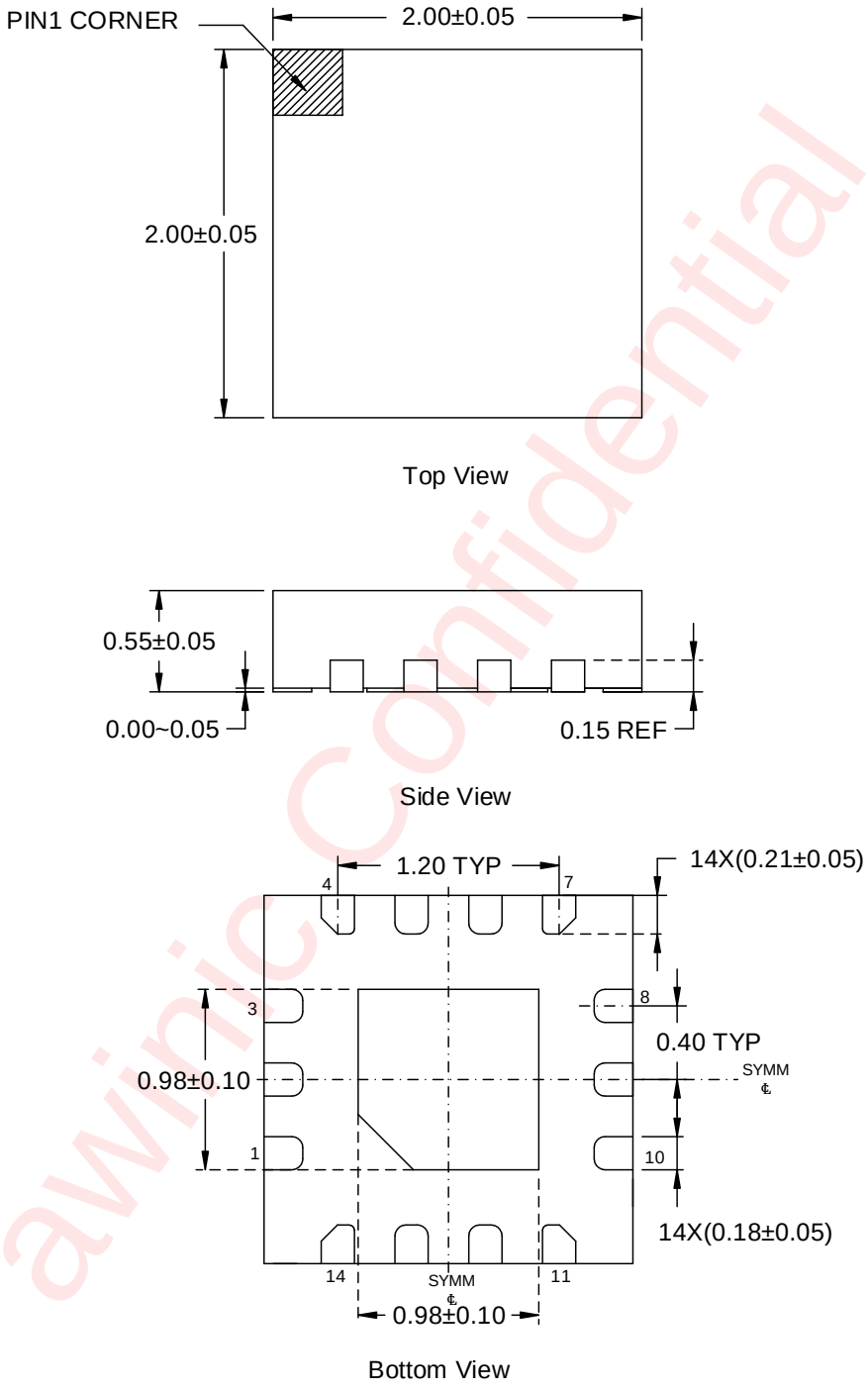
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	8.4	2.25	2.25	0.75	2	4	4	8	Q1

All dimensions are nominal

Figure 11 Tape and Reel

Package Description



Unit: mm

Figure 12 Package Outline

Land Pattern Data

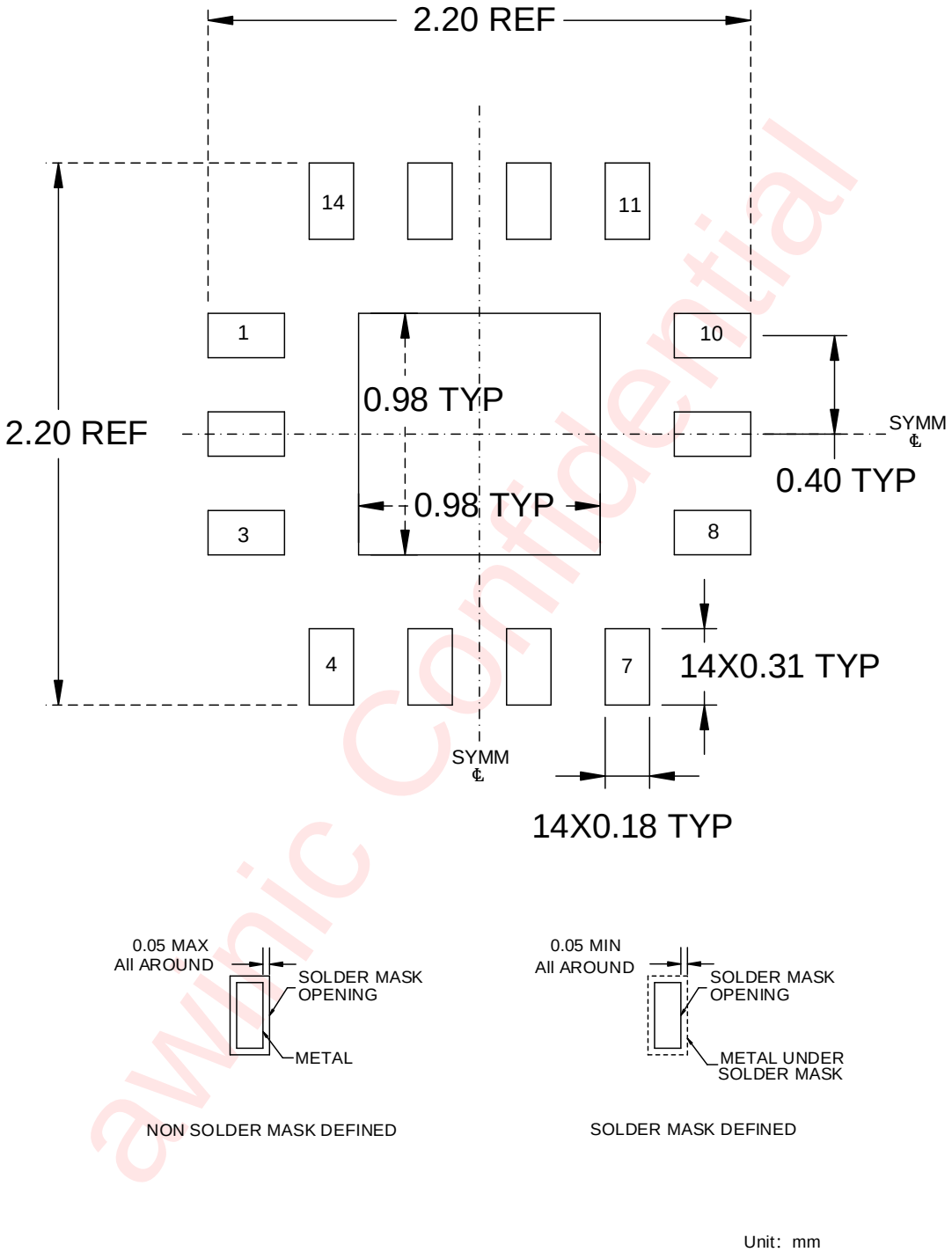


Figure 13 Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Nov. 2020	Officially Released
V1.1	Dec. 2020	Update power supply voltage range (P5)
V1.2	Jan. 2021	Change the spec of RL(P5)
V1.3	Apr. 2021	Change 2D register default value (P14)
V1.4	May 2021	Update power supply voltage range (P5)

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