10-bit DAC Uni-Directional VCM Auto-Focus Driver

Features

- Power Supply
  - 2.3V to 4.3V power supply
  - Support Power On Reset(POR)
  - Support Power Down(PD) mode
  - Support Thermal Shutdown(TSD)
- Built-In Digital-to-Analog Convertor
  - 10-bit resolution DAC
- Adjustable Maximum Output Current
  - Default current of 120mA/150mA
  - Optional current of 100mA/130mA, 150mA/180mA, 200mA/230mA
- Fast Settling Function
  - Support LSC(Linear Slope Control) mode
  - Support VRC(VCM Ringing Control) mode
  - Support VSC(VCM Shaping Control) mode
- 2-Wire I²C Serial Interface
  - 1.8V interface available
  - Fast-mode Plus(Fm+) compatible(1Mbit/s)
- Configurable Device Address
  - Default device address of 0x18(7-bit 0x0C)
  - Optional device address of 0x1A, 0x1C, 0x1E(7-bit 0x0D, 0x0E, 0x0F)
- Current Consumption
  - Power Down current less than 1μA
  - Quiescent current less than 0.5mA
- Package Dimension
  - Small 0.4mm pitch WLCSP 0.68mm x 1.08mm x 0.30mm -6B

General Description

The AW86017 is a uni-directional voice coil motor driver chip, which contains a 10-bit DAC. The operating voltage is from 2.3V to 4.3V. While the maximum output current is totally adjustable by register setting, the default value is 120mA.

The AW86017 is controlled through the I²C serial interface, and its operating frequency can reach up to 1MHz. The device address of the chip is default 0x18(7-bit 0x0C), and which can be changed by eNVM configuration.

The AW86017 contains Linear Slope Control mode and VCM Ringing Control mode etc. , which allows programmable configuration of output current waveform to minimize mechanical vibration for fast settling, and can be suitable for different types of voice coil motors.

The AW86017 contains power on reset circuit and power off function. The reset circuit ensures that the digital circuit works well when supply power up. The supply current consumption less than 1μA in Power Down mode.

The AW86017 can be used for auto focus applications in mobile cameras, digital still cameras, camcorders and action cameras etc. .

The AW86017 is available in a WLCSP 0.68mm x 1.08mm x 0.30mm -6B package.

Applications

- Mobile camera
- Digital still camera
- Camcorder
- Security camera
- Web camera
- Nano actuator

Pin Configuration And Top Mark

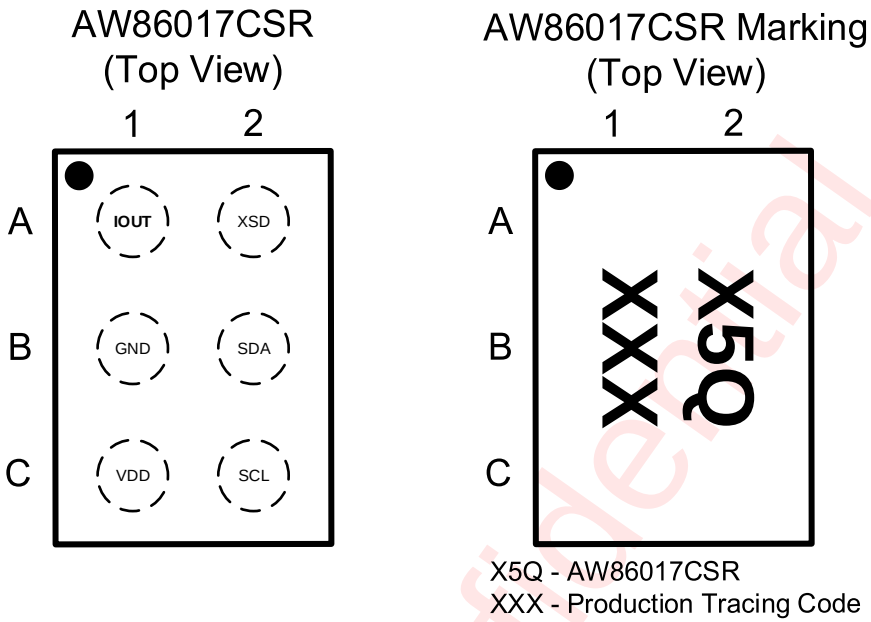


Figure 1 AW86017CSR Pin Configuration and Top Mark

Pin Definition

No.	Name	I/O	Description
A1	IOUT	out	Output current sink
A2	XSD	in	Shutdown mode (active low)
B1	GND	-	Ground
B2	SDA	inout	I^2C interface data input/output
C1	VDD	-	Supply Voltage
C2	SCL	in	I^2C interface clock input

Functional Block Diagram

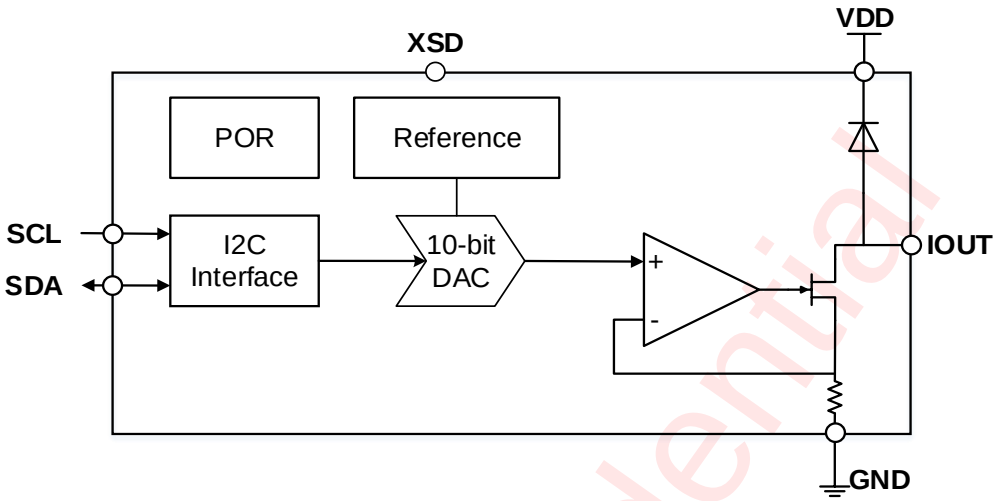


Figure 2 AW86017 Functional Block Diagram

Typical Application Circuits

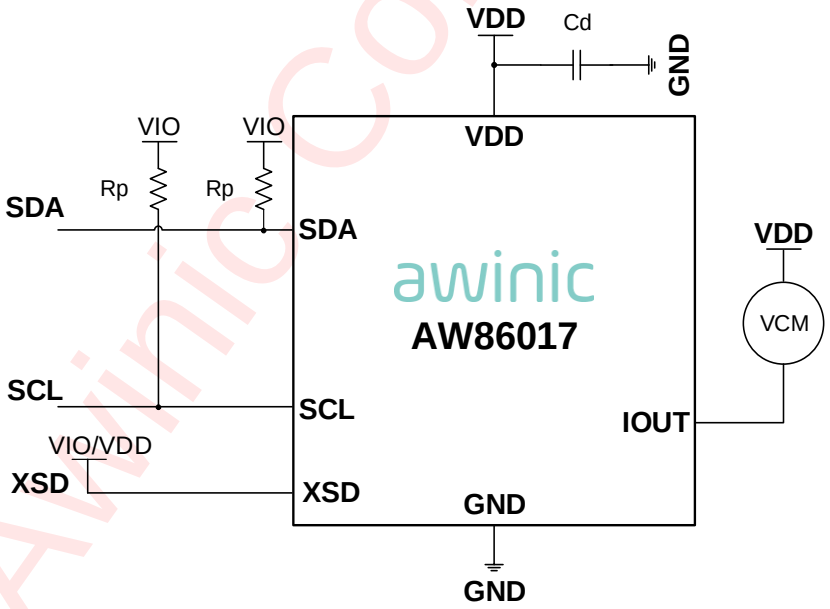


Figure 3 Typical Application Circuit of AW86017

Notice for Typical Application Circuits:

1. Power supply decoupling capacitor (Cd) should be placed as close to the VDD and GND as possible.
2. Pull-up Resistors (Rp) are necessary for IIC transmission.
3. XSD must be controlled by VIO, otherwise it can be connected to VDD.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86017CSR	-40℃～85℃	WLCSP 0.68mm x 1.08mm x 0.30mm -6B	X5Q	MSL1	RoHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE 1)

Parameters	Range
Supply voltage range V_{DD}	-0.3V to 5.5V
Control input voltage range V_{IN}	-0.3V to V_{DD}+0.3V
Operating free-air temperature range T_{OPR}	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature range T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	280°C
ESD(NOTE 2)	
Test standard(HBM): ESDA/JEDEC JS-001-2017	±2000V
Test standard(CDM): ESDA/JEDEC JS-002-2018	±1500V
Test standard(MM): JESD22-A115C	±400V
Latch-up	
Test standard: JESD78E	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power supply voltage	2.3		4.3	V
V_{IN}	Control input voltage	0		V_{DD}	V
f_{SCL}	Serial clock frequency		400	1000	kHz

Electrical Characteristics

V_{DD}=2.8V, V_{IO}=1.8V, T_A=25°C for typical values (unless otherwise noted)

Parameter		Test condition	Min	Typ	Max	Unit
Overall						
V_{DD}	Power supply voltage	On pin VDD	2.3	2.8	4.3	V
T_{TURNON}	Supply Turn On Time		0.05		3	ms
$T_{RESTART}$	Re-start Time		1			ms
T_{DELAY}	Turn On Delay				2	ms
I_{Qz}	Quiescent current	DAC=0		0.20		mA
I_Q	Quiescent current	DAC≠0		0.30		mA
I_{PD}	Power Down current	V_{DD}=2.8V		0.3		μA
t_{SET}(NOTE 3)	Setup waiting time			400		μs
Logic input / output（XSD）						
I_X	Input current		-1.0	2.8	5.0	μA
Logic input / output（SCL/SDA）						
I_S	Input current		-1.0	0.1	1.0	μA
V_{IL}	Logic input low level	SCL/SDA			0.5	V
V_{IH}	Logic input high level	SCL/SDA	1.3			V
t_G(NOTE 3)	Glitch rejection				20	ns
V_{OL}	SDA low level output voltage	SDA, I_{OL}=3mA			0.3	V
Driver						
I_{MAX0}(NOTE 4)	Maximum output current (IMAX=0)	IOUT=120mA	117	120	123	mA
		IOUT=150mA(NOTE 3)	145	150	155	
		IOUT=200mA(NOTE 3)	190	200	210	
		IOUT=100mA(NOTE 3)	97	100	103	
I_{MAX1}(NOTE 4)	Maximum output current (IMAX=1)	IOUT=120mA+30mA	147	150	153	mA
		IOUT=150mA +30mA(NOTE 3)	175	180	185	
		IOUT=200mA +30mA(NOTE 3)	220	230	240	
		IOUT=100mA +30mA(NOTE 3)	127	130	133	
I_{SD}	Shutdown current	XSD=0	-0.5	0.2	0.5	μA
Resolution	DAC resolution			10		Bits
R_{TOTAL}(NOTE 3)	Total output resistance	IOUT=120mA			1.5	Ω
INL(NOTE 3,5)	Integral Non-Linearity		-4		4	LSB
DNL(NOTE 3,5)	Differential Non-Linearity		-1		1	LSB

NOTE3: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

NOTE4: Maximum output current can be changed by register setting.

NOTE5: Linearity is guaranteed for 32code through 992code, while output current is at least 1LSB at 32code.

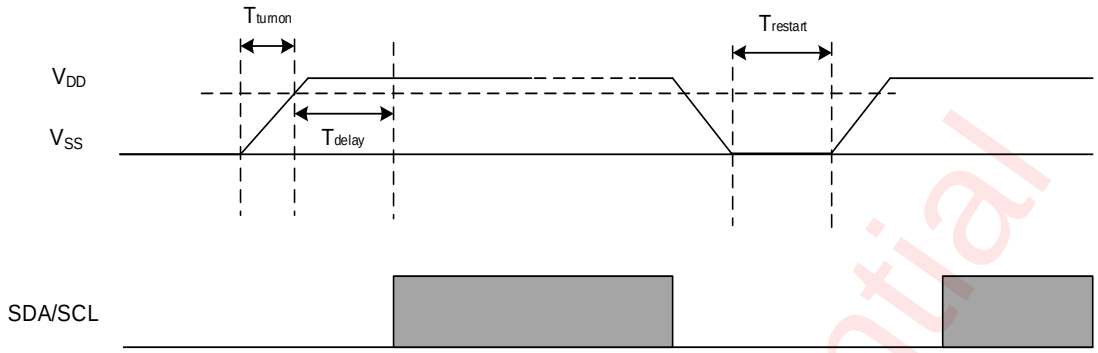


Figure 4 V_{DD} Supply And I2C Interface Timing

Detailed Functional Description

POWER UP SEQUENCE

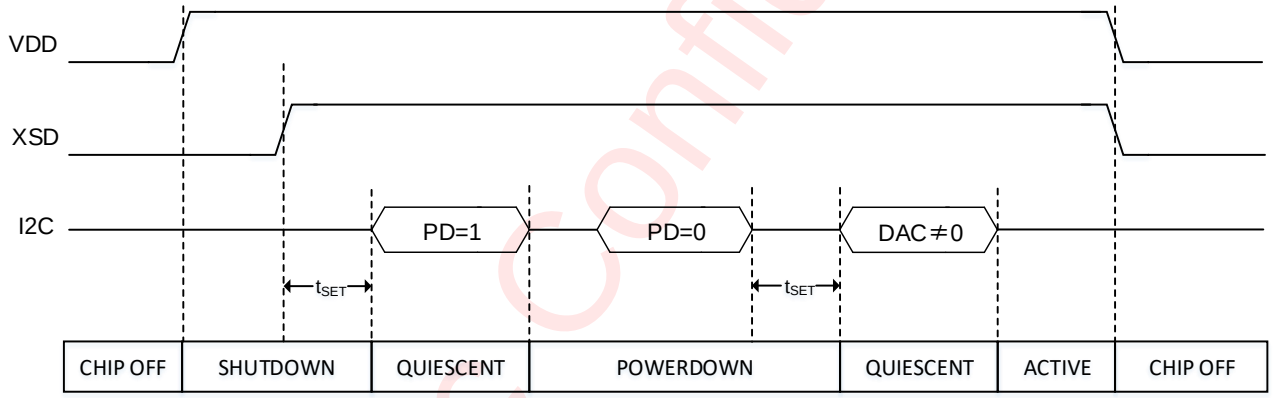


Figure 5 Power Up Sequence

The power on sequence of this device is illustrated in the above figure. Here are some considerations about XSD:

1. XSD must be controlled by VIO, otherwise it can be connected to VDD.
2. XSD must be controlled to “high” or “low” electrical level, means the floating state is forbidden.
3. Power Down (PD) mode should be operated after XSD rising.
4. Setup waiting time (t_{SET}) is needed after XSD rising or PD = “0”.

ADJUSTABLE MAXIMUM OUTPUT CURRENT

The maximum output current of the device is totally adjustable by register setting in Advanced Mode, the default value is 120mA. The device contains two separate built-in current gears, the register IMAX[5:4] – SEL_IMAX control the basic current gear, and the register IMAX[0] - IMAX is a switch of additional current gear.

SEL_IMAX[1:0]		IMAX	Basic Current	Additional Current	Total Maximum Output Current
0	0	0	120mA	0mA	120mA
0	1	0	150mA	0mA	150mA
1	0	0	200mA	0mA	200mA
1	1	0	100mA	0mA	100mA
0	0	1	120mA	30mA	150mA
0	1	1	150mA	30mA	180mA
1	0	1	200mA	30mA	230mA
1	1	1	100mA	30mA	130mA

OVER TEMPERATURE PROTECTION

The device has automatic temperature protection mechanism which prevents thermal damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default=150°C). The output stages will be disabled while Over Temperature Protection (OTP) happens, and will trigger to operate normally again when the junction temperature drops below the preset temperature low threshold (default=120°C). A status monitor is available in advanced mode register STATUS[4] – TSD, which means Thermal Shutdown (TSD).

FAST SETTLING FUNCTION

The device supports linear slope series control mode (includes LSC, VSC etc.) and voice coil motor ringing series control mode (includes DLC, VRC etc.), which allows programmable configuration of output current waveform to minimize mechanical vibration for fast settling function, and can be suitable for different types of voice coil motors. A status monitor is available in advanced mode register STATUS[0] – BUSY, it will automatic trigger to "1" when a control mode is excuting, and I^2C instruction will not respond during the "BUSY" status.

LSC & VSC SCHEME

In linear slope control (LSC) mode, the output current increase or decrease to the target in several same steps, the whole output current waveform appears as a first-order linear function, LSC mode is available both in normal mode and advanced mode. While in voice coil motor shaping control (VSC) mode, the output current increase or decrease to the target in several steps as well, but the whole output current waveform appears as a sine trigonometric function, VSC mode is only available in advanced mode.

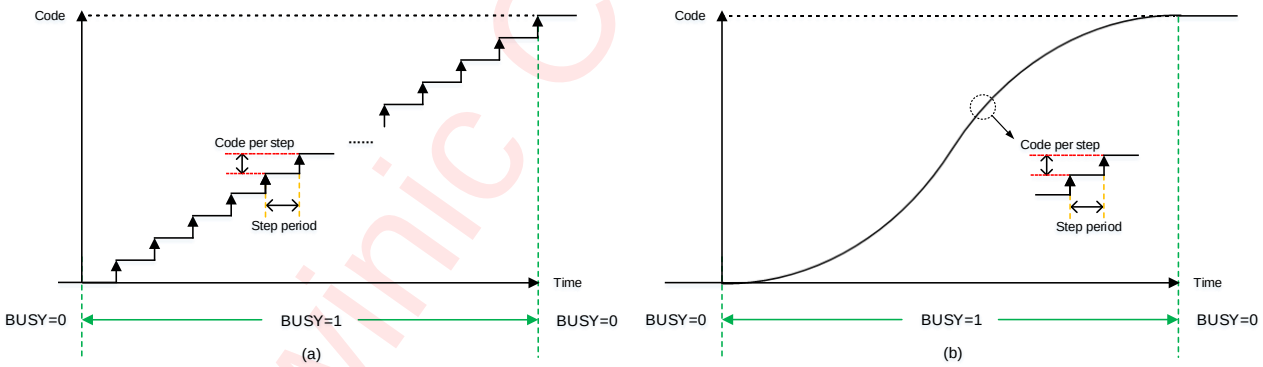


Figure 6 (a)LSC Scheme (b)VSC Scheme

DLC & VRC SCHEME

In Dual Level Control (DLC) mode, the output current increase or decrease to the target in two steps, DLC mode is available in normal mode, while you can use VRC2 in advanced mode to achieve the same effect. Voice coil motor ringing control (VRC) mode is a smart solution for reducing mechanical ringing and achieving very fast settling time, therefore it reduces autofocus response time and enhances image quality. VRC mode incorporates a wide band of tolerance around the vibration period of the VCM to compensate for manufacturing variability in the mechanical vibration period (T_{vib}) of VCM. The device offers different VRC modes whichc are trade-off operation time and tolerance. Customer can select the appropriate VRC mode to fit different specifications of voice coil motors.

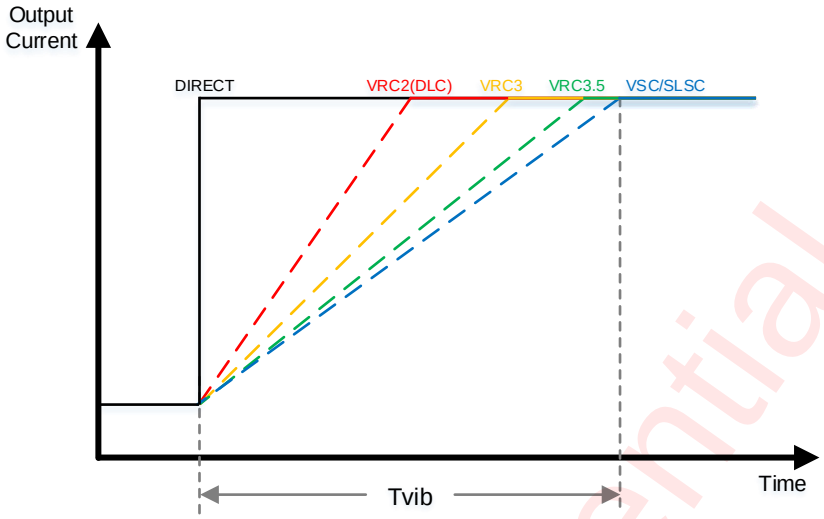


Figure 7 Control Mode Setting Time

Control Mode	Operation Time(NOTE 6)	Frequency Tolerance(NOTE 7)
DIRECT	-	-
VRC2(DLC)	T_{vib} x 0.5	±6%
VRC3	T_{vib} x 0.75	±16%
VRC3.5	T_{vib} x 0.93	±24%
SLSC	T_{vib} x 1.0	±31%
VSC	T_{vib} x 1.0	±34%

NOTE6: T_{vib} means the mechanical vibration period of voice coil motors.

NOTE7: Tolerance can be changed by mechanical characteristics of different voice coil motors.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in Fast-mode(Fm) at 400kHz and fast-mode plus(Fm+) at 1MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.6V) of this I²C interface.

DEVICE ADDRESS

The default device address of the chip is 0x18(7-bit 0x0C), and which can be changed by the factory, the other permitted I²C addresses are 0x1A, 0x1C, 0x1E(7-bit 0x0D, 0x0E, 0x0F).

DATA VALIDATION

When SCL is high level, SDA level must be stable. SDA can be changed only when SCL is low level.

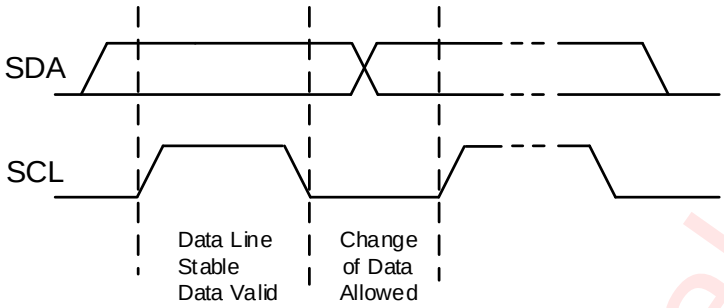


Figure 8 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

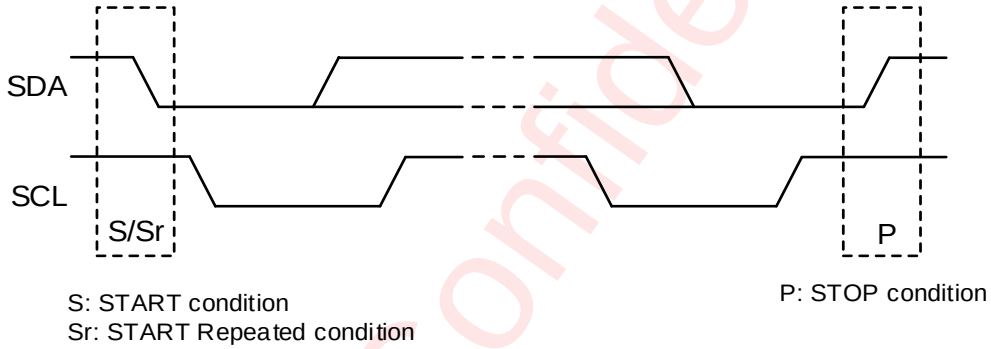


Figure 9 I²C Start/Stop Condition Timing

ACKNOWLEDGE(ACK)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

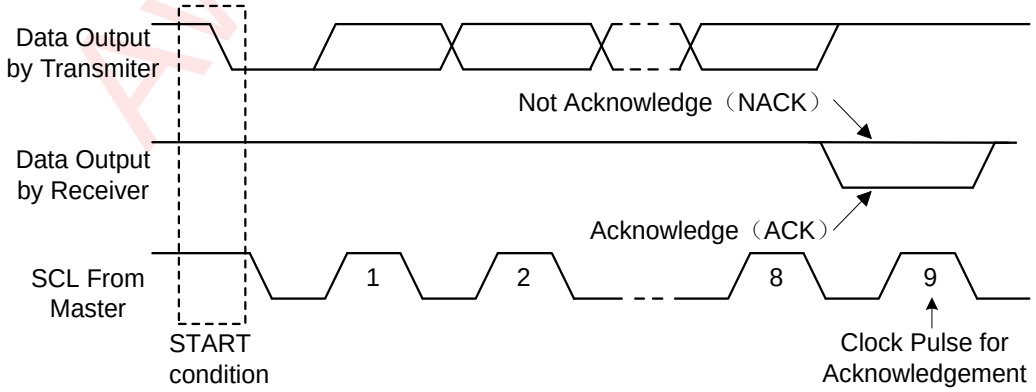


Figure 10 I²C ACK Timing

WRITE PROCESS

NORMAL MODE

The register address is not provided in Normal Mode, by using a 16-bits register data format. the transmission process in accordance with the following steps, as shown in the following figure.

1. Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.
2. Master device transmits the 7-bits device address of the slave device, and followed by the "read / write" flag ($R/\overline{W}$ = 0);
3. The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
4. The master device transmits the 8-bits write data to the first byte of register;
5. The slave device asserts an acknowledgment bit (ACK) to confirm whether the data byte 1 is sent successfully;
6. The master device transmits the 8-bits write data to the second byte of register;
7. The slave device asserts an acknowledgment bit (ACK) to confirm whether the data byte 2 is sent successfully;
8. The master device generates the STOP state to end the data transmission.

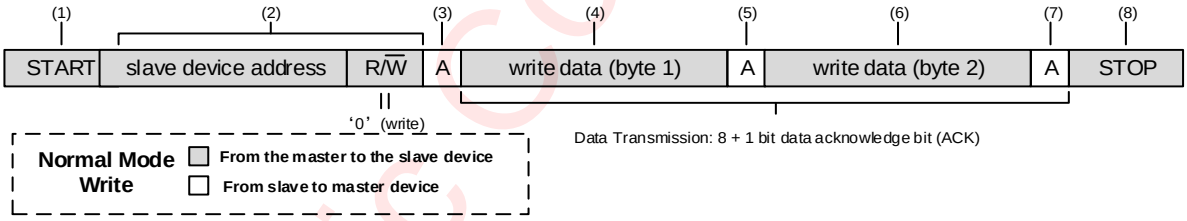


Figure 11 Normal Mode writing process

ADVANCED MODE

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledgment bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in the following figure.

1. Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.
2. Master device transmits the 7-bits device address of the slave device, and followed by the "read / write" flag ($R/\overline{W}$ = 0);
3. The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
4. The master device transmits the 8-bits register address to which the first data byte will written;
5. The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;
6. Master sends 8-bits of data to register which needs to be written;

7. The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;
8. If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6~7. In the latter case, the targeted register address will have been auto-incremented by the device.
9. The master device generates the STOP state to end the data transmission.

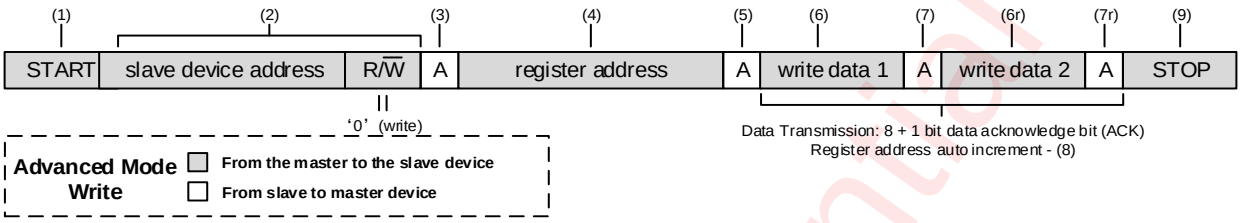


Figure 12 Advanced Mode writing process

READ PROCESS

NORMAL MODE

The register address is not provided in Normal Mode, by using a 16-bits register data format. The transmission process carried out by following steps listed in the following figure.

1. Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.
2. Master device transmits the 7-bits device address of the slave device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);
3. The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
4. Master transmits 8-bits read data to the first byte of register;
5. Continue to transmits the second byte of register, therefore it is no need for the slave to sends an acknowledgment bit (ACK) to confirm before ending the data transmission process;
6. Master transmits 8-bits read data to the second byte of register;
7. The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully, but no need for an acknowledgment bit (NOACK) in the second byte of data transmission process;
8. The master device generates the STOP state to end the data transmission.

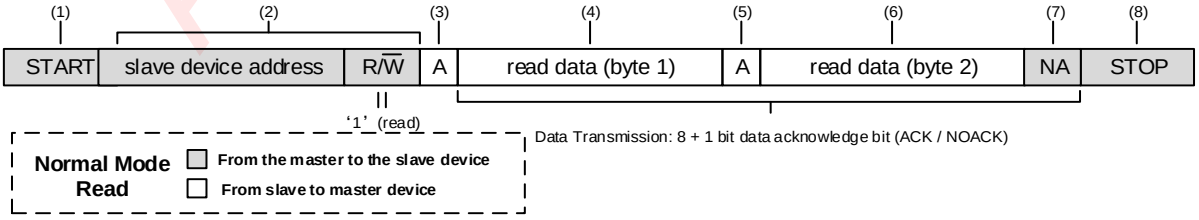


Figure 13 Normal Mode reading process

ADVANCED MODE

Reading process refers to the slave device reading data back to the master device. In this process, the

direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. As the slave device, the transmission process carried out by following steps listed in the following figure.

1. Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.
2. Master device transmits the 7-bits device address of the slave device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);
3. The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;
4. The master device transmits the register address to make sure where the first data byte will read;
5. The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
6. The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;
7. Master sends 7-bits address of the slave device and followed by a read / write flag ($R/\overline{W}$ = 1) again;
8. The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;
9. Master transmits 8-bits of data to register which needs to be read;
10. The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully, but no need for an acknowledgment bit (NOACK) in the last data transmission process;
11. The device automatically increment register address once after sent each acknowledgment bit (ACK);
12. The master device generates the STOP state to end the data transmission.

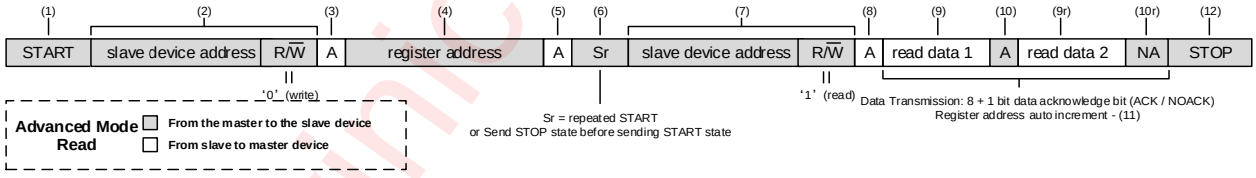


Figure 14 Advanced Mode reading process

I²C TIMING FEATURE

Parameter			Fast mode			Super-fast mode			Unit
No.	Symbol	Name	Min	Typ	Max	Min	Typ	Max	
1	f_{SCL}	SCL Clock frequency		400			1000		kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.3			μs
7	$t_{HD:STA}$	(repeat-start) start condition hold time	0.6			0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	Time between start and stop condition	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	0			0			ns

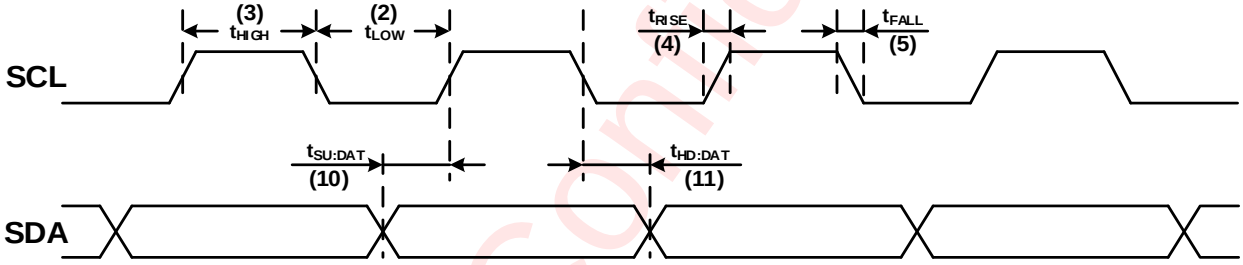


Figure 15 SCL and SDA timing relationships in the data transmission process

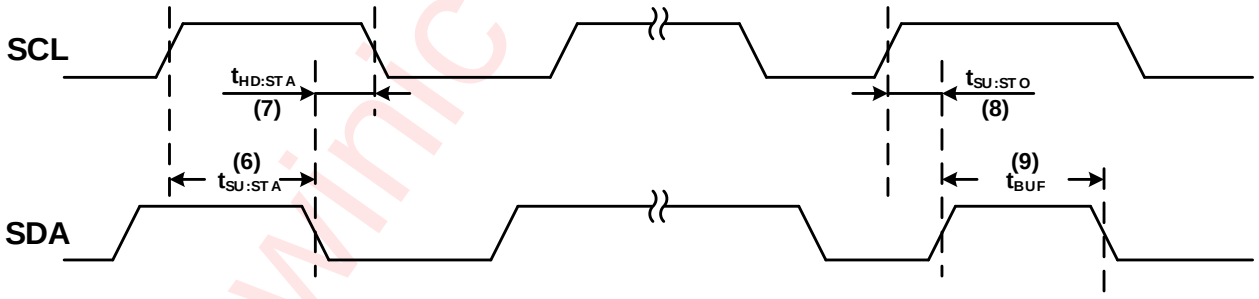


Figure 16 The timing relationship between START and STOP state

OPERATION MODE

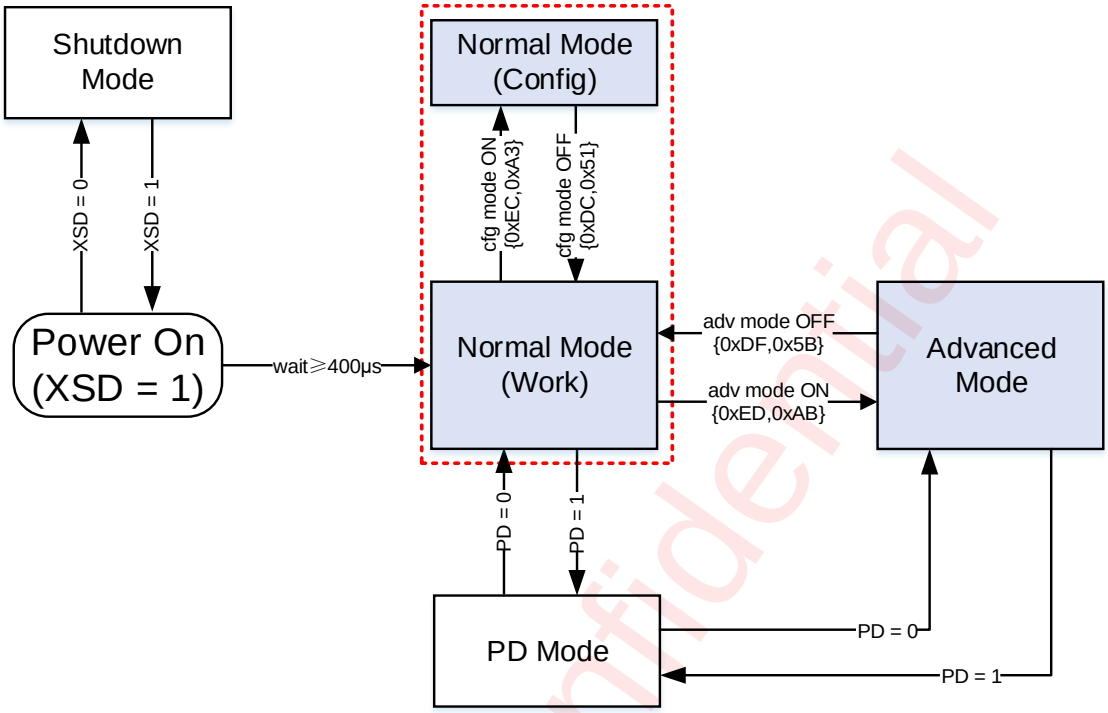


Figure 17 Operation Mode

SHUTDOWN MODE

The device switches to Shutdown Mode when the supply voltage is not ready or XSD pin is set to low. In this mode, all circuits inside this device will be shut down. I²C interface isn't accessible in this mode, and all of the internal configurable registers will be reset at next power on sequence (Power On Reset). The device will jump out of this mode when the supply voltages are prepared and XSD pin is set to high.

POWERDOWN MODE

The device switches to Powerdown Mode (PD Mode) by setting register PD = "1". In this mode, I²C interface is accessible, while almost all circuits inside are not work for low power consumption. The device will jump out of this mode when customer set register PD="0", and all of the internal configurable registers will be reset.

NORMAL MODE

The device switches to Normal Mode (Work) automatically after power on. In this mode, the device is fully operational. The register address is not provided in Normal Mode, by using a 16-bits register data format. Some normal fast settling control mode (LSC, DLC) are provided in this mode, customer can set the algorithm configuration in Normal Mode (Config).

ADVANCED MODE

Customer can set device to Advanced Mode by writing I²C instruction "0xED, 0xAB" in Normal Mode (Work). In this mode, the register address and 8-bits register data format is provided. Some advanced fast settling control mode (VRC, VSC, SLSC) are available, which can effectively reduces motor vibration time.

Register Configuration

NORMAL MODE

REGISTER LIST

The register address is not provided in Normal Mode, by using one more byte as register data, while the 16-bits register format of Normal Mode is shown as follows.

Byte	Bit	Symbol	R/W	Description	Default
1	7	PD	RW	Power Down mode 0: normal operation mode 1: power down mode (active high)	0x0
	6	FLAG	RW	FLAG bit must be check '0' before D[9:0] are written. During LSC or DLC operation, FLAG bit keeps '1'. While FLAG = '1', the I^2C command is ignored.	0x0
	5:0	D[9:0]	RW	Data input Output current = D[9:0] x (120mA / 1023)	0x00
2	7:4				0x0
	3:2	S[3:0]	RW	Codes per step 00: 0 codes per step(no SRC) - direct driving 01: 1 codes per step 10: 2 codes per step 11: 4 codes per step	0x0
	1:0		RW	Step period[unit: μs] Refer to "LSC time table"	0x0

SET UP METHOD

Driving mode – Direct, Linear Slope Control (LSC), Dual Level Control (DLC).

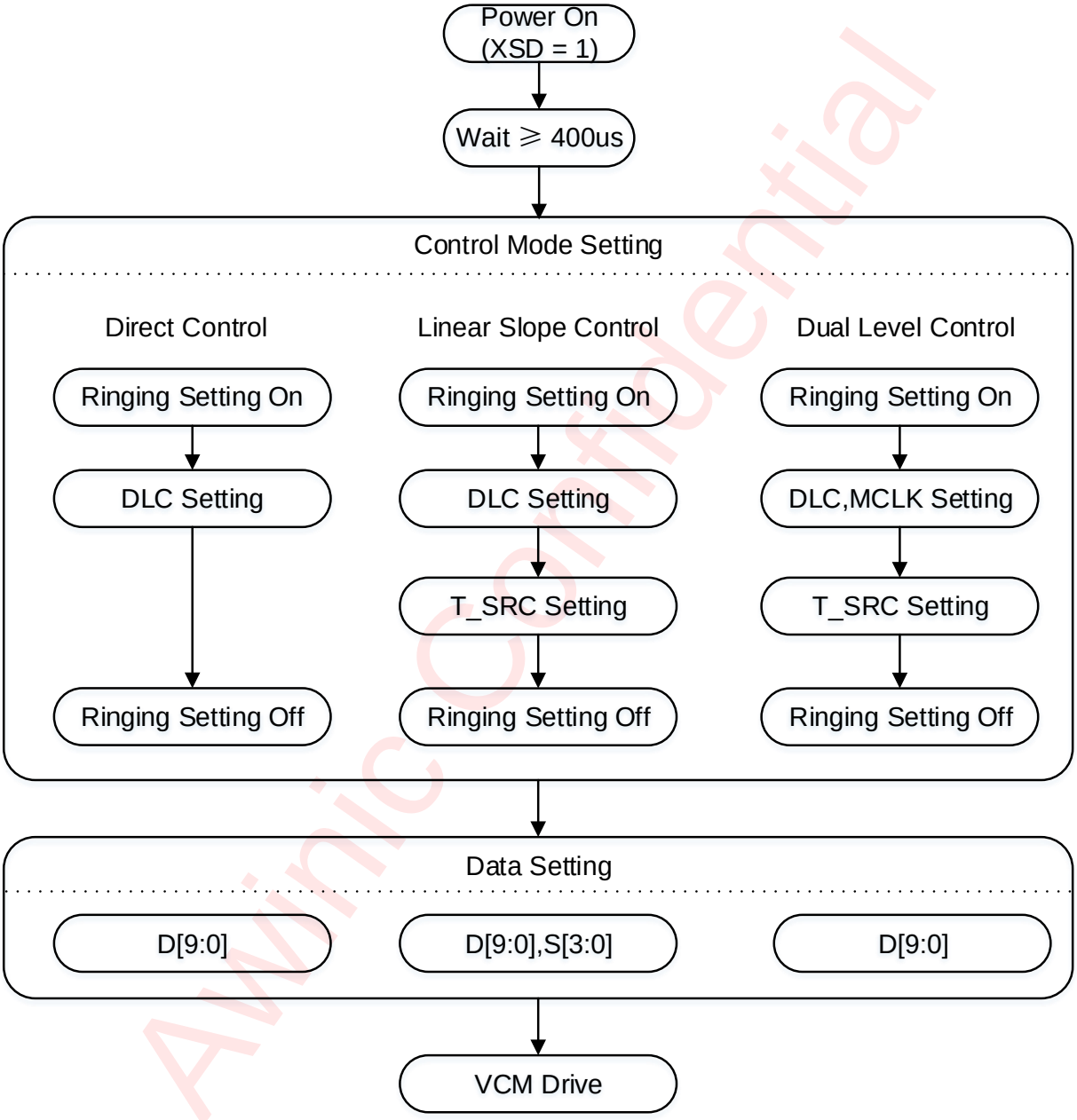


Figure 18 Normal Mode Set Up Method

DIRECT MODE SET UP METHOD(NOTE 8)

Ringing setting ON: Byte1(0xEC)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:0	RING_ON	RW	write 0xA3 to enter Control Mode Setting mode	0x0

Direct Driving setting: Byte1(0xA1)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:4	Reserved	RW	Not used	0x0
	3	DLC	RW	Dual level control mode 0: Direct and LSC 1: DLC mode	0x0
	2	Reserved	RW	Not used	0x1
	1:0	MCLK[1:0]	RW	MCLK[unit: ms] 00: x2(double) 01: x1(default) 10: x0.5(half) 11: x0.25(quarter) Refer to "DLC time table"	0x1

Ringing setting OFF: Byte1(0xDC)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:0	RING_OFF	RW	write 0x51 to exit Control Mode Setting mode ※During a Control Mode setting sequence, DAC command does not update.	0x0

D Setting					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
1	7	PD	RW	Power Down mode 0: normal operation mode 1: power down mode (active high)	0x0
	6	FLAG	RW	FLAG bit must be check '0' before D[9:0] are written. During LSC or DLC operation, FLAG bit keeps '1'. While FLAG = '1', the I^2C command is ignored.	0x0
	5:0	D[9:0]	RW	Data input Output current = D[9:0] x (120mA / 1023)	0x00
2	7:4				0x0
	3:2	S[3:0]	RW	Codes per step 00: 0 codes per step(no SRC) - direct driving 01: 1 codes per step 10: 2 codes per step 11: 4 codes per step	0x0
	1:0		RW	Step period[unit: μs] Refer to "LSC time table"	0x0

NOTE8: Direct Mode can be used for testing VCM vibration period(T_{vib}).

LSC MODE SET UP METHOD

Ringing setting ON: Byte1(0xEC)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:0	RING_ON	RW	write 0xA3 to enter Control Mode Setting mode	0x0

LSC Mode setting: Byte1(0xA1)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:4	Reserved	RW	Not used	0x0
	3	DLC	RW	Dual level control mode 0: Direct and LSC 1: DLC mode	0x0
	2	Reserved	RW	Not used	0x1
	1:0	MCLK[1:0]	RW	MCLK[unit: ms] 00: x2(double) 01: x1(default) 10: x0.5(half) 11: x0.25(quarter) Refer to "DLC time table"	0x1

T_SRC setting: Byte1(0xF2)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:3	T_SRC[4:0]	RW	Slew Rate Control time table index Refer to "LSC time table"	0x00
	2:0	Reserved	RW	Not used	0x0

Ringing setting OFF: Byte1(0xDC)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:0	RING_OFF	RW	write 0x51 to exit Control Mode Setting mode ※During a SRC setting sequence, DAC command does not update.	0x0

D and S Setting					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
1	7	PD	RW	Power Down mode 0: normal operation mode 1: power down mode (active high)	0x0
	6	FLAG	RW	FLAG bit must be check '0' before D[9:0] are written. During LSC or DLC operation, FLAG bit keeps '1'. While FLAG = '1', the I^2C command is ignored.	0x0
	5:0	D[9:0]	RW	Data input Output current = D[9:0] x (120mA / 1023)	0x00
2	7:4				0x0
	3:2	S[3:0]	RW	Codes per step 00: 0 codes per step(no SRC) - direct driving 01: 1 codes per step 10: 2 codes per step 11: 4 codes per step	0x0
	1:0		RW	Step period[unit: μs] Refer to "LSC time table"	0x0

LSC time table：

LSC step period is set by S[1:0] and T_SRC[4:0].

1 Step period (Unit:[μs])				
T_SRC[4:0]	S[1:0]			
	00	01	10	11
10000	136.0	272.0	544.0	1088.0
10001	130.0	260.0	520.0	1040.0
10010	125.0	250.0	500.0	1000.0
10011	120.0	240.0	480.0	960.0
10100	116.0	232.0	464.0	928.0
10101	112.0	224.0	448.0	896.0
10110	108.0	216.0	432.0	864.0
10111	104.0	208.0	416.0	832.0
11000	101.0	202.0	404.0	808.0
11001	98.0	196.0	392.0	784.0
11010	95.0	190.0	380.0	760.0
11011	92.0	184.0	368.0	736.0
11100	89.0	178.0	356.0	712.0
11101	87.0	174.0	348.0	696.0
11110	85.0	170.0	340.0	680.0
11111	83.0	166.0	332.0	664.0
00000	81.0	162.0	324.0	648.0
00001	79.0	158.0	316.0	632.0
00010	77.5	155.0	310.0	620.0
00011	76.0	152.0	304.0	608.0
00100	74.5	149.0	298.0	596.0
00101	73.0	146.0	292.0	584.0
00110	71.5	143.0	286.0	572.0
00111	70.0	140.0	280.0	560.0
01000	69.0	138.0	276.0	552.0
01001	68.0	136.0	272.0	544.0
01010	67.0	134.0	268.0	536.0
01011	66.0	132.0	264.0	528.0
01100	65.5	131.0	262.0	524.0
01101	65.0	130.0	260.0	520.0
01110	64.5	129.0	258.0	516.0
01111	64.0	128.0	256.0	512.0

DLC MODE SET UP METHOD

Ringing setting ON: Byte1(0xEC)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:0	RING_ON	RW	write 0xA3 to enter Control Mode Setting mode	0x0

DLC Mode and MCLK setting: Byte1(0xA1)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:4	Reserved	RW	Not used	0x0
	3	DLC	RW	Dual level control mode 0: Direct and LSC 1: DLC mode	0x0
	2	Reserved	RW	Not used	0x1
	1:0	MCLK[1:0]	RW	MCLK[unit: ms] 00: x2(double) 01: x1(default) 10: x0.5(half) 11: x0.25(quarter) Refer to "DLC time table"	0x1

T_SRC setting: Byte1(0xF2)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:3	T_SRC[4:0]	RW	Slew Rate Control time table index Refer to "DLC time table"	0x00
	2:0	Reserved	RW	Not used	0x0

Ringing setting OFF: Byte1(0xDC)					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
2	7:0	RING_OFF	RW	write 0x51 to exit Control Mode Setting mode ※During a SRC setting sequence, DAC command does not update.	0x0

D Setting					
Byte	**Bit**	**Symbol**	**R/W**	**Description**	**Default**
1	7	PD	RW	Power Down mode 0: normal operation mode 1: power down mode (active high)	0x0
	6	FLAG	RW	FLAG bit must be check '0' before D[9:0] are written. During LSC or DLC operation, FLAG bit keeps '1'. While FLAG = '1', the I^2C command is ignored.	0x0
	5:0	D[9:0]	RW	Data input Output current = D[9:0] x (120mA / 1023)	0x00
2	7:4				0x0
	3:2	S[3:0]	RW	Codes per step 00: 0 codes per step(no SRC) - direct driving 01: 1 codes per step 10: 2 codes per step 11: 4 codes per step	0x0
	1:0		RW	Step period[unit: μs] Refer to "LSC time table"	0x0

DLC time table：

DLC step period is set by MCLK[1:0] and T_SRC[4:0], the default value is $T_{vib}/2$.

$T_{vib}/2$ (Unit:[ms])				
T_SRC[4:0]	MCLK[1:0]			
	00	01	10	11
10000	21.25	10.63	5.31	2.66
10001	20.31	10.16	5.08	2.54
10010	19.53	9.77	4.88	2.44
10011	18.75	9.38	4.69	2.34
10100	18.13	9.06	4.53	2.27
10101	17.50	8.75	4.38	2.19
10110	16.88	8.44	4.22	2.11
10111	16.25	8.13	4.06	2.03
11000	15.78	7.89	3.95	1.97
11001	15.31	7.66	3.83	1.91
11010	14.84	7.42	3.71	1.86
11011	14.38	7.19	3.59	1.80
11100	13.91	6.95	3.48	1.74
11101	13.59	6.80	3.40	1.70
11110	13.28	6.64	3.32	1.66
11111	12.97	6.48	3.24	1.62
00000	12.66	6.33	3.16	1.58
00001	12.34	6.17	3.09	1.54
00010	12.11	6.05	3.03	1.51
00011	11.88	5.94	2.97	1.48
00100	11.64	5.82	2.91	1.46
00101	11.41	5.70	2.85	1.43
00110	11.17	5.59	2.79	1.40
00111	10.94	5.47	2.73	1.37
01000	10.78	5.39	2.70	1.35
01001	10.63	5.31	2.66	1.33
01010	10.47	5.23	2.62	1.31
01011	10.31	5.16	2.58	1.29
01100	10.23	5.12	2.56	1.28
01101	10.16	5.08	2.54	1.27
01110	10.08	5.04	2.52	1.26
01111	10.00	5.00	2.50	1.25

ADVANCED MODE

The device has an advanced mode. It enters its advanced mode by writing 0xED, 0xAB sequentially. The VRC mode adjusts the amplitude and timing of the output current to meet the requirements. When it is in its advanced mode, it can be back to its normal mode by writing 0xDF, 0x5B sequentially.

The device supports LSC, SLSC, VRC, VSC control mode in its advanced mode, which can effectively reduces motor vibration time. The different control modes adapt to the VCM of different manufacturers.

REGISTER LIST

Addr	Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	IC_INFO	RO	IC_MANU_ID				IC_MODEL				0x03
0x01	IC_VER	RO					IC_VER				0x01
0x02	CTRL	RW								PD	0x00
0x03	CODE_H	RW							CODE_H		0x00
0x04	CODE_L	RW	CODE_L								0x00
0x05	STATUS	RO			XSD	TSD			DONE	BUSY	0x00
0x06	MODE	RW	RING				RING_MODE				0x00
0x07	DIV	RW							DIV		0x00
0x08	VRCT	RW		VRCT							0x00
0x09	PRESET	RW	PRESET								0x00
0x0A	NRC	RW							NRC_EN	NRC_MD	0x00
0x10	IMAX	RW			SEL_IMAX					IMAX	0x00

RO: Read Only

RW: Read and Write available

SET UP METHOD

Here gives some examples of set up sequence, more details please refer to “Register Detailed Description”.

The IIC Device Address of the device is default 0x18(7-bit 0x0C), and other options are available: 0x1A, 0x1C, 0x1E(7-bit 0x0D, 0x0E, 0x0F).

Control Mode	Operate Seq.	Device Addr.	Register Addr.	Register Data	Description
Power Down	1	0x18	0xED	0xAB	Enter Advanced Mode
	2	0x18	0x02	0x01	Enter Power Down Mode
Direct	1	0x18	0xED	0xAB	Enter Advanced Mode
	2	0x18	0x06	0x00	Set Direct Mode
	3	0x18	0x03,0x04	CODE[9:0]	VCM Drive
VRC-3	1	0x18	0xED	0xAB	Enter Advanced Mode
	2	0x18	0x06	0x84	Set VRC-3 Mode
	3	0x18	0x07	DIV[1:0]	Set Period Divider
	4	0x18	0x08	VRCT[6:0]	Set Time Step
	5	0x18	0x03,0x04	CODE[9:0]	VCM Drive

REGISTER DETAILED DESCRIPTION

IC_INFO: Address(0x00)

Bit	Symbol	R/W	Description	Default
7:4	IC_MANU_ID	RO	IC Manufacturer ID	0x0
3:0	IC_MODEL	RO	IC Model	0x3

IC_VER: Address(0x01)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RO	Not used	0
3:0	IC_VER	RO	IC Version	0x1

CTRL: Address(0x02)

Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Not used	0
0	PD	RW	Soft Reset (PD Mode) 0: Work(Realease Soft Shutdown) 1: Soft Shutdown, enter PD Mode	0x0

CODE_H: Address(0x03)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:2	Reserved	RW	Not used	0
1:0	CODE_H	RW	10-bit DAC Code bit8~bit9 Output current = CODE[9:0] x (120mA / 1023) [mA]	0x0

CODE_L: Address(0x04)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	CODE_L	RW	10bit DAC Code bit0~bit7 (trig byte) Output current = CODE[9:0] x (120mA / 1023) [mA] DAC output is updated when address 0x04 is written.	0x00

STATUS: Address(0x05)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5	XSD	RO	Conventional Mode Hard Reset 0: Hardware Shutdown 1: Work	0x0
4	TSD	RO	Thermal Shutdown State Monitor (Over Temperature Protect Flag) 0: Work 1: Thermal Shutdown	0x0
3:2	Reserved	RO	Not used	0
1	DONE	RO	Power On Initialization Done Signal 0: Unprepared 1: Initialization done	0x0
0	BUSY	RO	Indicate the chip is busying generate wave. BUSY bit should be ”L” when ”CODE_H and CODE_L” registers are written. During ringing control operation, the BUSY bit is ”H” and the I^2C write commands to registers except PD bit of CTRL(0x02) are ignored.	0x0

MODE: Address(0x06)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	RING	RW	Ringing Control Enable 0: Direct mode 1: Ringing control(VRC, LSC, SLSC, VSC)	0x0
6:4	Reserved	RW	Not used	0
3:0	RING_MODE	RW	Control Mode Selection RING / RING_MODE / Control Mode / VRC Operation Time 0 / X / Direct 1 / 0000 / VRC2 / T_{vib} x 0.5 1 / 0100 / VRC3 / T_{vib} x 0.75 1 / 1000 / VRC3.5 / T_{vib} x 0.93 1 / 0110 / LSC1 / N/A 1 / 1010 / LSC2 / N/A 1 / 1110 / LSC4 / N/A 1 / 1111 / LSC8 / N/A 1 / 0011 / SLSC / T_{vib} x 1.0 1 / 0001 / VSC / T_{vib} x 1.0 1 / else / Reserved	0x0

DIV: Address(0x07)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:2	Reserved	RW	Not used	0
1:0	DIV	RW	Time Step Scaling Factor (Period Divider) 2'b00: 1x 2'b01: 2x 2'b10: 4x 2'b11: 8x	0x0

VRCT: Address(0x08)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0
6:0	VRCT	RW	Time Step Setting LSC Step Time = (63.5us + VRCT[6:0] / 2 us) x DIV[1:0] (range: 63.5us~1016us) VRC Setting Time = Tvib = (3.81ms + VRCT[6:0] x 0.03ms) x DIV[1:0] (range: 3.81ms~60.96ms) More details refer to "VRC time table"	0x00

PRESET: Address(0x09)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:0	PRESET	RW	Noise Reduce Control Algorithm Code Pre-Setting CODE_H <= { 7'b0, PRESET[7] } ; CODE_L <= { PRESET[6:0], 1'b0 } ; ex) PRESET[7:0] = b'1111 1111('hFF) is DAC Code for preset = b'01 1111 1110('h1FE)	0x00

NRC: Address(0x0A)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:3	Reserved	RW	Not used	0
2	NRC_EN	RW	Noise Reduce Control Algorithm Enable 0: NRC Disable 1: NRC Enable	0x0
1:0	NRC_MD	RW	Noise Reduce Control Algorithm Setting 0: NRC Start 1: NRC Landing	0x0

IMAX: Address(0x10)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RW	Not used	0
5:4	SEL_IMAX	RW	Maximum Output Current Gear Control 2'b00: 120mA (default) 2'b01: 150mA 2'b10: 200mA 2'b11: 100mA	0x0
3:1	Reserved	RW	Not used	0
0	IMAX	RW	Maximum Output Current Additional Gear Enable 0: 120mA(default) 1: 120mA(default)+30mA = 150mA	0x0

VRC time table：

VRC setting time is set by VRCT[6:0] and DIV[1:0], which are related to T_{vib}.

Tvib (Unit:[ms])				
VRCT[6:0]	DIV[1:0]			
	00	01	10	11
000 0000	3.81	7.62	15.24	30.48
000 0001	3.84	7.68	15.36	30.72
000 0010	3.87	7.74	15.48	30.96
000 0011	3.90	7.80	15.60	31.20
000 0100	3.93	7.86	15.72	31.44
000 0101	3.96	7.92	15.84	31.68
000 0110	3.99	7.98	15.96	31.92
000 0111	4.02	8.04	16.08	32.16
000 1000	4.05	8.10	16.20	32.40
000 1001	4.08	8.16	16.32	32.64
000 1010	4.11	8.22	16.44	32.88
000 1011	4.14	8.28	16.56	33.12
000 1100	4.17	8.34	16.68	33.36
000 1101	4.20	8.40	16.80	33.60
000 1110	4.23	8.46	16.92	33.84
000 1111	4.26	8.52	17.04	34.08
001 0000	4.29	8.58	17.16	34.32
001 0001	4.32	8.64	17.28	34.56
001 0010	4.35	8.70	17.40	34.80
001 0011	4.38	8.76	17.52	35.04
001 0100	4.41	8.82	17.64	35.28
001 0101	4.44	8.88	17.76	35.52
001 0110	4.47	8.94	17.88	35.76
001 0111	4.50	9.00	18.00	36.00
001 1000	4.53	9.06	18.12	36.24
001 1001	4.56	9.12	18.24	36.48
001 1010	4.59	9.18	18.36	36.72
001 1011	4.62	9.24	18.48	36.96
001 1100	4.65	9.30	18.60	37.20
001 1101	4.68	9.36	18.72	37.44
001 1110	4.71	9.42	18.84	37.68
001 1111	4.74	9.48	18.96	37.92

(Next Page Continued)

Tvib (Unit:[ms])				
VRCT[6:0]	DIV[1:0]			
	00	01	10	11
010 0000	4.77	9.54	19.08	38.16
010 0001	4.80	9.60	19.20	38.40
010 0010	4.83	9.66	19.32	38.64
010 0011	4.86	9.72	19.44	38.88
010 0100	4.89	9.78	19.56	39.12
010 0101	4.92	9.84	19.68	39.36
010 0110	4.95	9.90	19.80	39.60
010 0111	4.98	9.96	19.92	39.84
010 1000	5.01	10.02	20.04	40.08
010 1001	5.04	10.08	20.16	40.32
010 1010	5.07	10.14	20.28	40.56
010 1011	5.10	10.20	20.40	40.80
010 1100	5.13	10.26	20.52	41.04
010 1101	5.16	10.32	20.64	41.28
010 1110	5.19	10.38	20.76	41.52
010 1111	5.22	10.44	20.88	41.76
011 0000	5.25	10.50	21.00	42.00
011 0001	5.28	10.56	21.12	42.24
011 0010	5.31	10.62	21.24	42.48
011 0011	5.34	10.68	21.36	42.72
011 0100	5.37	10.74	21.48	42.96
011 0101	5.40	10.80	21.60	43.20
011 0110	5.43	10.86	21.72	43.44
011 0111	5.46	10.92	21.84	43.68
011 1000	5.49	10.98	21.96	43.92
011 1001	5.52	11.04	22.08	44.16
011 1010	5.55	11.10	22.20	44.40
011 1011	5.58	11.16	22.32	44.64
011 1100	5.61	11.22	22.44	44.88
011 1101	5.64	11.28	22.56	45.12
011 1110	5.67	11.34	22.68	45.36
011 1111	5.70	11.40	22.80	45.60

(Next Page Continued)

Tvib (Unit:[ms])				
VRCT[6:0]	DIV[1:0]			
	00	01	10	11
100 0000	5.73	11.46	22.92	45.84
100 0001	5.76	11.52	23.04	46.08
100 0010	5.79	11.58	23.16	46.32
100 0011	5.82	11.64	23.28	46.56
100 0100	5.85	11.70	23.40	46.80
100 0101	5.88	11.76	23.52	47.04
100 0110	5.91	11.82	23.64	47.28
100 0111	5.94	11.88	23.76	47.52
100 1000	5.97	11.94	23.88	47.76
100 1001	6.00	12.00	24.00	48.00
100 1010	6.03	12.06	24.12	48.24
100 1011	6.06	12.12	24.24	48.48
100 1100	6.09	12.18	24.36	48.72
100 1101	6.12	12.24	24.48	48.96
100 1110	6.15	12.30	24.60	49.20
100 1111	6.18	12.36	24.72	49.44
101 0000	6.21	12.42	24.84	49.68
101 0001	6.24	12.48	24.96	49.92
101 0010	6.27	12.54	25.08	50.16
101 0011	6.30	12.60	25.20	50.40
101 0100	6.33	12.66	25.32	50.64
101 0101	6.36	12.72	25.44	50.88
101 0110	6.39	12.78	25.56	51.12
101 0111	6.42	12.84	25.68	51.36
101 1000	6.45	12.90	25.80	51.60
101 1001	6.48	12.96	25.92	51.84
101 1010	6.51	13.02	26.04	52.08
101 1011	6.54	13.08	26.16	52.32
101 1100	6.57	13.14	26.28	52.56
101 1101	6.60	13.20	26.40	52.80
101 1110	6.63	13.26	26.52	53.04
101 1111	6.66	13.32	26.64	53.28

(Next Page Continued)

Tvib (Unit:[ms])				
VRCT[6:0]	DIV[1:0]			
	00	01	10	11
110 0000	6.69	13.38	26.76	53.52
110 0001	6.72	13.44	26.88	53.76
110 0010	6.75	13.50	27.00	54.00
110 0011	6.78	13.56	27.12	54.24
110 0100	6.81	13.62	27.24	54.48
110 0101	6.84	13.68	27.36	54.72
110 0110	6.87	13.74	27.48	54.96
110 0111	6.90	13.80	27.60	55.20
110 1000	6.93	13.86	27.72	55.44
110 1001	6.96	13.92	27.84	55.68
110 1010	6.99	13.98	27.96	55.92
110 1011	7.02	14.04	28.08	56.16
110 1100	7.05	14.10	28.20	56.40
110 1101	7.08	14.16	28.32	56.64
110 1110	7.11	14.22	28.44	56.88
110 1111	7.14	14.28	28.56	57.12
111 0000	7.17	14.34	28.68	57.36
111 0001	7.20	14.40	28.80	57.60
111 0010	7.23	14.46	28.92	57.84
111 0011	7.26	14.52	29.04	58.08
111 0100	7.29	14.58	29.16	58.32
111 0101	7.32	14.64	29.28	58.56
111 0110	7.35	14.70	29.40	58.80
111 0111	7.38	14.76	29.52	59.04
111 1000	7.41	14.82	29.64	59.28
111 1001	7.44	14.88	29.76	59.52
111 1010	7.47	14.94	29.88	59.76
111 1011	7.50	15.00	30.00	60.00
111 1100	7.53	15.06	30.12	60.24
111 1101	7.56	15.12	30.24	60.48
111 1110	7.59	15.18	30.36	60.72
111 1111	7.62	15.24	30.48	60.96

Application Information

CAPACITOR SELECTION

Recommend decoupling capacitor (Cd) value is at least 1μF.

RESISTOR SELECTION

Recommend pull-up resistor (Rp) value is 1kΩ@f_{SCL}=1000kHz or 4.7kΩ@f_{SCL}=400kHz.

PCB Layout Consideration

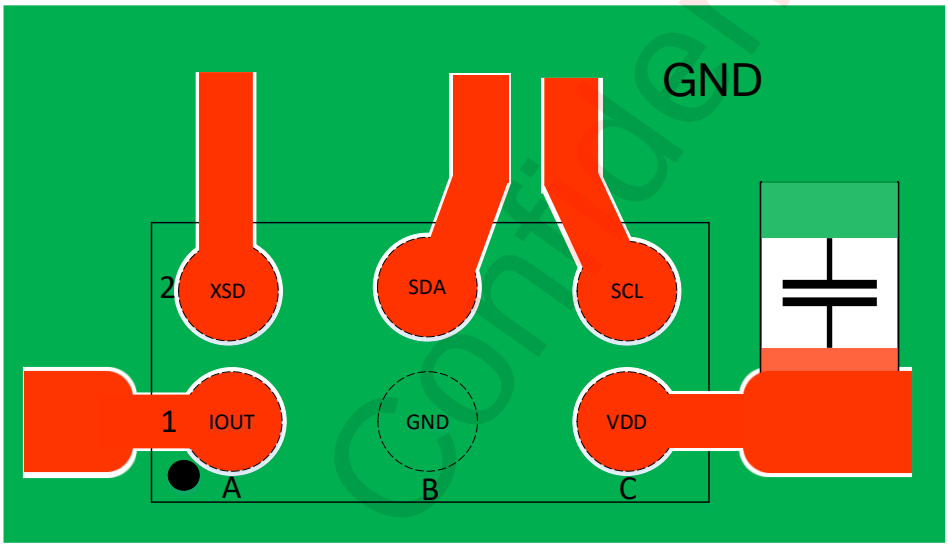


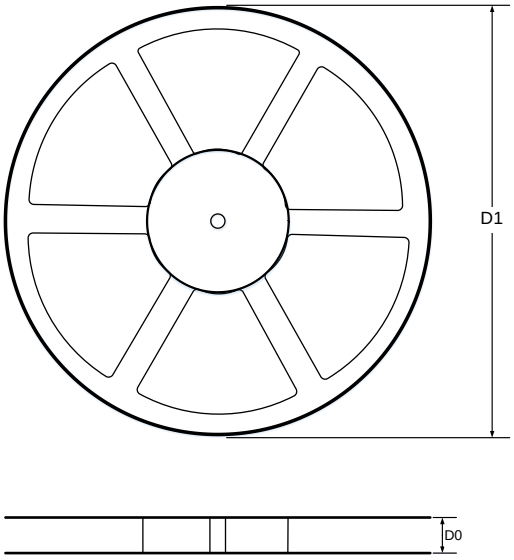
Figure 19 AW86017 PCB Layout Placement

To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

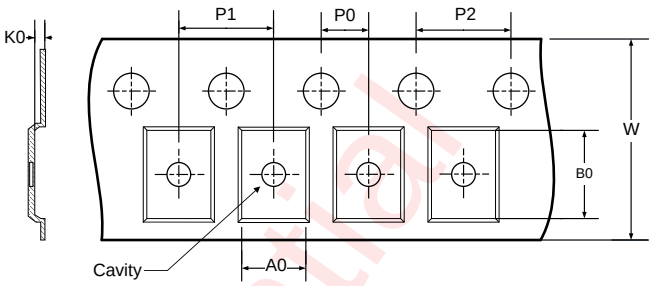
1. The decoupling capacitor Cd should be placed close to the chip VDD and GND on the same layer as the chip to ensure the best filtering effect.
2. I^2C bus should be surrounded by GND as mush as possible.
3. VDD,IOUT should be routed as thick as possible after exiting from the pad to meet the overcurrent capability; VDD,IOUT must be routed to meet at least 250mA of current.

Tape And Reel Information

REEL DIMENSIONS

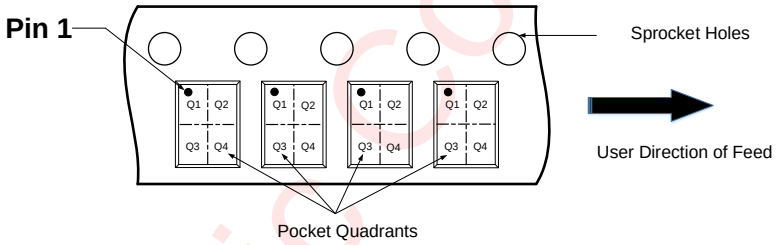


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



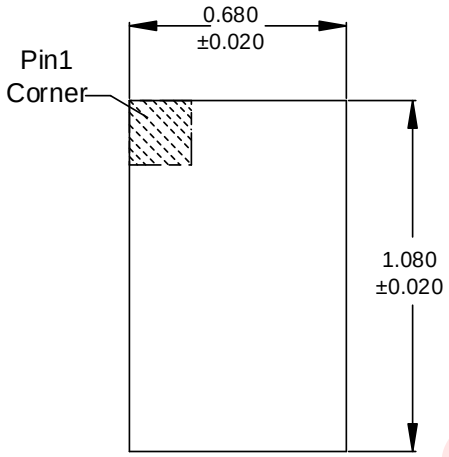
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

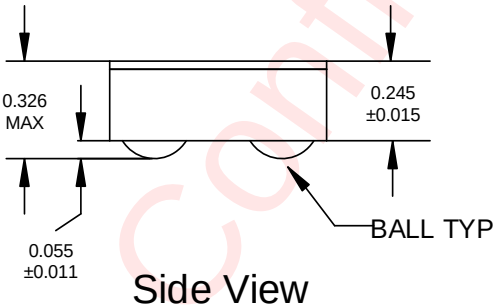
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	0.78	1.21	0.38	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

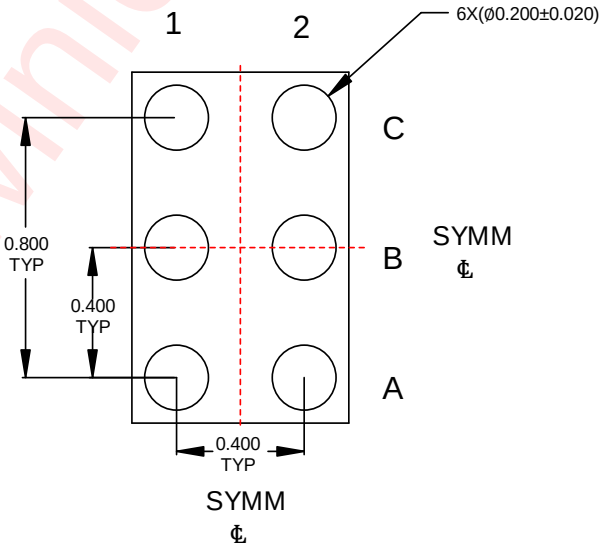
Package Description



Top View



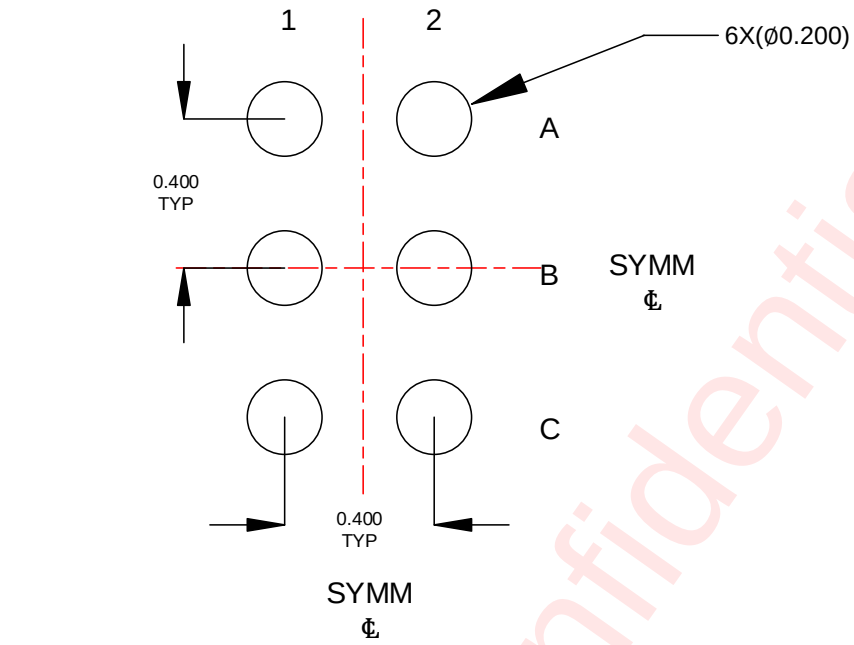
Side View

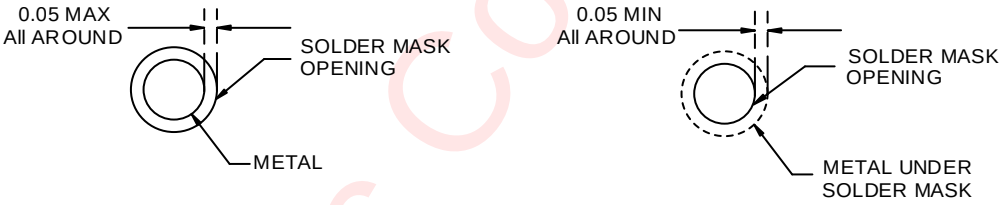


Bottom View

Unit：mm

Land Pattern Data





NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Feb 2022	Officially released
V1.1	Mar 2022	Add Advanced Mode – set up method Add ESD Test standard(MM): JESD22-A115C
V1.2	Apr 2022	Add Parameter I_{MAX1} – Maximum output current (IMAX=1) Add Parameter R_{TOTAL} – Total output resistance Add NOTE for Electrical Characteristics
V1.3	Jul 2022	Open the function – Adjustable Maximum Output Current Add Parameter I_{MAX0} and I_{MAX1} for all current gears
V1.4	Aug 2022	Add Notice for Typical Application Circuits Add Recommended Operating Conditions Clear up Detail Functional Description Clear up Register Configuration Add Application Information Add PCB Layout Consideration
V1.5	Apr 2025	Add VDD Supply And I2C Interface Timing Update the description of electrical properties Update design assurance

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