3-Wire Serial EEPROM
1Kbit (8-bit or 16-bit wide)

FEATURES

- Standard Voltage and Low Voltage Operation:
  - FT93C46A: V_{CC} = 1.7V to 5.5V
- User Selectable Internal Organization:
  - FT93C46A: 128 x 8 or 64 x 16
- 2 MHz Clock Rate (5V) Compatibility.
- Industry Standard 3-wire Serial Interface.
- Self-Timed ERASE/WRITE Cycles (5ms max including auto-erase).
- Automatic ERAL before WRAL.
- Sequential READ Function.
- High Reliability: Typical 1 Million Erase/Write Cycle Endurance.
- 100 Years Data Retention.
- Industrial Temperature Range (-40^{o}C to 85^{o}C).
- Standard 8-pin SOP/TSSOP/DIP/UDFN Pb-free Packages.

DESCRIPTION

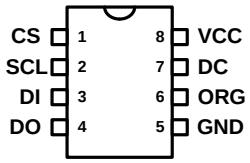
The FT93C46A series are 1024 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 64 words of 16 bits each when the ORG pin is connected to VCC (or unconnected) and 128 words of 8 bits (1 byte) each when the ORG pin is tied to ground. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead SOP package, 8-lead TSSOP, 8-lead DIP and 8-lead UDFN packages. Our extended V_{CC} range (1.7V to 5.5V) devices enables wide spectrum of applications.

The FT93C46A is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Serial Clock (SCL). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Once a device begins its self-timed program procedure, the data out pin (DO) can indicate the READY/BUSY status by rising chip select (CS).

PIN CONFIGURATION

Pin Name	Pin Function
CS	Chip Select
SCL	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
ORG	Internal Organization
DC	Don't Connect
VCC	Power Supply
GND	Ground

All these packaging types come in Pb-free certified.



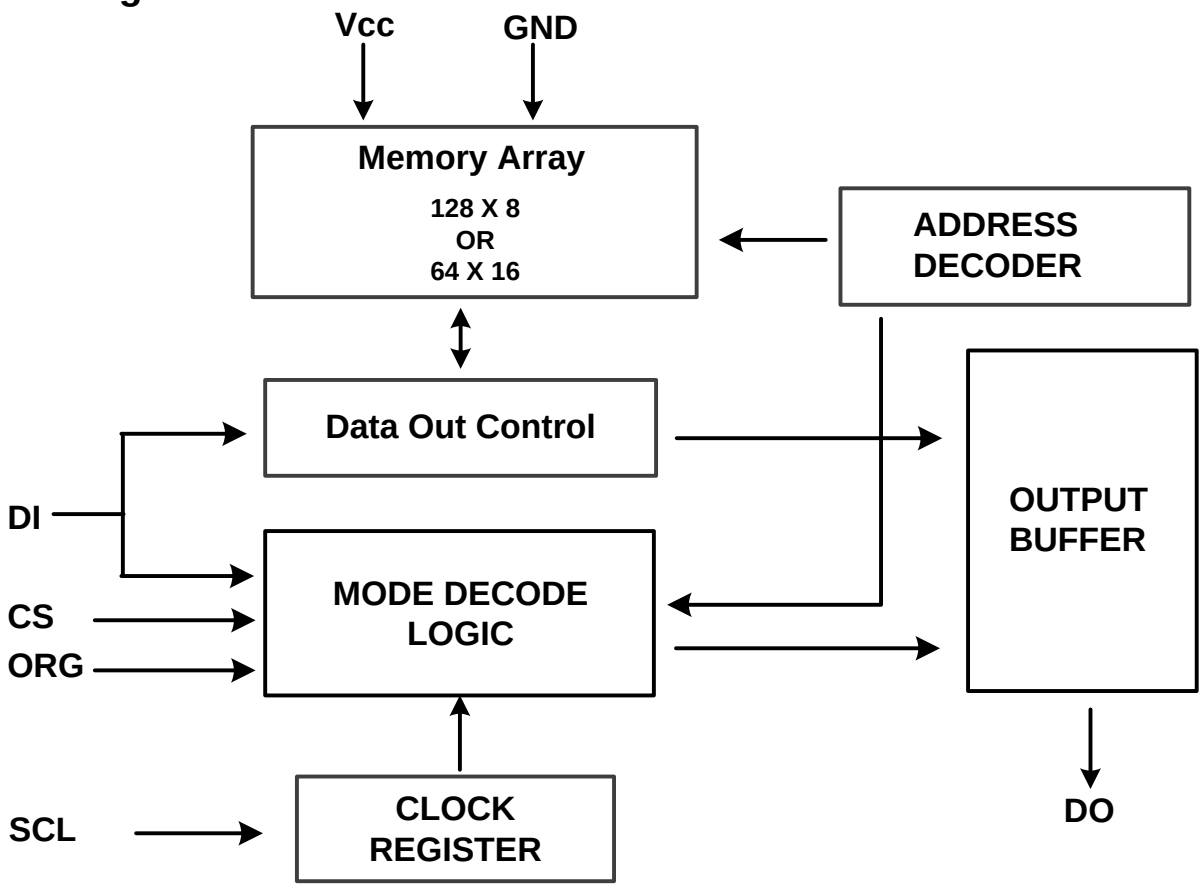
8L SOP
8L TSSOP
8L DIP
8L UDFN

ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40°C to 85°C
Storage temperature:	-50°C to 125°C
Input voltage on any pin relative to ground:	-0.3V to V_{CC} + 0.3V
Maximum voltage:	8V

*** Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.**

Block Diagram



PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the rising edge of this clock is to clock data out of the EEPROM device.

(B) CHIP SELECT (CS)

This is the chip select input signal for the serial EEPROM device. .

(C) SERIAL DATA INPUT (DI)

This is data input signal for the serial device.

(D) SERIAL DATA OUTPUT (DO)

This is data output signal for the serial device.

(E) INTERNAL ORGANIZATION (ORG)

This is internal organization input signal for the serial EEPROM device. When the ORG pin is connected to VCC or unconnected the EEPROM is organized as 64 words of 16 bits each and when ORG pin is connected to ground the EEPROM is organized as 128 bytes of 8 bits each. Typically, these signals are hardwired to either V_{IH} or V_{IL}. If left unconnected, they are internally recognized as V_{IH}.

MEMORY ORGANIZATION

The FT93C46A memory is organized either as bytes (x8) or as words (x16). If Internal Organization (ORG) is unconnected (or connected to VCC) the words (x16) organization is selected; When Internal Organization is connected to ground the bytes (x8) organization is selected.

INSTRUCTION SET for the FT93C46A

Instruction	SB	Op Code	Address[1]		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A_6- A_0	A_5- A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11xxxxx	11xxxx			Write enable must precede all programming modes.
EWDS	1	00	00xxxxx	00xxxx			Disables all programming instructions.
ERASE	1	11	A_6- A_0	A_5- A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_6- A_0	A_5- A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	00	10xxxxx	10xxxx			Erases all memory locations.
WRAL	1	00	01xxxxx	01xxxx	D_7 - D_0	D_{15} - D_0	Writes all memory locations.

1. X = Don't Care bit.

(A) START BIT (SB)

Each instruction is preceded by a rising edge on Chip Select (CS) with Serial Clock (SCL) being held Low.

(B) OPERATION CODE (OP-CODE)

Two op-code bits, read on Serial Data Input (DI) during the rising edge of Serial Clock (SCL).

(C) ADDRESS

The address bits of the byte or word that is to be accessed. For the FT93C46A, the address is made up of 6 bits for the x16 organization or 7 bits for x8 organization.

(D) DATA

The data bits of the byte or word that is to be accessed. For the FT93C46A, the data is made up of 16 bits (word) for the x16 organization or 8 bits (byte) for x8 organization.

INSTRUCTION SETS DESCRIPTION

(A) READ

The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SCL. It should be noted that when a dummy bit (logic “0”) precedes the 8- or 16-bit data output string.

(B) ERASE/WRITE ENABLE

To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

(C) ERASE/WRITE DISABLE

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the

READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

(D) ERASE

The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

(E) WRITE

The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.

(F) ERASE ALL

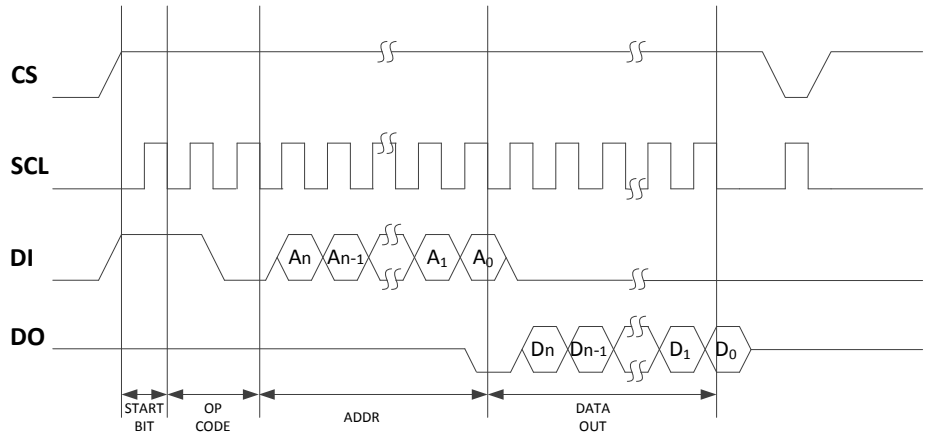
The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

(G) WRITE ALL

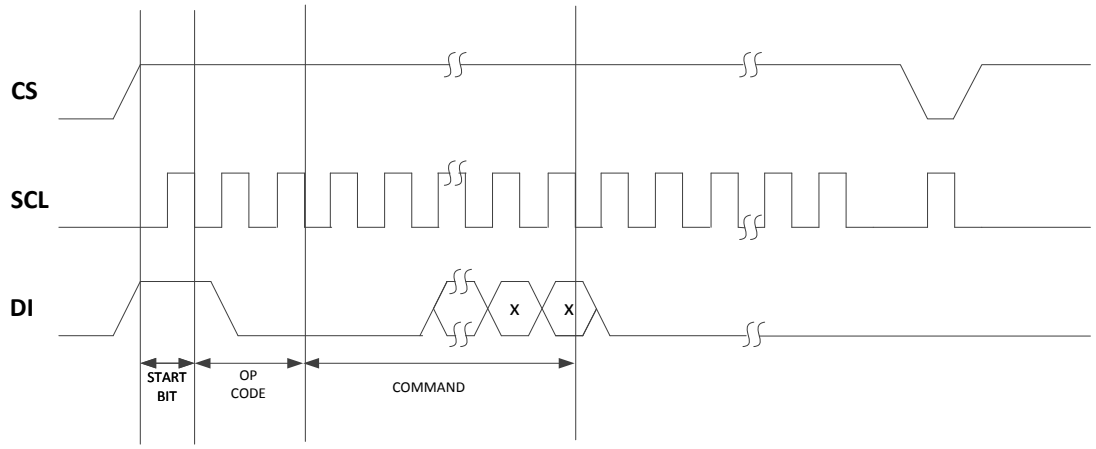
The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

Timing Diagrams

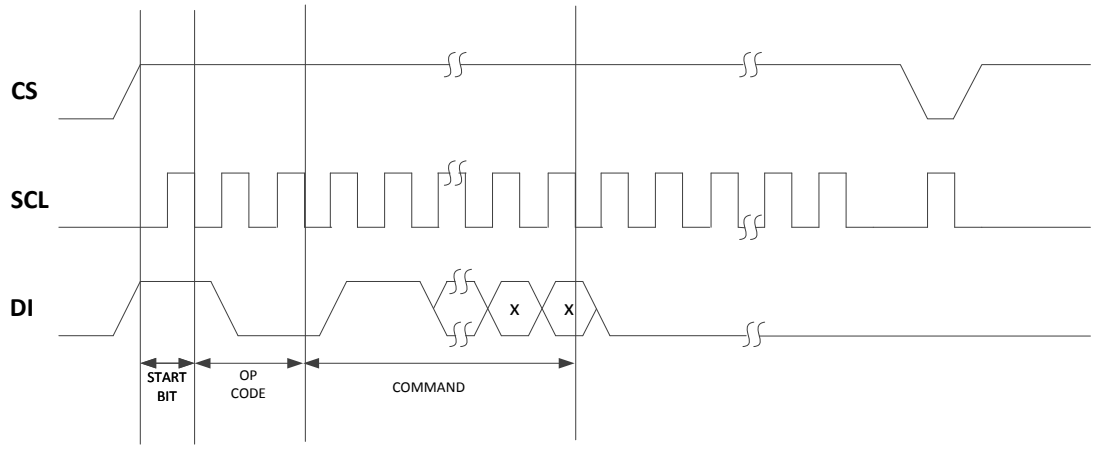
READ Timing



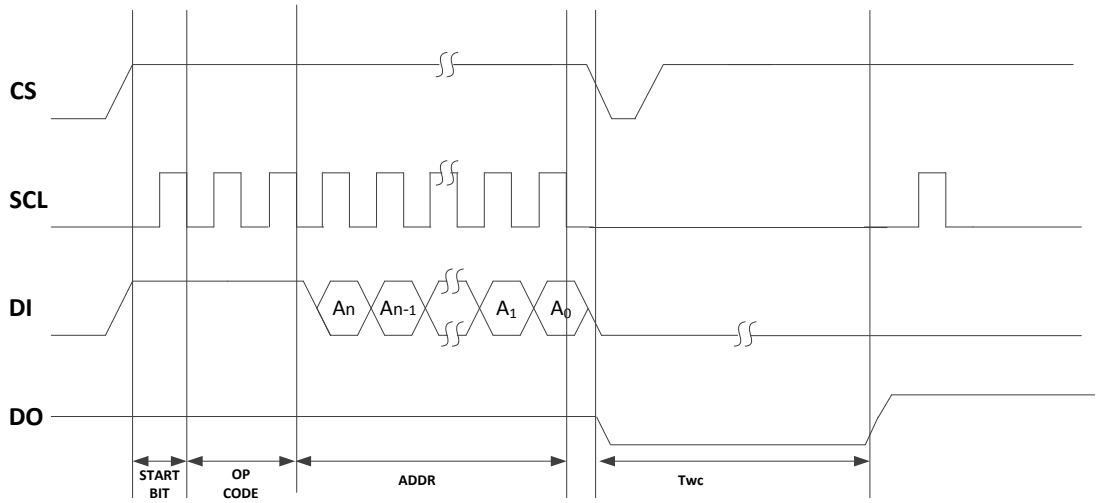
EWDS Timing



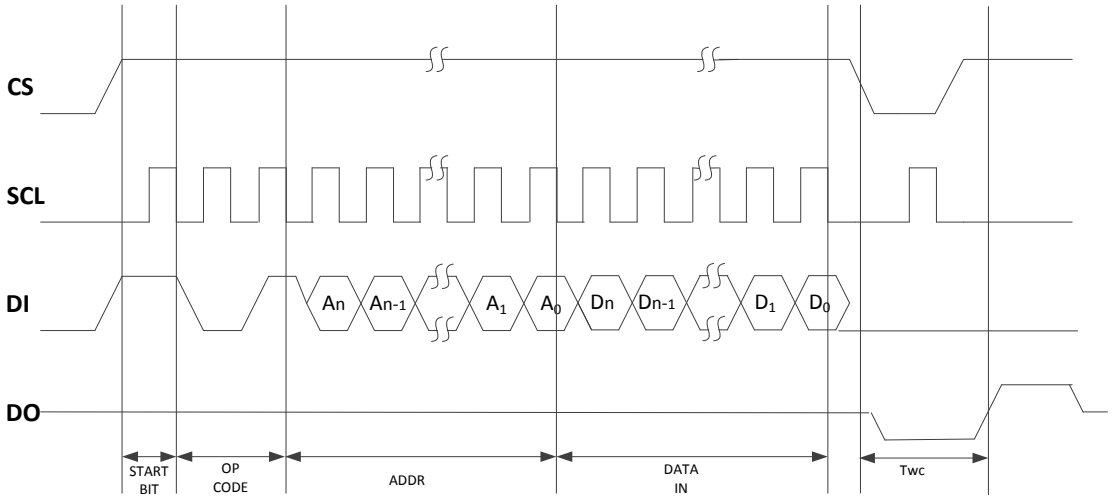
EWEN Timing



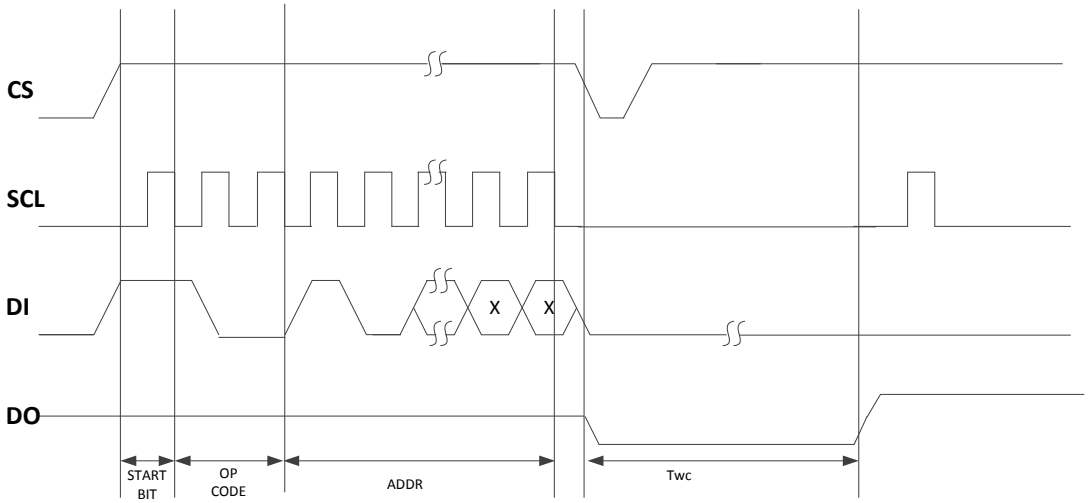
ERASE Timing



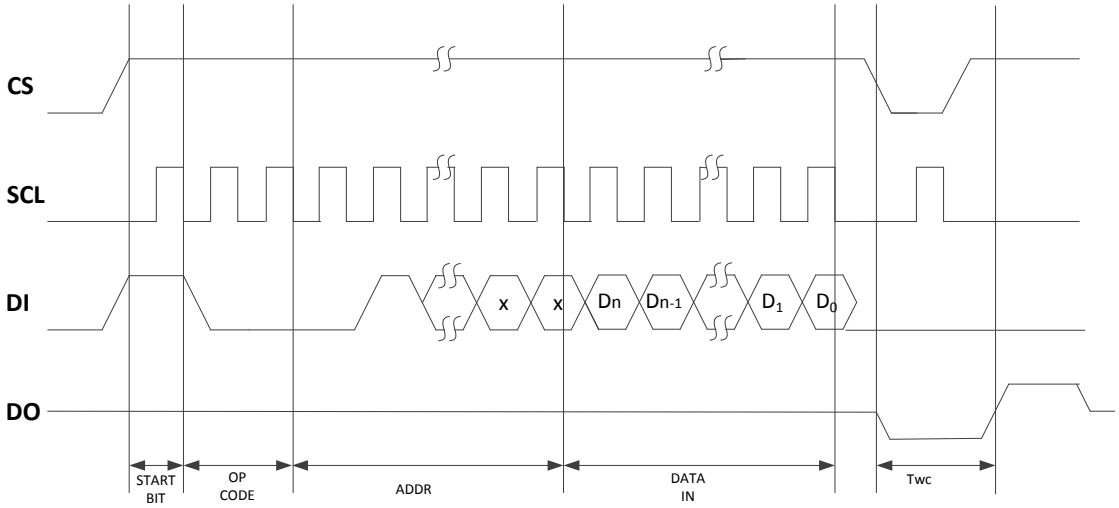
WRITE Timing



ERAL Timing(1)

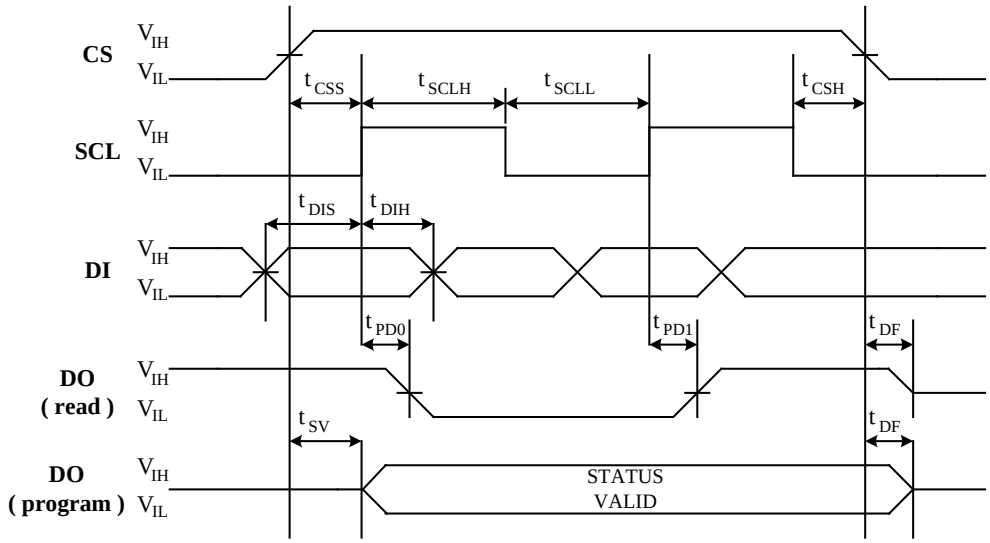


WRAL Timing(2)



Note : 1. Valid only at V_{CC}=4.5V to 5.5V
2. Valid only at V_{CC}=4.5V to 5.5V

Synchronous Data Timing



AC CHARACTERISTICS

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V.

Symbol	Parameter[1]	1.7V ≤ V_{CC} < 2.7V		2.7V ≤ V_{CC} < 4.5V		4.5V ≤ V_{CC} ≤ 5.5V		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	0.25	0	1	0	2	MHz
t_{SCLH}	SCL High Time	1000		250		200		ns
t_{SCLL}	SCL Low Time	1000		250		200		ns
t_{CS}	Minimum CS Low Time	1000		250		200		ns
t_{CSS}	CS Setup Time	200		50		50		ns
t_{CSH}	CS Hold Time	0		0		0		ns
t_{DIS}	DI Setup Time	400		100		100		ns
t_{DIH}	DI Hold Time	400		100		100		ns
t_{PD1}	Output Delay to '1'		1000		250		200	ns
t_{PD0}	Output Delay to '0'		1000		250		200	ns
t_{SV}	CS to Status Valid		1000		250		200	ns
t_{DF}	CS to DO in Hi-Z		400		100		100	ns
t_{WC}	Write Cycle Time		10		5		5	ms

Notes: 1. The parameters are expected by characterization but are not fully screened by test.

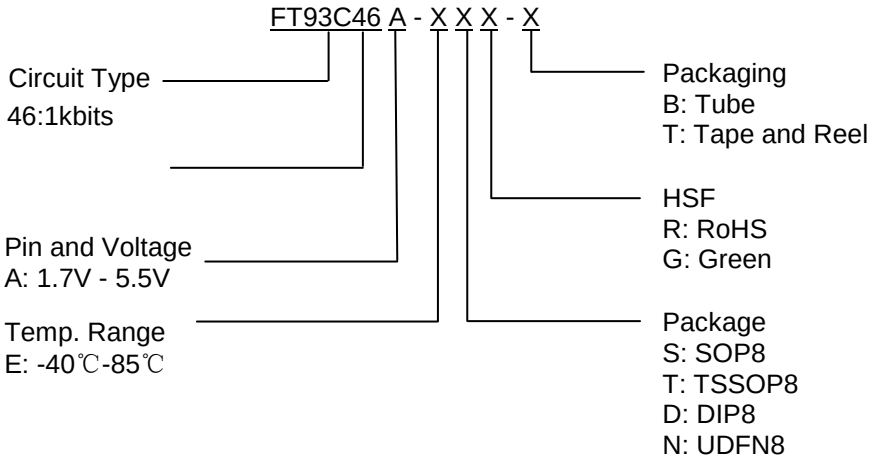
DC CHARACTERISTICS

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter[1]	Test Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Read Current	V_{CC} = 5.0V; SCL=1.0 MHz		0.5	2	mA
I_{CC2}	Write Current	V_{CC} = 5.0V; SCL=1.0 MHz		0.5	2	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V; CS = 0V			0.2	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V; CS = 0V			1.5	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V; CS = 0V			1.5	µA
I_{IL}	Input Leakage	V_{in} = 0V to V_{CC}		0.1	1	µA
I_{OL}	Output Leakage	V_{in} = 0V to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage	1.7V ≤ V_{CC} ≤ 5.5V	-0.3		V_{CC}x0.2	V
V_{IH}	Input High Voltage	1.7V ≤ V_{CC} ≤ 5.5V	V_{CC}x0.7		V_{CC}+0.5	V
V_{OL1}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V; I_{OL} = 2.1 mA			0.4	V
V_{OL2}	Output Low Voltage	1.7V ≤ V_{CC} < 2.7V; I_{OL} = 0.15 mA			0.2	V
V_{OH1}	Output High Voltage	2.7V ≤ V_{CC} ≤ 5.5V; I_{OH} = -0.4 mA	2.4			V
V_{OH2}	Output High Voltage	1.7V ≤ V_{CC} < 2.7V; I_{OH} = -100 µA	V_{CC}-0.2			V

Notes: 1. The parameters are expected by characterization but are not fully screened by test.

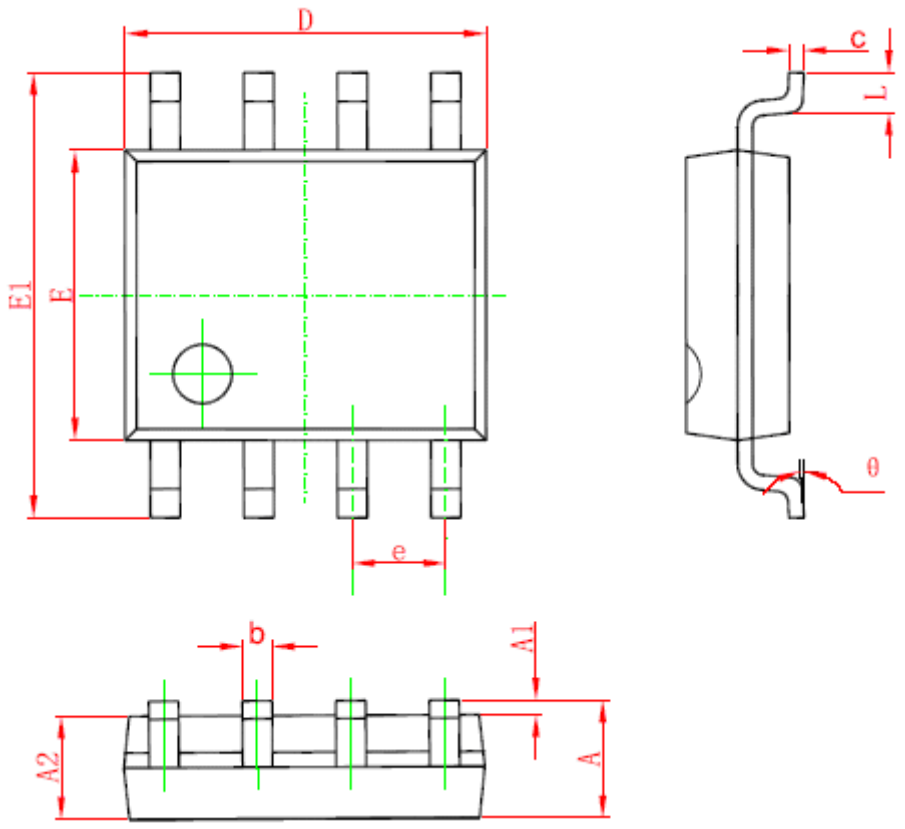
Order code:


FT93C46 A - X X X - X
Circuit Type
46:1kbits
Pin and Voltage
A: 1.7V - 5.5V
Temp. Range
E: -40℃-85℃
Packaging
B: Tube
T: Tape and Reel
HSF
R: RoHS
G: Green
Package
S: SOP8
T: TSSOP8
D: DIP8
N: UDFN8

ORDER INFORMATION

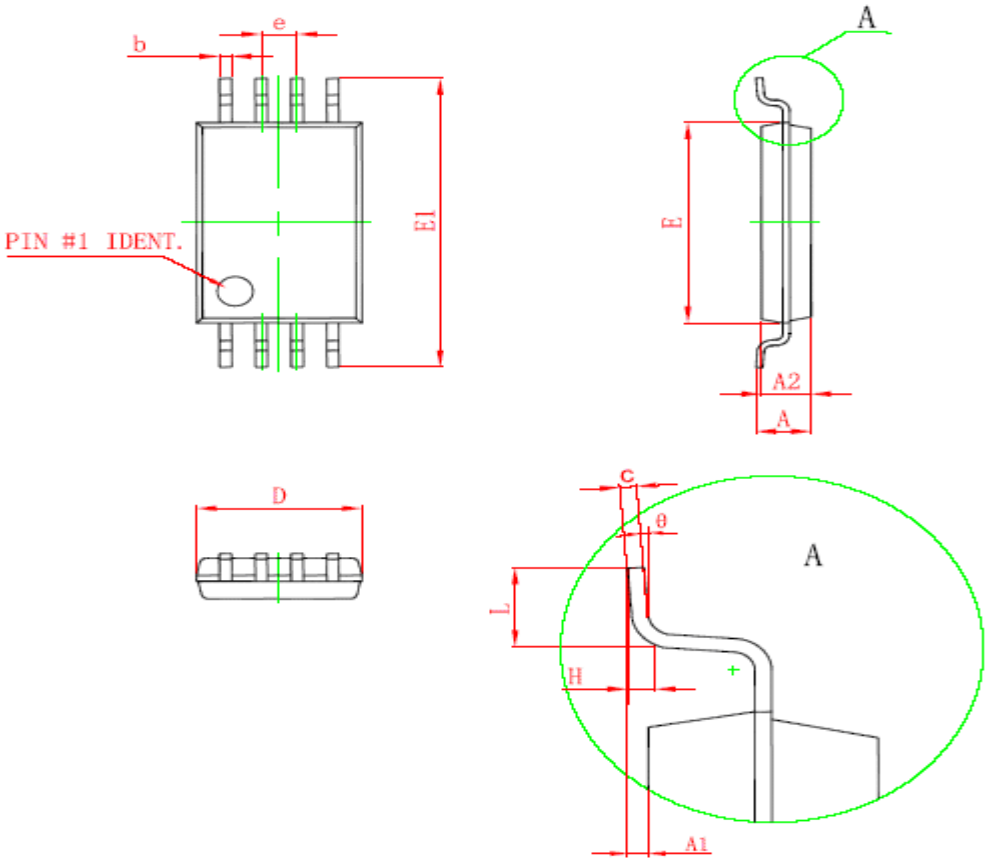
Density	Package	Temperature Range	Voltage	HSF	Packaging	Ordering Code
1kbits	SOP8	-40℃-85℃	1.7V-5.5V	RoHS	Tube	FT93C46A-ESR-B
					Tape and Reel	FT93C46A-ESR-T
				Green	Tube	FT93C46A-ESG-B
					Tape and Reel	FT93C46A-ESG-T
	TSSOP8			RoHS	Tube	FT93C46A-ETR-B
					Tape and Reel	FT93C46A-ETR-T
				Green	Tube	FT93C46A-ETG-B
					Tape and Reel	FT93C46A-ETG-T
	DIP8			RoHS	Tube	FT93C46A-EDR-B
	UDFN8			RoHS	Tape and Reel	FT93C46A-ENR-T

SOP8 PACKAGE OUTLINE DIMENSIONS



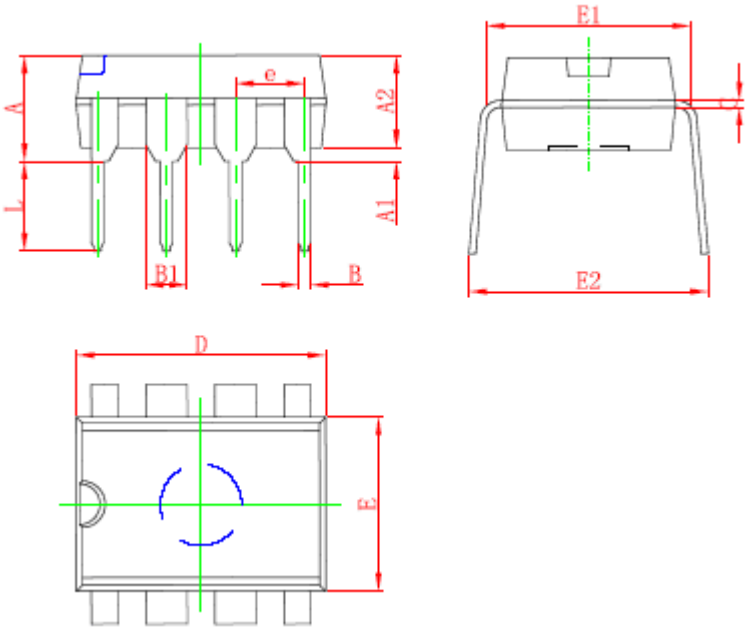
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP8 PACKAGE OUTLINE DIMENSIONS



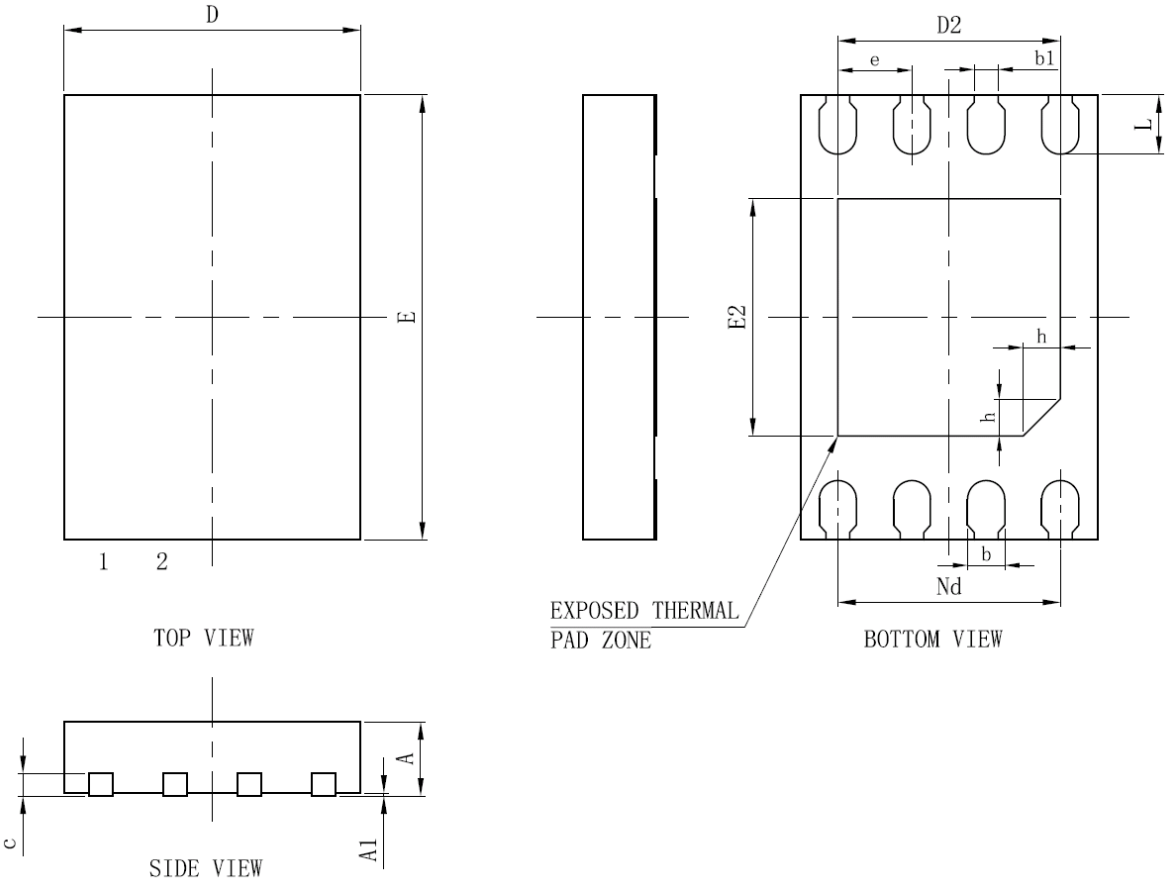
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

UDFN8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.017	0.021
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.039
b1	0.160REF		0.006REF	
c	0.100	0.200	0.004	0.008
D	1.900	2.100	0.075	0.083
D2	1.400	1.600	0.055	0.062
e	0.500BSC		0.020BSC	
Nd	1.500BSC		0.059BSC	
E	2.900	3.100	0.114	0.122
E2	1.500	1.700	0.059	0.067
L	0.300	0.500	0.012	0.020
h	0.200	0.300	0.066	0.12

REVISION HISTORY

Revision	Date	Descriptions
Rev1.0	Apr.2024	Initial version.

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