具有中断功能的16位I²C和SMBus IO扩展器

16-bit I²C-bus and SMBus IO expander with Interrupt

■ FEATURES

- Power supply range : 2.2V~5.5V
- Capable of Directly Driving LEDs
- 16 IOs can be configured as an input or an output independently
- Support interrupt, active low
- Standard I²C interface, 8 programmable device addresses (4 for HTR3339, 1 for HTR33351)
- Support Inverse Polarity Configuration
- Low Standby-Current Consumption
- Pb-free Packages, QFN4×4-24L, QFN3×3-20L

- 供电范围：2.2V~5.5V
- 支持LED驱动
- 16个IO，可任意置为独立的输入或输出
- 中断功能，低电平有效
- 标准I²C接口，8个I²C器件地址可选(HTR3339为4个，HTR33351为1个)
- 支持反极性配置
- 支持低功耗待机
- QFN4×4-24L，QFN3×3-20L，无铅封装

■ APPLICATIONS

- GPIO expansion for I²C-bus applications

- I²C总线控制的GPIO扩展应用

■ DESCRIPTION

HTR33xx is a 16-bit I²C-bus and SMBus IO expander with 2.2V~5.5V power supply. Any of the 16 IOs can be configured as an input or an output independently. Meanwhile, any IO are capable of driving LEDs directly.

At power on, the IOs are configured as inputs by default. Configurations are set through I²C interface, such as input or output selection, Polarity Inversion, and so on.

When the IOs are configured as inputs, they are continuously monitored for state changes. State changes are indicated at the INTN output. Once the IO state are read through the I2C interface, the INTN output is cleared.

HTR3339 has RSTN pin to set the registers to their default values. HTR3335, HTR33351 and HTR3339 don't include internal IO pullup resistor, so that they require external pull-ups and pull-downs on unused IOs when they are configured as inputs.

HTR3339 has 4 programmable device addresses, while HTR3355 and HTR3335 have 8, and HTR33351 has 1.

HTR33xx is available in QFN4×4-24L and QFN3×3-20L package.

HTR33xx是一款I²C和SMBus IO扩展器，2.2V~5.5V电源供电。16个IO端口中的任何一个都可以单独配置为输入或输出。此外，任一IO可驱动LED。

通电后，16个IO端口配置默认为输入，并可通过I²C进行相关配置，如输入或输出选择、反极性等配置

所有配置为输入的IO端口都会持续监控状态变化，IO口的变化由INTN输出指示。当IO状态通过I²C接口被读取时，INTN输出被清除。

HTR3339具有RSTN引脚，其拉低时所有寄存器恢复到默认状态。HTR3335，HTR33351和HTR3339的IO内部没有上拉电阻，因此当其配置为输入且未使用时，需要外部的上下拉。

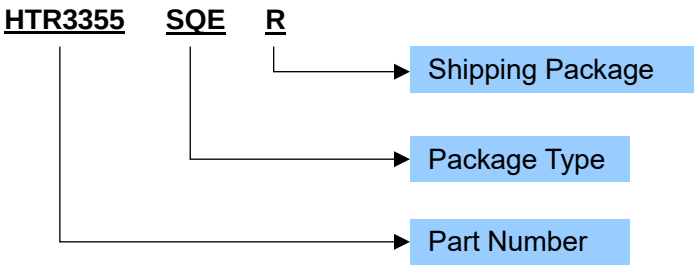
HTR3339具有4个器件地址，HTR3355和HTR3335则有8个，HTR33351则有1个。

HTR33xx提供QFN4×4-24L和QFN3×3-20L封装。

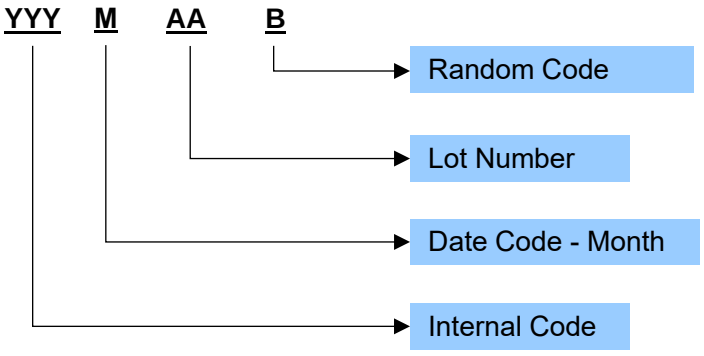
■ ORDERING INFORMATION

Ordering Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HTR3355SQER	QFN4×4-24L (SQE)	HTR3355 YYYMAAB[1]	-40℃～85℃	Tape and Reel (R) 5000PCS
HTR3335SQER	QFN4×4-24L (SQE)	HTR3335 YYYMAAB	-40℃～85℃	Tape and Reel (R) 5000PCS
HTR3339SQER	QFN4×4-24L (SQE)	HTR3339 YYYMAAB	-40℃～85℃	Tape and Reel (R) 5000PCS
HTR33351SQER	QFN3×3-20L (SQE)	HTR33351 YYYMAAB	-40℃～85℃	Tape and Reel (R) 5000PCS

Ordering Number

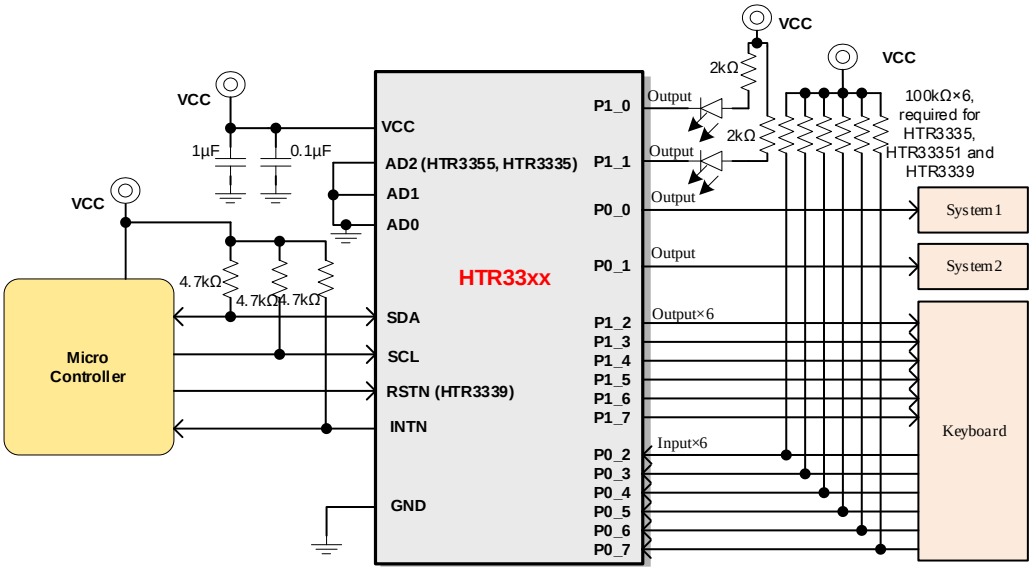


Production Tracking Code



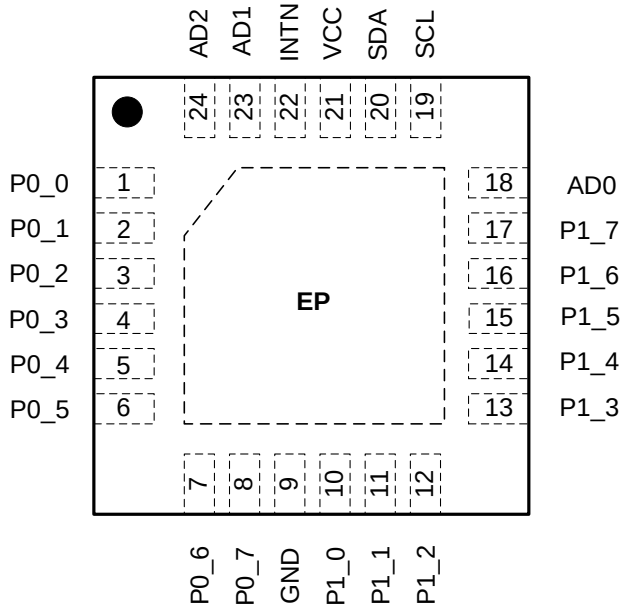
[1] YYYMAAB is production tracking code

■ TYPICAL APPLICATION

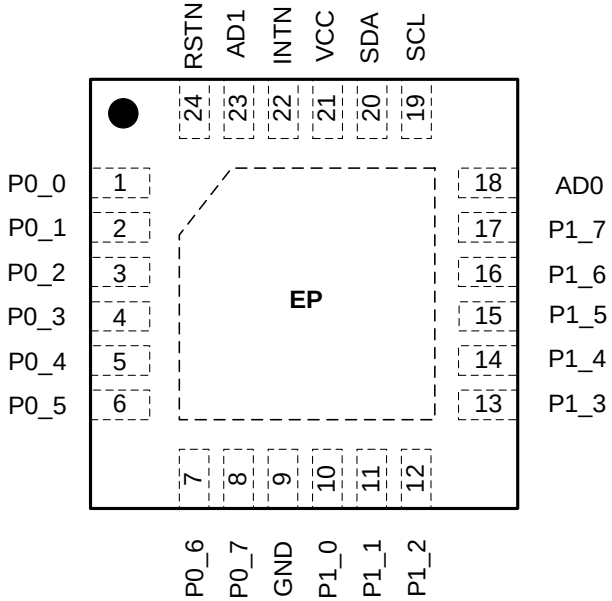


Functional LED drivers, IO and Keyboard expander

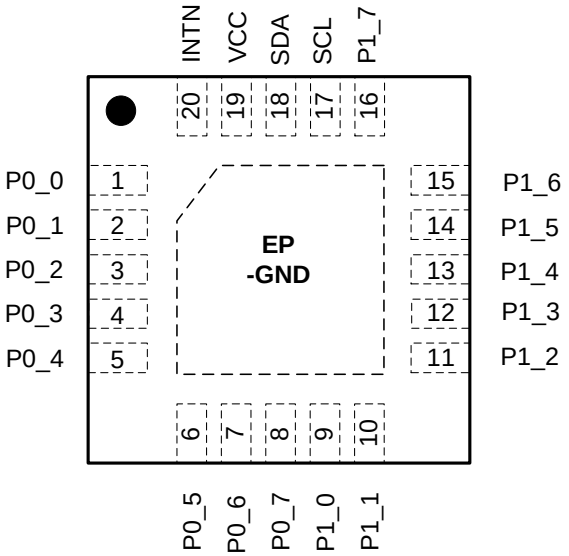
■ TERMINAL CONFIGURATION



HTR3355, HTR3335 Top View



HTR3339 Top View



HTR33351 Top View

■ TERMINAL FUNCTION

Name	Description
P1_0~P0_7	Input or output terminal, push-pull structure, input as default. 输入或输出（推挽结构），默认输入。
GND	Ground. 地
P1_0~P1_7	Input or output terminal, push-pull structure, input as default. 输入或输出（推挽结构），默认输入。
AD0	I^2C device address, connect to VCC or GND。 I^2C器件地址选择，接VCC或GND。
SCL	I^2C serial clock. I^2C时钟
SDA	I^2C serial data. I^2C数据
VCC	Power supply. 电源输入端.
INTN	Interrupt output pin, open-drain, need external pull-up resistor; active low. 中断输出，开漏结构，需外部上拉电阻；低有效
AD1	I^2C device address, connect to VCC or GND。 I^2C器件地址选择，接VCC或GND。
AD2 (HTR3355, HTR3335) RSTN (HTR3339)	AD2: I^2C device address, connect to VCC or GND。 AD2: I^2C器件地址选择，接VCC或GND。 RSTN: Hardware reset pin, active low. RSTN: 硬件复位，低为复位
EP (GND)	Provides both electrical and thermal connection from the device to the board. Connect to the system ground. 接地。

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage for VCC	V_{CC}	-0.5		6	V
Input Voltage	V_I	-0.5		6	V
Output Voltage	V_O	-0.5		6	V
Input current	I_I			±20	mA
Output current	I_O			±50	mA
Continuous supply current	I_{CC}			160	mA
Continuous current through GND	I_{SS}			-250	mA
Moisture Sensitivity Level (MSL)			MSL3		
Ambient Operating Temperature	T_A	-40		85	℃
Junction Temperature	T_J			150	℃
Storage Temperature	T_{STG}	-65		150	℃
ESD (HBM)			±2		kV

● Main Electrical Characteristics

Condition: T_A = 25°C, VCC = 3.6V, unless otherwise specified

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage and current						
Power supply voltage for VCC	V_{CC}		2.2		5.5	V
Power On Reset Voltage, rising	V_{PORR}			1.8		V
Power On Reset Voltage, falling	V_{PORF}			1.6		V
Supply current	I_{CC}	I_O =0, I/O =inputs, f_{SCL}= 400kHz, tr =3 ns, No load, V_{CC}= 5.5V		22		uA
		I_O =0, I/O =inputs, f_{SCL}= 400kHz, tr =3 ns, No load, V_{CC}= 3.6V		11		uA
		I_O =0, I/O =inputs, f_{SCL}= 400kHz, tr =3 ns, No load, V_{CC}= 2.7V		8		uA
		I_O =0, I/O =inputs, f_{SCL}= 400kHz, tr =3 ns, No load, V_{CC}= 1.95V		5		uA
Standby current	I_{SD}	V_I = GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load, V_{CC}= 5.5V		1.1		uA
		V_I = GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load, V_{CC}= 3.6V		0.7		uA
		V_I = GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load, V_{CC}= 2.7V		0.5		uA
		V_I = GND, I_O = 0, I/O = inputs, f_{SCL} =0 kHz, No load, V_{CC}=1.95V		0.3		uA
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load, V_{CC}= 5.5V		2.5		uA
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load, V_{CC}= 3.6V		1		uA
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load, V_{CC}= 2.7V		0.7		uA
		V_I = V_{CC}, I_O = 0, I/O = inputs, f_{SCL} =0 kHz, No load, V_{CC}=1.95V		0.5		uA
Input and Output						
Low-level input voltage	V_{IL}		-0.5		0.3V_{CC}	V
High-level input voltage	V_{IH}	SCL, SDA	0.7V_{CC}		V_{CC}	V
		Ax, RSTN, IOs	0.7V_{CC}		5.5	V
High-level output current	I_{OH}	IOs			-10	mA

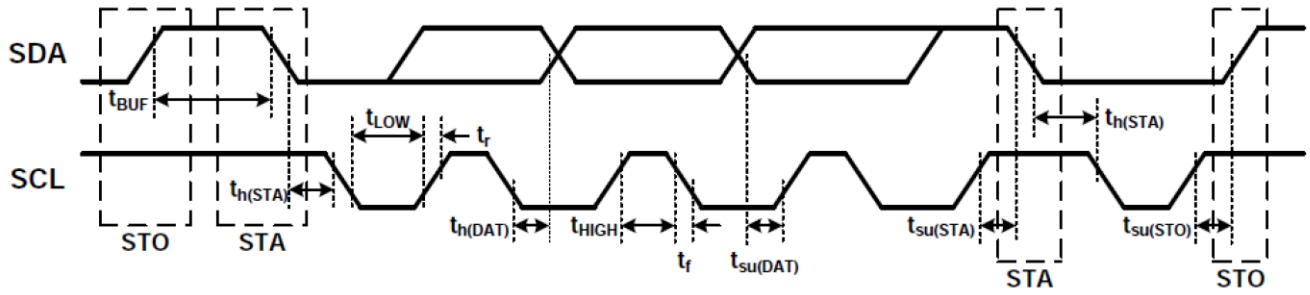
[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Low-level output current	I_{OL}	SDA, INTN, V_{OL} = 0.4 V	3			mA
		IOs, V_{OL} = 0.5 V	8			mA
		IOs, V_{OL} = 0.7 V	10			mA
High-level output voltage	V_{OH}	IOs, I_{OH} = -8mA, V_{CC} = 2.3V	1.8			V
		IOs, I_{OH} = -10mA, V_{CC} = 2.3V	1.7			V
		IOs, I_{OH} = -8mA, V_{CC} = 3.0V	2.6			V
		IOs, I_{OH} = -10mA, V_{CC} = 3.0V	2.5			V
		IOs, I_{OH} = -8mA, V_{CC} = 4.75V	4.1			V
		IOs, I_{OH} = -10mA, V_{CC} = 4.75V	4.0			V
HIGH-level input leakage current	I_{LIH}	V_I = V_{CC}			1	uA
LOW-level input leakage current	I_{LIL}	V_I = V_{SS}, IOs			-100	uA
		V_I = V_{SS}, SCL, SDA, Ax, RSTN			1	uA
Internal pull-up resistor for each IO	R_{UP}	Only for HTR3355		100		kohm
Input capacitance	C_i	SCL, SDA,		6	10	pF
		IOs		3.7	5	pF
output capacitance	C_O	IOs		3.7	5	pF

- **I²C Control Port**

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Serial-Clock frequency	f_{SCL}			400	kHz
Bus free time between a STOP and a START condition	t_{BUF}	1.3			us
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{h(STA)}$	0.6			us
Setup time for a repeated START condition	$t_{su(STA)}$	0.6			us
Setup Time for SCL to STOP condition	$t_{su(STO)}$	0.6			us
Data hold time	$t_{h(DAT)}$	0		0.9	us
Setup Time, SDA to SCL	$t_{su(DAT)}$	100			ns
Required Pulse Duration, SCL HIGH	t_{HIGH}	0.7			us
Required Pulse Duration, SCL LOW	t_{LOW}	1.3			us
Rise Time, SCL and SDA	T_r			300	ns
Fall Time, SCL and SDA	T_f			300	ns



- **Reset Timing**

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Reset pulse duration	t_W	6			ns
Reset recovery time	t_{REC}	0			ns
Time to reset; for VCC = 2.2 V ~ 5.5 V	t_{reset}	400			ns

- **Port Timing and Interrupt Timing**

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
data output valid time (from SCL to IO output), VCC = 2.2 V ~ 5.5 V	t_{V_IO}			200	ns
data input set-up time (from IO input to SCL)	t_{SU}	150			ns
data input hold time (from IO input to SCL)	t_H	1			us
valid time on pin INTN (from IO input to INT)	t_{V_INT}			4	us
reset time on pin INTN (from SCL to INT)	t_{RST_INT}			4	us

■ APPLICATION INFORMATION

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At power on, the IOs are configured as inputs by default. Configurations are set through I²C interface, such as input or output selection, Polarity Inversion, and so on.

When the IOs are configured as inputs, they are continuously monitored for state changes. State changes are indicated at the INTN output. Once the IO state are read through the I²C interface, the INTN output is cleared.

HTR3339 has RSTN pin to set the registers to their default values. HTR3335, HTR33351 and HTR3339 don't include internal IO pullup resistor, so that they require external pull-ups and pull-downs on unused IOs when they are configured as inputs.

HTR3339 has 4 programmable device addresses, while HTR3355 and HTR3335 have 8, and HTR33351 has 1.

HTR33xx is available in QFN4×4-24L and QFN3×3-20L package.

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所有配置为输入的IO端口都会持续监控状态变化，IO口的变化由INTN输出指示。当IO状态通过I²C接口被读取时，INTN输出被清除。

HTR3339具有RSTN引脚，其拉低时所有寄存器恢复到默认状态。HTR3335, HTR33351和HTR3339的IO内部没有上拉电阻，因此当其配置为输入且未使用时，需要外部的上下拉。

HTR3339具有4个器件地址，HTR3355和HTR3335则有8个, HTR33351则有1个。

HTR33xx提供QFN4×4-24L和QFN3×3-20L封装。

1 Power On Reset

Once HTR33xx is powered on, an internal power-on reset was made after VCC reaches V_{PORR}, and the registers of HTR33xx resume into default states. After that, VCC must be lowered to below V_{PORF} for another power-reset cycle.

HTR33xx通电后，VCC到达VPORR后，HTR33xx的寄存器恢复到默认状态。之后，必须将VCC降至V_{PORF}以下，进行另一次电源重置循环。

2 IO Input or Output Selection

The register In/Out_P0 and In/Out_P1 can configure IOs as input or output. Each bit of the register is corresponding to each IO, the bit set '1' as input, '0' as output. The default value is '0' as output.

Once the IOs are configured as input, The state of IO can be read through I²C in the register Input_P0 and Input_P1.

In/Out_P0 和 In/Out_P1 设定端口为输入、输出状态。寄存器每一 Bit 对应某个 IO 端口，该 bit 置 '1' 代表输入状态，置 '0' 代表输出状态。默认值为 0，输出状态。

IO 设置为输入时，通过 I²C 接口读 Input_Port0 和 Input_Port1 可获得当前 IO 端口逻辑状态。

3 Interrupt Function

HTR33xx will monitor IO state once IO is configured as input. The change of input IO status (from high-level to low-level or from low-level to high-level) can trigger a low state of INTN terminal. INTN is open-drain output, active low, which needs external pull-up resistor.

When the IO input status is read through the I²C interface, or the IO input status is changed to original setting, the interrupt can be cleared. When a certain IO port is configured to output mode, the change of its state will not cause interrupt.

Changing an IO from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The interrupt caused by the change of P0 status can only be cleared by reading register Input_P0, and one caused by the change of P1 status can only be cleared by reading register Input_P1. Meawhile, the interrupt can also be cleared by reset.

The interrupt sequence is as below.

一旦 IO 配置为输入，且 IO 中断功能启用，HTR33xx 将监控 IO 状态。输入 IO 状态的改变（由低变高或由高变低）会触发 INTN 脚的拉低。INTN 是开漏输出，低电平有效，需要外部上拉电阻器。

通过 I²C 接口读取 IO 输入状态（Input_P0 和 Input_P1），或者 IO 输入状态改变到初始设置时，可以清除中断。将 IO 口配置成输出模式后，其状态的变化不会产生中断。

如果引脚状态与输入端口寄存器的内容不一致，将 IO 从输出更改为输入可能会导致误中断。

由 P0 口变化产生的中断，只能通过读 Input_P0 寄存器清除；由 P1 口变化产生的中断，只能通过读 Input_P1 寄存器清除。另外，还可通过复位功能清除中断。

中断时序如下图。

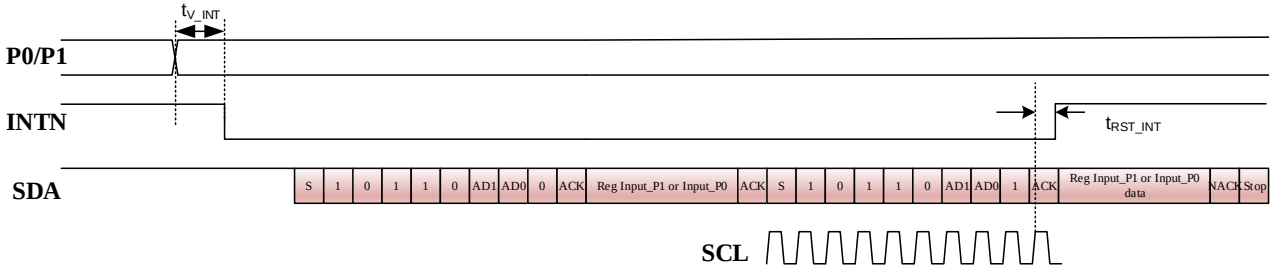

Figure 1 Interrupt Sequence

4 I²C Communication

The HTR33xx device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multi-master bus environment or wait-state insertion.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus.

Note that for multile byte reading and writing, after the first byte is read or written, additional bytes are read or written, but the data now reflect the information in or will be sent to the other register in the pair. For example, if Input P_1 is read or written, the next byte read or write is Input P_0.

HTR33xx I²C接口支持双向传输，该接口与I²C总线协议兼容，并支持100 kHz和400 kHz数据传输速率。这是一个从设备，不支持多主机的总线环境，及等待状态下的插入。

I²C总线具有两个信号，SDA（数据）和SCL（时钟），在系统中的器件之间使用串行数据传输进行通信。地址和数据的8位字节首先传输最高有效位（MSB）。此外，总线上传输的每个字节由接收设备用确认位（ACK）进行确认。每个传输操作从主设备驱动总线上的启动条件开始，并以主设备驱动总线上的停止条件结束。当时钟处于逻辑高电平时，总线使用数据终端（SDA）上的转换来指示启动和停止条件。SDA上的高到低转换表示开始，低到高转换表示停止。正常的数据位转换必须在时钟为低时发生。

主机生成7位从机地址和读/写（R/W）位，以打开与另一个设备的通信，然后等待确认条件。在应答时钟周期内，设备保持SDA低，以指示确认。当发生这种情况时，主机发送序列的下一个字节。每个设备有唯一的7位从机地址加上R/W位（1字节）。所有兼容设备通过并联的总线共享信息。

SDA和SCL需通过外部上拉电阻截至逻辑高电平。

需要特别注意的是，在连读或连写时，在读或写第一个byte后，需要读写另外的byte，读到的第二个byte的数据，或者写的第二个byte的数据，都是对应的寄存器对的另一个寄存器。例如，Input P_1寄存器读或写后，第二个byte就是对应InputP_0寄存器。

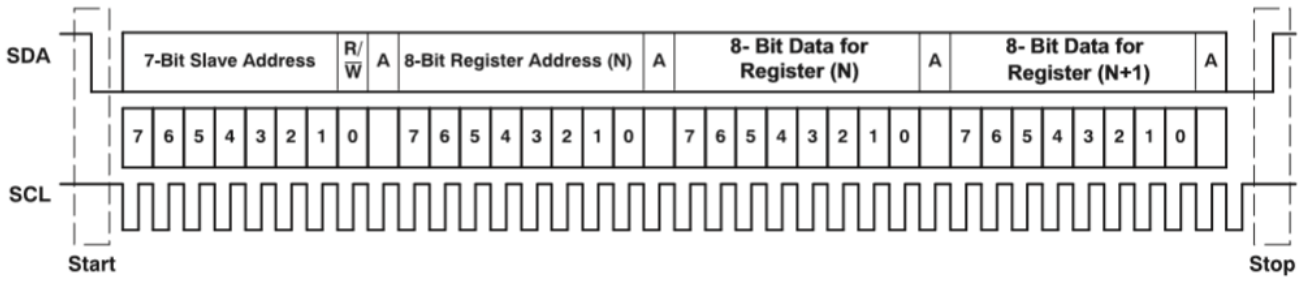

Figure 2 Typical I²C Sequence

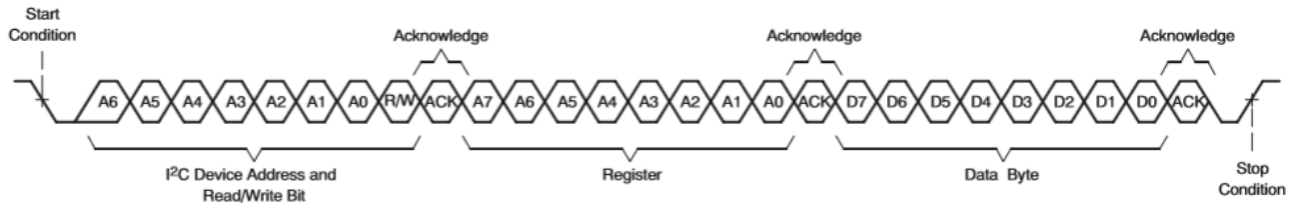

Figure 3 I²C Writing

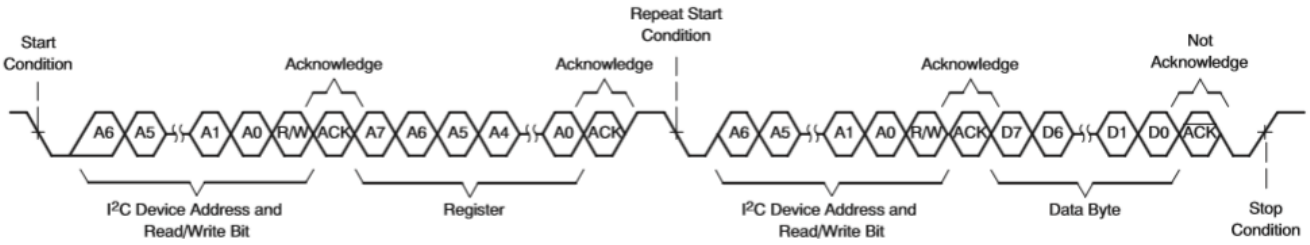

Figure 4 I²C Reading

5 Device Address

The device address of HTR33xx can be set by AD2, AD1 and AD0 terminals, see as below.

HTR33xx 器件地址由引脚 AD2、AD1、AD0 设置，如下表。

Table1 Device Address of HTR3355, HTR3335

0	1	0	0	AD2	AD1	AD0	R/W

Table2 Device Address of HTR3339

1	1	1	0	1	AD1	AD0	R/W

Table3 Device Address of HTR33351

0	1	0	0	0	0	0	R/W

6 RSTN Terminal (HTR3339)

A reset can be made by holding the RSTN pin low for a minimum of t_W. The reset timing is as below. The HTR3339 registers and I²C/SMBus state machine are held in their default states until RSTN is once again high. This input requires a pull-up resistor to VCC, if no active connection is used.

RSTN 引脚持续 t_W 的时间为低，可产生复位。复位时序如下图。在此期间，HTR3339 寄存器和 I2C/SMBus 状态机恢复到默认状态，并维持支持 RSTN 拉高。若 RSTN 无外部连接，则需要外加上拉电阻到 VCC。

NOTE:

注意：

1. After reset, all registers resume to default. The interrupt (INTN) is cleared and pulled up by external pull-up resistor.

1. 复位后，寄存器恢复到默认状态。中断状态（INTN）被清除，由外部上拉电阻将其拉高。

7 Register Map

Table4 Register Map

Register Address	R/W	Name	Function	Default Value
00h	R	Input_P0	Input state of P0 terminals	Determined by P0
01h	R	Input_P1	Input state of P1 terminals	Determined by P1
02h	R/W	Output_P0	Output state of P0 terminals	FFh
03h	R/W	Output_P1	Output state of P1 terminals	FFh
04h	R/W	Polarity Inversion P0	Inverse the polarity of input P0	00h
05h	R/W	Polarity Inversion P1	Inverse the polarity of input P1	00h
06h	R/W	In/Out_P0	Configure P0 terminals as input or output	FFh
07h	R/W	In/Out_P1	Configure P1 terminals as input or output	FFh
other	-	-	Reserved. Do not write	-

Register Address: 00h, 01h, Input state of P0, P1 terminals (default value is determined by each IO status)

Address	Name	Default	Description
00h	Input_P0	x	The current logic status of P0 terminals: 0-low level；1-high level P0 端口引脚当前逻辑状态。0-低电平；1-高电平
01h	Input_P1	x	The current logic status of P1 terminals: 0-low level；1-high level P1 端口引脚当前逻辑状态。0-低电平；1-高电平

Registers 00h,01h reflect the logic status of the IO terminals, regardless of whether the pin is defined as an input or an output. They can only be read but not written by I^2C interface. The default value of the two registers are determined by the externally applied logic level.

Bits 7 to 0 of register 00h correspond to the input status of P0_7 to P0_0 terminals, bits 7 to 0 of register 01h correspond to the input status of P1_7 to P1_0 terminals.

寄存器（00h，01h）用以反映 IO口当前的逻辑状态，不论该 IO 口是配置为输入模式还是输出模式。该寄存器仅支持读操作；写操作无效。其默认值由外部引脚电平决定。

寄存器 00h 的第 7 至第 0 位依次对应 P0_7~P0_0 的输入状态，01h 的第 7 至第 0 位依次对应 P1_7~P1_0 的输入状态。

Register Address: 02h, 03h, Output state register (default FFh)

Address	Name	Default	Description
02h	Output_P0	see Table1	Set the output status of P0 terminals. 0-low level; 1-high level 设置 P0 端口引脚输出值。0-输出低电平；1-输出高电平
03h	Output_P1	see Table1	Set the output status of P1 terminals. 0-low level; 1-high level 设置 P1 端口引脚输出值。0-输出低电平；1-输出高电平

Registers 02h, 03h is used to set the output status of IO port. Bit values in this register have no effect on IOs defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual IO value.

Bits 7 to 0 of register 02h correspond to the output status of P0_7 to P0_0 terminals, bits 7 to 0 of register 03h correspond to the output status of P1_7 to P1_0 terminals.

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寄存器（02h，03h）用以设置 IO 口的输出值。对于配置为输入模式的 IO 口，其对应的位无效；同样地，读取该寄存器的值也只能读到寄存器本身的值，而不能读到对应端口上的状态。

寄存器 02h 的第 7 至第 0 位依次对应 P0_7~P0_0 的输出状态，03h 的第 7 至第 0 位依次对应 P1_7~P1_0 的输出状态。

Register Address: 04h, 05h, Polarity Inversion Register (default 00h)

Address	Name	Default	Description
04h	In/Out_P0	00h	Inverse the polarity of input P0. 0-retained polarity; 1-inverse polarity 设置 P0 输入端口是否反向。0-保持极性；1-反向
05h	In/Out_P1	00h	Inverse the polarity of input P0. 0-retained polarity; 1-inverse polarity 设置 P1 输入端口是否反向。0-保持极性；1-反向

The Polarity Inversion registers (04H, 05H) allow polarity inversion of IOs defined as input. If a bit in this register is set to 1, the corresponding port pin's polarity is inverted. If a bit in this register is set to 0, the corresponding port pin's polarity is retained.

Bits 7 to 0 of register 04h correspond to the output status of P0_7 to P0_0 terminals, bits 7 to 0 of register 05h correspond to the output status of P1_7 to P1_0 terminals.

配置寄存器（04H，05H）用以设置 输入 IO 口的反向。若某一位设置为 1，则其对应的端口极性为反向；若某一位设置为 0，则其对应的端口没有反向。

寄存器 04H 的第 7 至第 0 位依次对应 P0_7~P0_0 的配置控制，05H 的第 7 至第 0 位依次对应 P1_7~P1_0 的配置控制。

Register Address: 06h, 07h, Input / Output Configuration register (default FFh)

Address	Name	Default	Description
06h	In/Out_P0	FFh	Configure P0 terminals as input or output. 0-output; 1-input 设置 P0 端口为输入或输出。0-输出模式；1-输入模式
07h	In/Out_P1	FFh	Configure P1 terminals as input or output. 0-output; 1-inputl 设置 P1 端口为输入或输出。0-输出模式；1-输入模式

The Configuration registers (06H, 07H) configure the directions of the IO pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

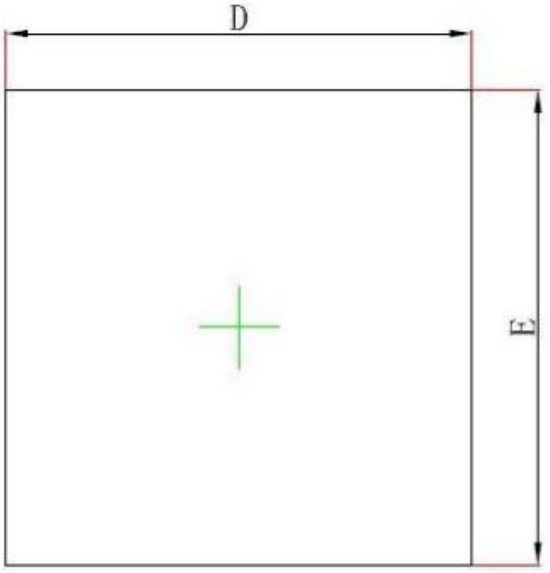
Bits 7 to 0 of register 06h correspond to the output status of P0_7 to P0_0 terminals, bits 7 to 0 of register 07h correspond to the output status of P1_7 to P1_0 terminals.

配置寄存器（06H，07H）用以设置 IO 口处于输入模式或输出模式。每一位 IO 口可单独配置为输入或输出模式。若某一位设置为 1，则其对应的端口被配置为输入模式；若某一位设置为 0，则其对应的端口被配置为输出模式。

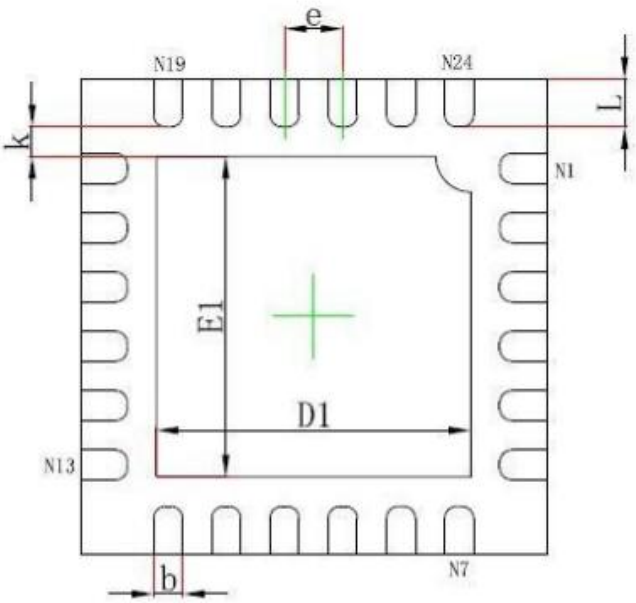
寄存器 06H 的第 7 至第 0 位依次对应 P0_7~P0_0 的配置控制，07H 的第 7 至第 0 位依次对应 P1_7~P1_0 的配置控制。

■ PACKAGE OUTLINE

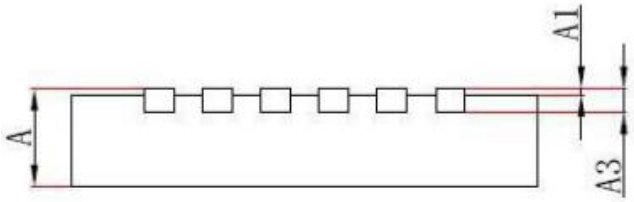
QFN4×4-24L



Top View



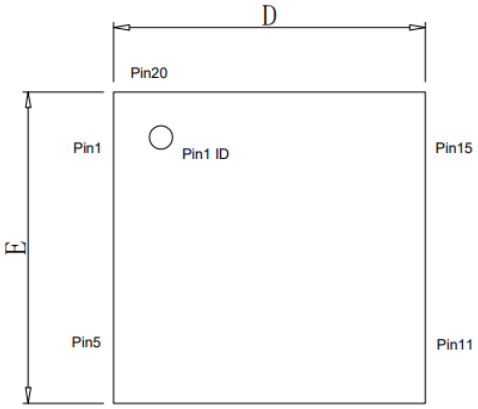
Bottom View



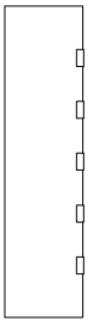
Side View

Symbol	Dimensions in Millimeters		
	Min.	NOM	Max.
A	0.700	0.750	0.800
A1	0.000		0.050
A3	0.195	0.203	0.211
D	3.900	4.000	4.100
E	3.900	4.000	4.100
E1	2.500		2.700
D1	2.600	2.700	2.800
k	0.250MIN.		
b	0.200	0.250	0.300
e	0.500TYP.		
L	0.300	0.400	0.500

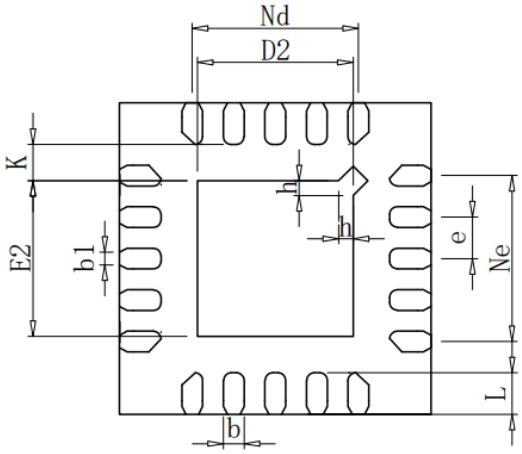
QFN3×3-20L



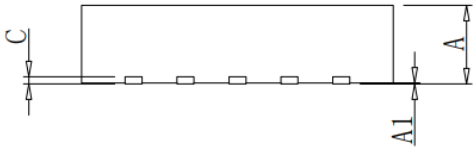
Top View



Side View



Bottom View



Side View

Symbol	Dimensions in Millimeters		
	Min.	NOM	Max.
A	0.65	0.75	0.85
A1		0.02	0.05
b	0.15	0.20	0.25
b1	0.120 REF.		
c	0.203 REF.		
D	2.90	3.00	3.10
D2	1.45	1.50	1.55
e	0.40 BSC		
Ne	1.6 BSC		
Nd	1.6 BSC		
E	2.90	3.00	3.10
E2	1.45	1.50	1.55
D1	2.600	2.700	2.800
L	0.35	0.40	0.45
h	0.15	0.20	0.25
K	0.350 TYP.		

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