125mW免输出耦合电容的立体声线路驱动器/耳机放大器

■ 特点

- 输出无需隔直流电容
- 卓越的低音效果
- 无咔嗒/噼噗声
- 低THD+N: 最低0.002%
- 低噪声, V_N:8μV
- 支持单端输入和全差分输入
- 1.65V至4.8V较宽的电源工作范围
- 输出功率: 125mW (f_{IN} = 1kHz, V_{DD}=4.2V, R_L=32Ω, THD+N=0.1%)
- 无铅封装, QFN16L-PP 3mm*3mm

■ 应用

- 耳机
- 机顶盒
- LCD电视
- 多媒体音频接口
- 蓝光/DVD播放器
- 音频消费电子产品

■ 概述

HT97180(L)是一款差分输入/单端输入、可直接输出驱动的耳机放大器/线路驱动器。4.2V供电时，器件可为32ohm耳机提供125mW的功率而不失真。器件可通过外部电阻调节增益（固定增益6dB版本需要提前定制）。器件在音频范围内具有卓越的THD+N表现。

器件具有较宽的电源工作范围，最低支持1.6V电源电压供电。

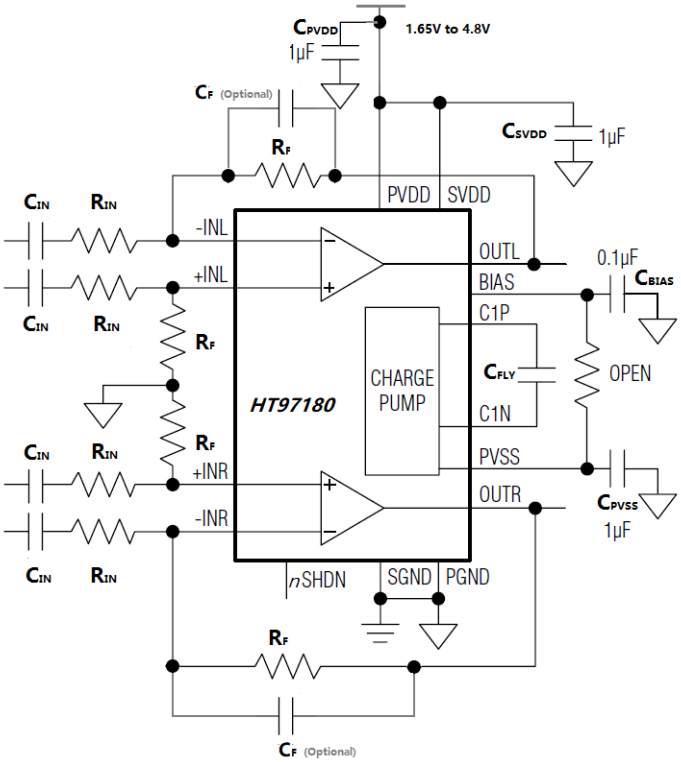
器件的启动时间为4.2ms，另130ms的版本需要提前定制。

器件内部集成电荷泵产生负电压，器件输出级由输入正电压和该负电压驱动，使得输出偏置在零电位，省去了大尺寸、容易引入失真的输出耦合电容。

器件使能开关时，没有咔嗒/噼噗声。

器件封装为3mm x 3mm, 16-pin QFN-PP，能在 -40°C 至 +85°C 温度范围内工作。

■ 典型应用



125mW Direct Drive Line Drivers/Headphone Amplifiers

■ FEATURES

- Direct Drive Outputs Eliminate DC-Blocking Capacitors, Save Space
- Excellent Bass Fidelity
- Shutdown and Startup without any Click-Pop Noise
- Exceptional Low THD+N: 0.002% Minimum
- Absolutely Low Noise Performance, V_N:8μV
- Differential or Single-Ended Input
- Wide 1.65V to 4.8V Operating Range
- Output Power: 125mW (f_{IN} = 1kHz, V_{DD}=4.2V, R_L=32Ω, THD+N=0.1%);
- Pb Free Packages, QFN16L-PP 3mm*3mm, Extremely Simple BOM Needed

■ APPLICATIONS

- Headphones
- Simple Multimedia Interfaces
- Set-Top Boxes
- Blue-ray and DVD Players
- LCD Televisions
- Prosumer Audio Devices

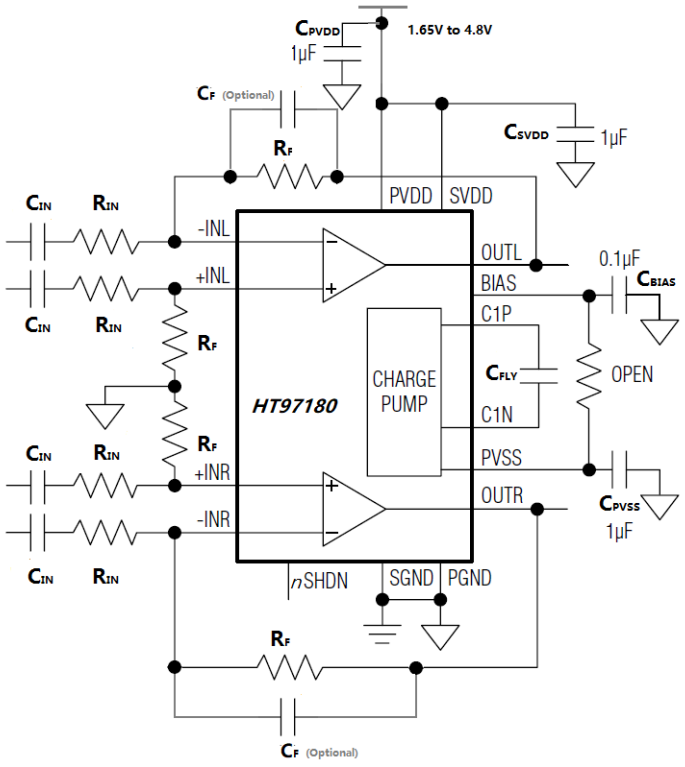
■ DESCRIPTION

The HT97180(L) is a differential input Direct Drive line driver/headphone amplifier, which can also drive single-ended input signal. It is capable of being driven with 125mW into 32Ω with a 4.2V supply. The IC is offered with an externally set gain through external resistors (or an internally fixed 6dB gain which needs to be pre-booked. The external gain setting nodes can also be used to configure filters for set-top box applications. The IC has exceptional THD+N over the full audio bandwidth.

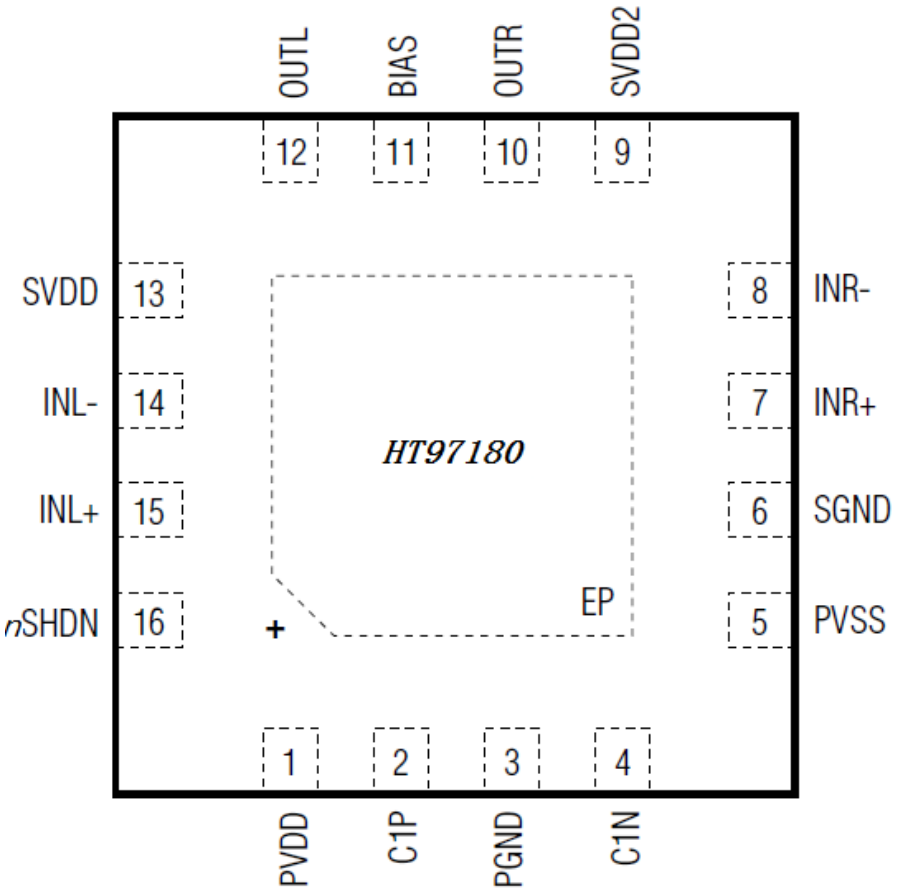
Two versions of the IC can be chosen with different turn-on times (t_{ON}). The versions for headphone applications feature a t_{ON} of 4.2ms while the version, intended for set-top-box applications, which needs to be pre-booked, feature a 130ms t_{ON}. An on-chip charge pump inverts the power-supply input, creating a negative rail. The output stage of the amplifier is powered between the positive input supply and the output of the charge pump. The bipolar supplies bias the output about ground, eliminating the need for large, distortion-introducing output coupling capacitors. The IC shutdowns and startups without click-pop noise.

The IC is available in a 3mm x 3mm, 16-pin QFN-PP and is specified over the extended -40°C to +85°C temperature range.

■ TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



■ TERMINAL FUNCTION

PIN	NAME	Description
1	PVDD	Charge-Pump Power-Supply Input. Bypass to PGND with 1μF.
2	C1P	Positive Flying Capacitor Connection. Connect a 1μF capacitor between C1P and C1N.
3	PGND	Power Ground. Connect PGND and SGND together at the system ground plane.
4	C1N	Negative Flying Capacitor Connection. Connect a 1μF capacitor between C1P and C1N.
5	PVSS	Negative Charge-Pump Output. Bypass to PGND with 1μF.
6	SGND	Signal Ground. Connect PGND and SGND together at the system ground plane.
7	INR+	Right Positive Polarity Input
8	INR-	Right Negative Polarity Input
9	SVDD2	Signal Path Power-Supply Input. Connect directly to PVDD.
10	OUTR	Right Direct Drive Output
11	BIAS	Internal Supply Node. Bypass to PGND with 0.1μF.
12	OUTL	Left Direct Drive Output
13	SVDD	Signal Path Power-Supply Input. Bypass to PGND with 1μF. Connect directly to PVDD.
14	INL-	Left Negative Polarity Input
15	INL+	Left Positive Polarity Input
16	nSHDN	Active-Low Shutdown. Drive nSHDN high for normal operation.
__	EP	Exposed Pad. Electrically connect to PGND or leave unconnected.

■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	MOQ/Shipping Package
HT97180SQER	QFN16L-PP	HT97180 UVWXYZ *1	-40℃～85℃	Tape & Reel 5000PCS
HT97180LSQER	QFN16L-PP	HT97180 UVWXYZ *1	-40℃～85℃	Tape & Reel 5000PCS

*1 WXYZ/UVWXYZ is production track code.

■ ELECTRICAL CHARACTERISTIC

● Absolute Maximum Ratings*2

PARAMETER*3	Symbol	MIN	MAX	UNIT
Supply Voltage (SVDD, SVDD2, PVDD) Range	V_{DD}	-0.3	+5.5	V
PVSS and BIAS Voltage Range		-5.5	+0.3	V
SGND Voltage Range	SGND	-0.3	+0.3	V
Input (INL+, INL-, INR+, INR-) Voltage Range	V_{IN}	$-V_{SVDD}/2$	$+V_{SVDD}/2$	V
Input (nSHDN) Voltage Range	nSHDN	-0.3	+5.5	V
Output (OUTL, OUTR) Voltage Range	V_{OUT}	-5	5	V
C1P Voltage Range	C1P	-0.3	V_{PVDD}+0.3	V
C1N Voltage Range	C1N	V_{PVSS}	+0.3	V
Operating temperature range	TA	-40	85	℃
Operating junction temperature range	TJ	-40	150	℃
Storage temperature range	TSTG	-65	150	℃

*2 Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

*3 All Voltages is referenced to PGND.

● Electrical Characteristics*4

Condition: Ta=25°C, V_{DD} (= V_{PVDD} = V_{SVDD} = V_{SVDD2}) = 3.6V, V_{PGND} = V_{SGND} = 0V, R_{IN} = R_F = 20kΩ, C_{FLY} = 1uF, C_{PVDD} = C_{PVSS} = 1uF, C_{BIAS} = 0.1uF, RL=32R,unless otherwise specified.

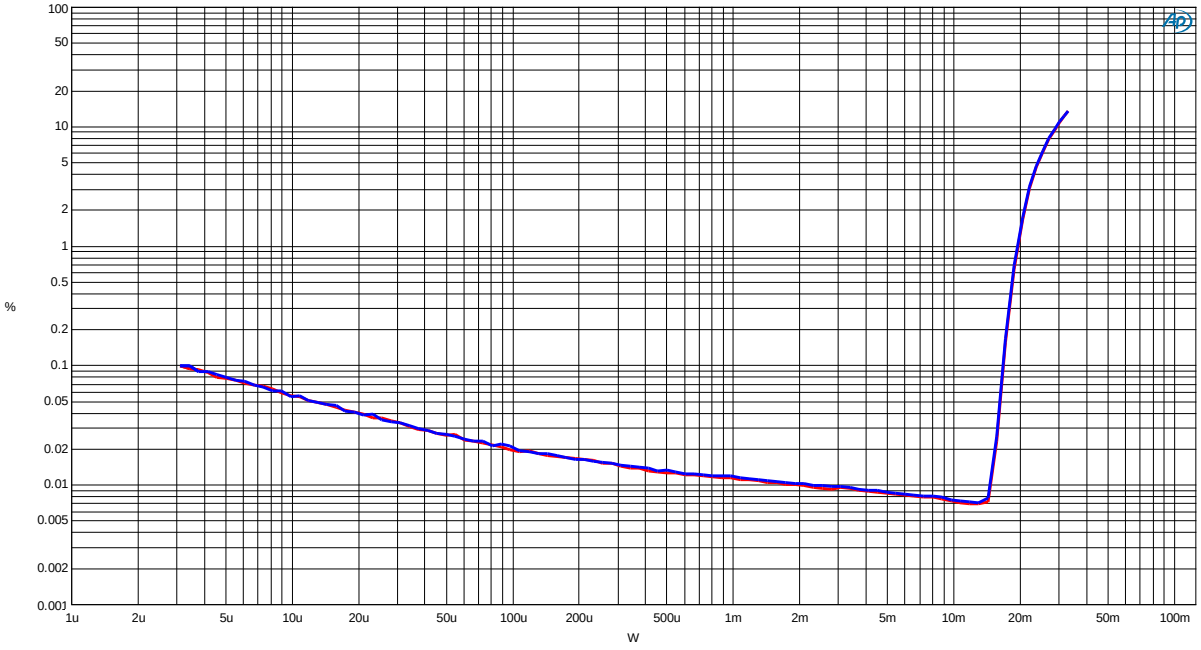
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage range	V_{DD}		1.65		4.8	V
Quiescent Supply Current	I_{DD}	No Load		2.7		mA
Under-voltage Lockout	UVLO				1.6	V
Shutdown Supply Current	I_{SD}	nSHDN = 0		0.1		uA
Start-up time	t_{ON}	Power on, or pull nSHDN to high		4.2		ms
Amplifier						
Output Offset Voltage	V_{OS}	HT97180			500	uV
		HT97180L		1		mV
Input Common-Mode Voltage Range	V_{CM}	Voltage at IN+ and IN-	-0.5 x V_{PVDD}		+0.5 x V_{PVDD}	V
Maximum Differential Input Signal	V_{DIFF}				V_{PVDD}	V_P
Power-Supply Rejection Ratio	PSRR	V_{DD} = from 1.65V to 4.8V		85		dB
		f_{IN} = 217Hz, 200mVpp		78		
		f_{IN} = 10kHz, 200mVpp		63		

Common-Mode Rejection Ratio	CMRR	$-V_{PVDD}/2 \le V_{CM} \le +V_{PVDD}/2$		86		dB
Output Power	P_{OUT}	VDD = 1.8V, R_L = 32Ω, THD+N = 1%		18.5		mW
		VDD = 3.3V, R_L = 32Ω, THD+N = 1%		80		mW
		VDD = 4.2V, R_L = 32Ω, THD+N = 1%		135		
Total Harmonic Distortion Plus Noise	THD+N	VDD=1.8V,1kHz, 22Hz to 22kHz BW, P_{OUT} = 10mW, R_L = 32Ω		0.007		%
		VDD=3.6V,1kHz, 22Hz to 22kHz BW, P_{OUT} = 20mW, R_L = 32Ω		0.005		%
		VDD=3.6V,1kHz, 22Hz to 22kHz BW, V_{OUT} = 1.0V, R_L = 3kohm		0.002		%
Signal-to-Noise Ratio	SNR	P_{OUT} = 20mW, 22Hz to 22kHz BW, A-weighted, R_L = 32Ω		98		dB
Output Noise Voltage	V_N	A-weighted, RIN = RF = 10kΩ		8		uV
CrossTalk	CT	1kHz, P_{OUT} = 20mW, RL = 32Ω		-88		dB
		10kHz, P_{OUT} = 20mW, RL = 32Ω		-68		
Maximum Capacitive Load Drive	CL			470		pF
External Feedback Resistor Range	R_F		4.7	20	100	kΩ
Oscillator Frequency	f_{OSC}		450	500	550	kHz
Logic Input						
nSHDN Input Logic High	V_{IH}		1			V
nSHDN Input Logic Low	V_{IL}	Input Grounded, With or without load			0.4	V

*4: Depending on parts and PCB layout, characteristics may be changed.

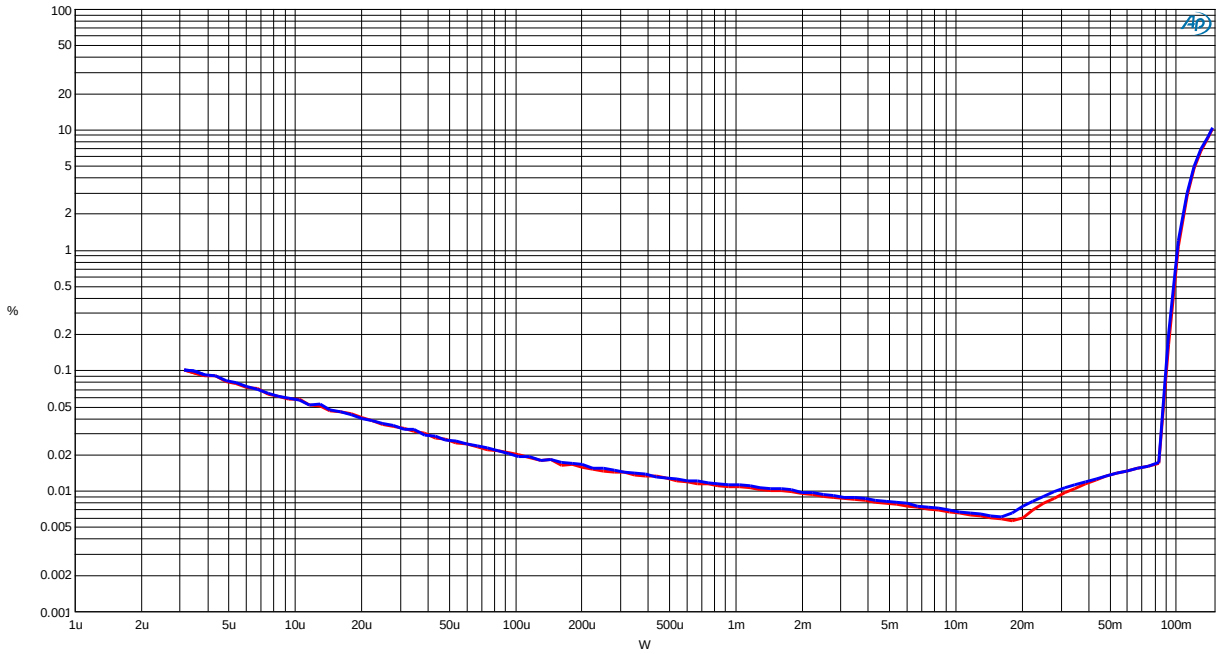
■ TYPICAL OPERATING CHARACTERISTICS

Condition: Ta=25°C, V_{DD} (= V_{PVDD} = V_{SVDD} = V_{SVDD2}) = 3.6V, V_{PGND} = V_{SGND} = 0V, R_{IN} = R_F = 20kΩ, C_{IN} = 1uF,C_{FLY} = C_{PVDD} = C_{PVSS} = 1uF, C_{BIAS} = 0.1uF,RL=32R, fin=1kHz, unless otherwise specified.



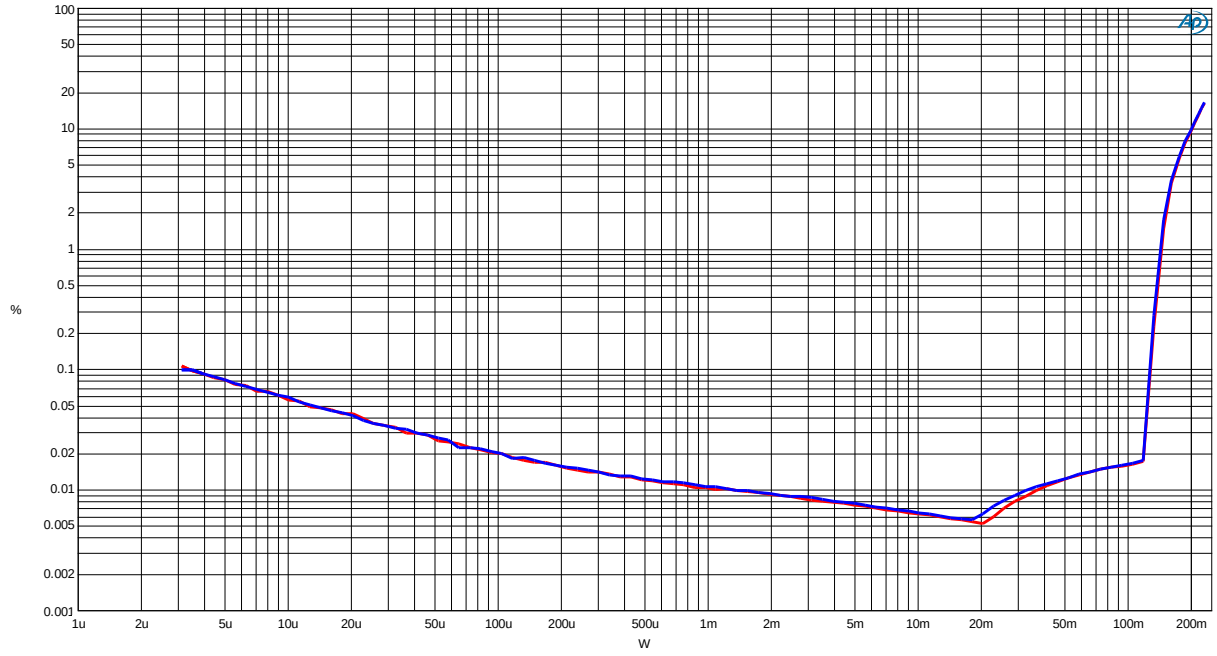
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	
1	3	Blue	Solid	3	Analyzer.THD+N Ratio B	Left	

Po vs THD+N(VDD=1.8V)



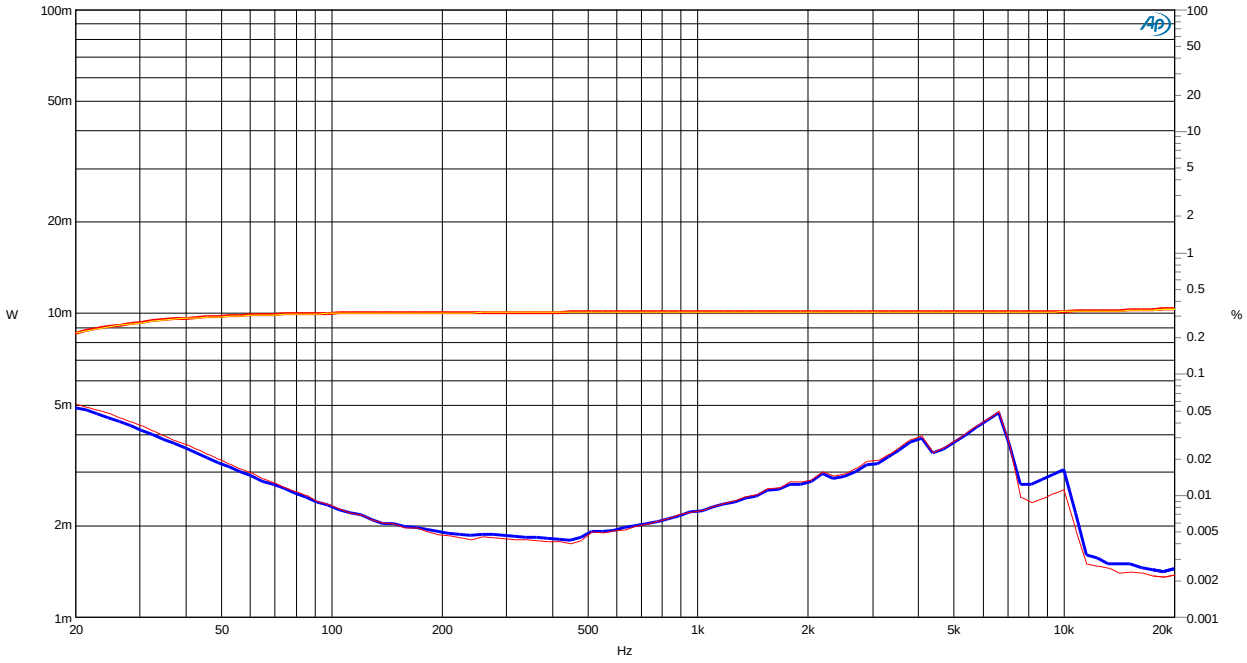
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	
1	3	Blue	Solid	3	Analyzer.THD+N Ratio B	Left	

Po vs THD+N(VDD=3.6V)



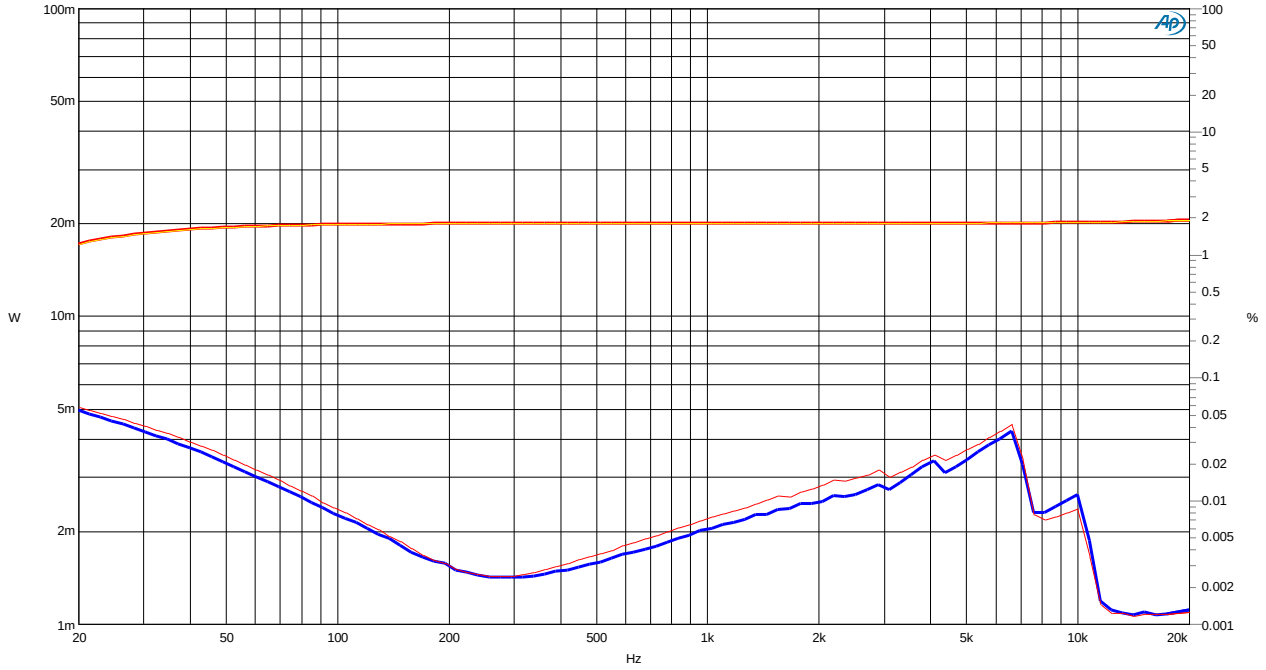
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Analyzer.THD+N Ratio A	Left	
1	3	Blue	Solid	3	Analyzer.THD+N Ratio B	Left	

Po vs THD+N(VDD=4.2V)



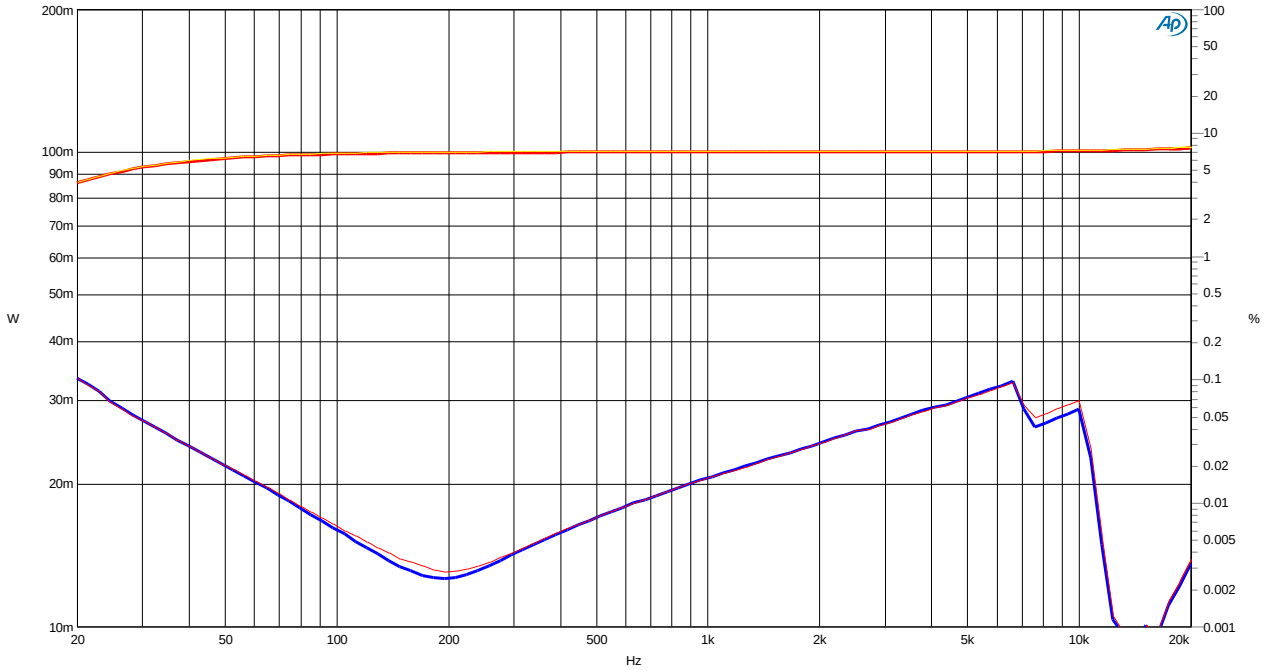
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Analyzer.Level A	Left	
1	2	Blue	Solid	3	Analyzer.THD+N Ratio A	Right	
1	3	Yellow	Solid	1	Analyzer.Level B	Left	

fin vs THD+N(VDD=1.8V, Po=10mW)



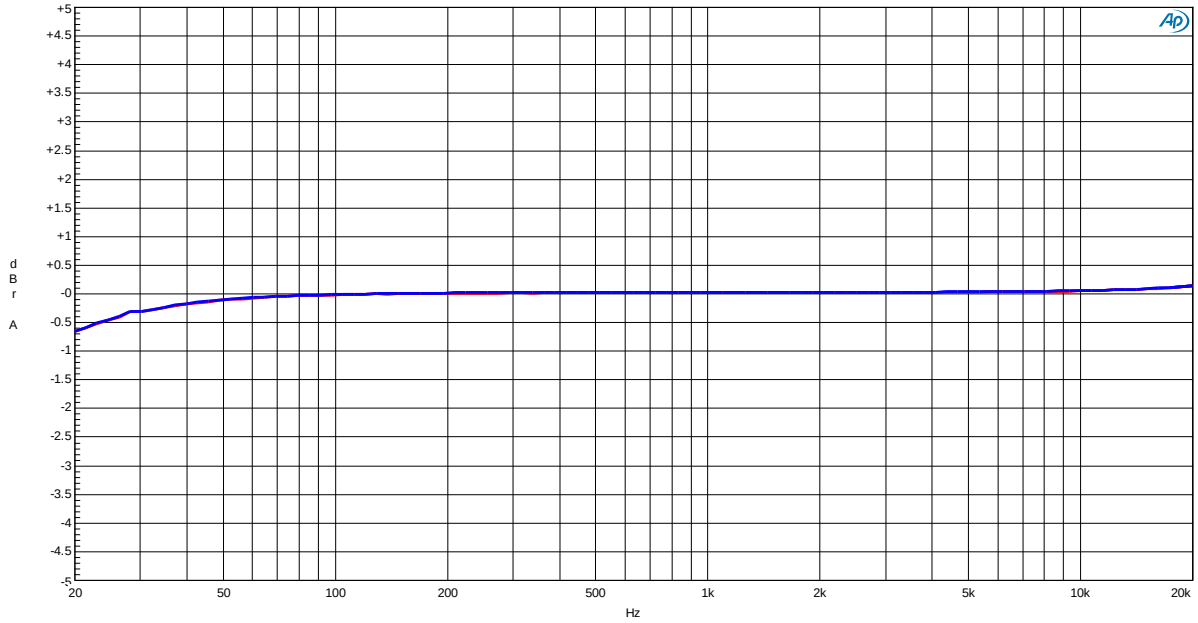
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Analyzer.Level A	Left	
1	2	Blue	Solid	3	Analyzer.THD+N Ratio A	Right	
1	3	Yellow	Solid	1	Analyzer.Level B	Left	

fin vs THD+N(VDD=3.6V, Po=20mW)



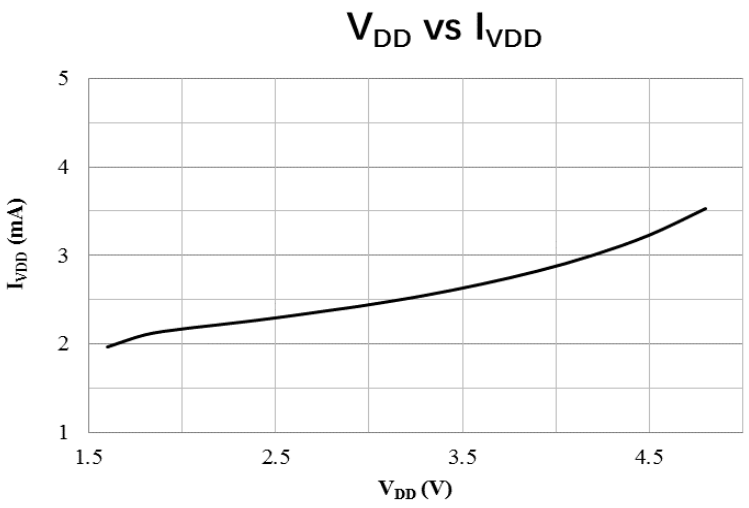
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Analyzer.Level A	Left	
1	2	Blue	Solid	3	Analyzer.THD+N Ratio A	Right	
1	3	Yellow	Solid	1	Analyzer.Level B	Left	

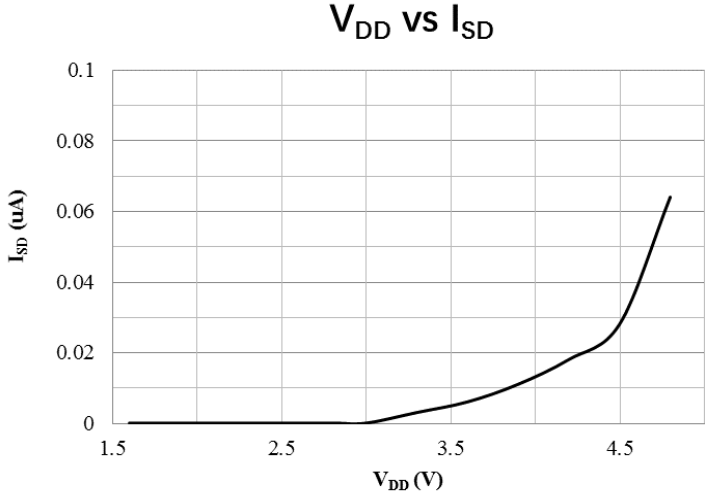
fin vs THD+N(VDD=4.2V, Po=100mW)



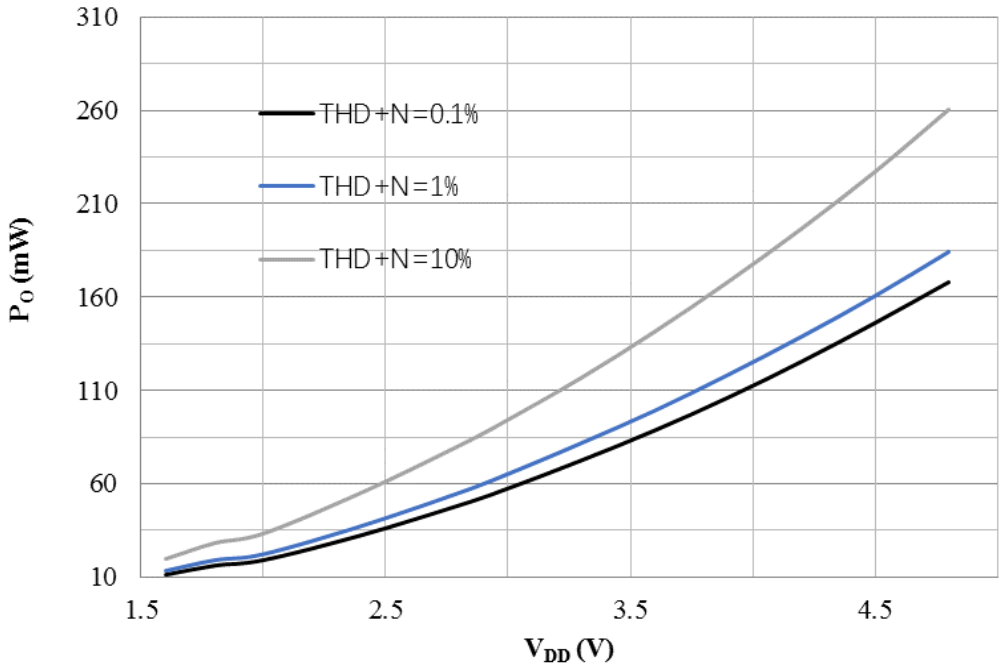
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Analyzer.Level A	Left	
1	2	Blue	Solid	3	Analyzer.Level B	Left	

Fin vs GAIN

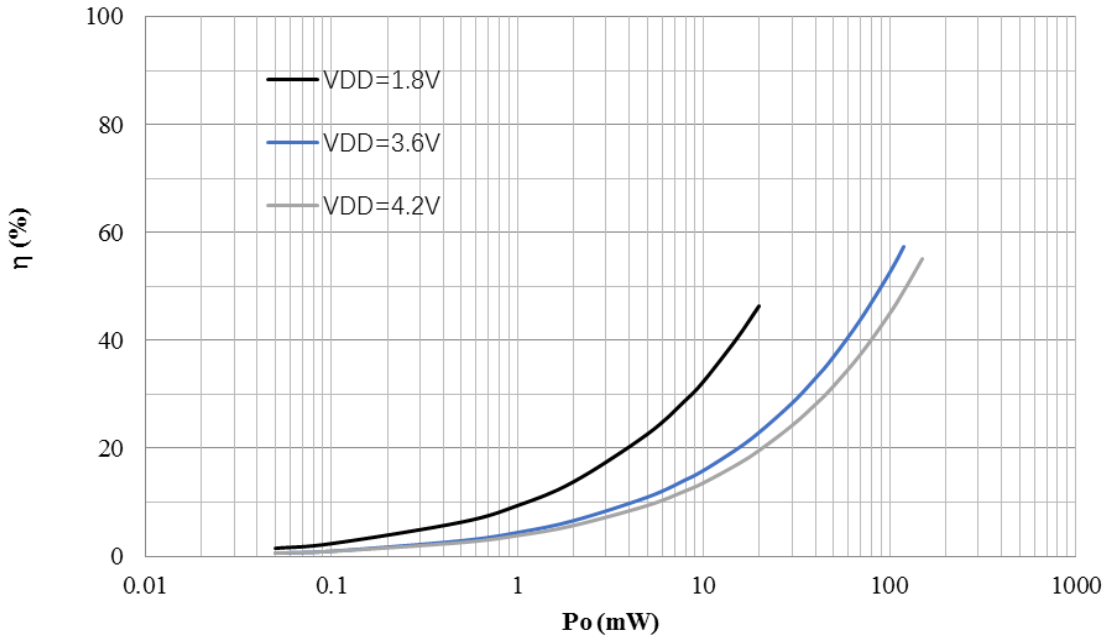




V_{DD} vs P_O



Po vs η

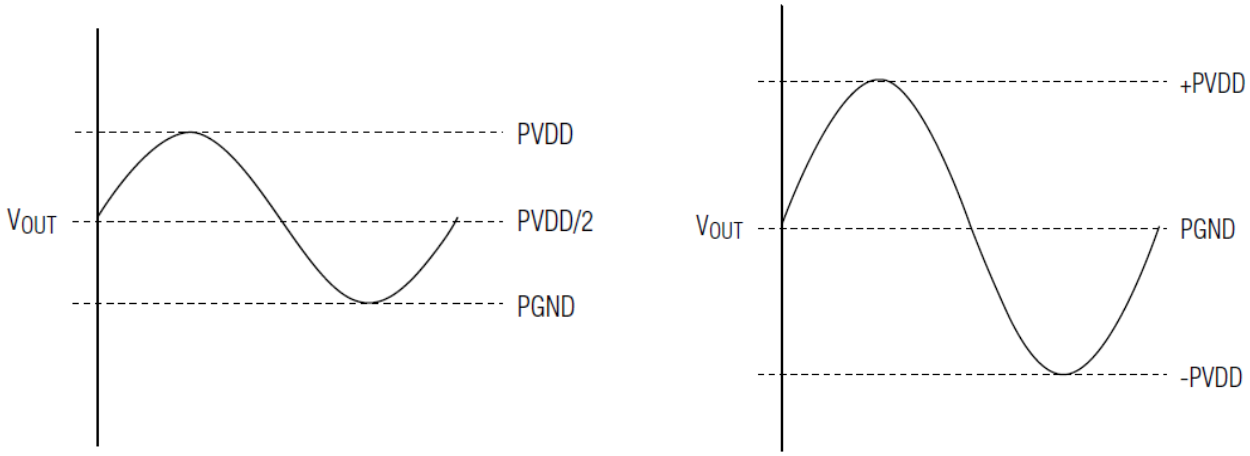


■ APPLICATION INFORMATION

1. Detailed Description

The HT97180(L) is a fully differential input line driver/ headphone amplifier for set-top boxes, LCD TV, and home theater applications where audio fidelity is of primary importance. Power consumption of the amplifier is reduced while maintaining high SNR and THD+N performance. The HT97180(L) require external input and feedback resistors to set amplifier gain. For internal fixed gain of +6dB, it is only available if pre-booked.

The HT97180(L) operates from a single supply ranging from 1.65V to 4.8V. An on-chip charge pump inverts the positive supply (PVDD), creating an equal magnitude negative supply (PVSS). The headphone amplifiers operate from bipolar supplies with their outputs biased about PGND (Figure 1). The benefit of this PGND bias is that the amplifier outputs do not have a DC component, typically PVDD/2. The large DC-blocking capacitors required with conventional headphone amplifiers are unnecessary, thus conserving board space, reducing system cost, and improving frequency response. Output power of 125mW into 32Ω is achievable from a 4.2V supply. The device features an under-voltage lockout that prevents operation from an insufficient power supply and click-pop suppression that eliminates audible transients on startup and shutdown.



Conventional Driver-Basing Scheme Direct Drive Biasing Scheme

Fig. 1 Conventional Driver Output Waveform vs. HT97180(L) Output Waveform

2. Differential Input or Single-Ended Input

The IC can be configured as differential or single-ended input amplifiers (Figures 2 and 3), making it compatible with all codecs. A differential input offers improved noise immunity over a single-ended input. In devices such as cellular phones, high-frequency signals from the RF transmitter can couple into the amplifier's input traces. The signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs while signals common to both inputs are cancelled. The gain of the HT97180(L) is set by:

$$A_V = R_F/R_{IN}$$

The common-mode rejection ratio (CMRR) is limited by the external resistor matching, and if used, input capacitor matching at low frequencies. For example, the worst-case variation of 1% tolerant resistors results in 40dB CMRR, while 0.1% resistors result in 60dB CMRR. For best matching, use resistor arrays.

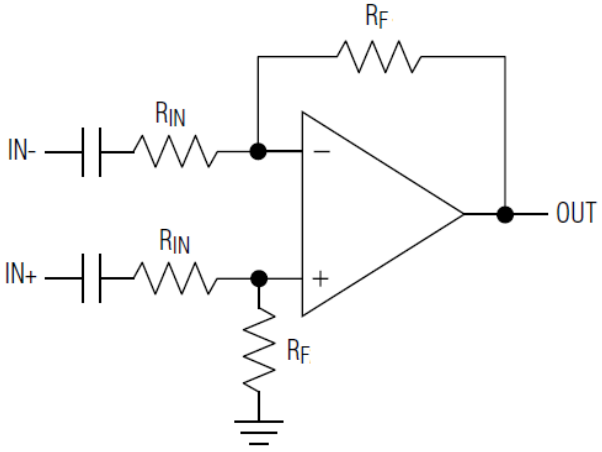


Fig. 2 Differential Input Configuration

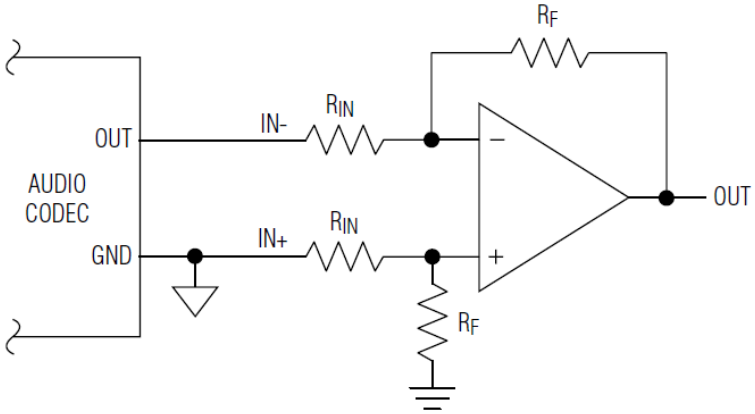


Fig. 3 Single-ended Input Configuration

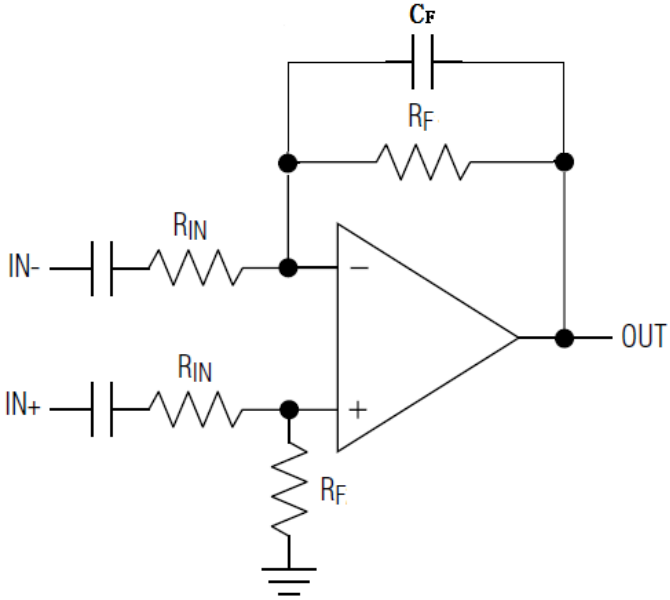


Fig. 4 Add CF to keep system stable

The headphone has parasitic capacitance and If the parasitic capacitance is bigger than a certain value, it may cause the system out of stable. Fig. 4 shows that a capacity CF parallel with RF to keep the system more stable. Generally, a 6.8pF capacity is enough. However, if headphone's parasitic capacitance is very big, for example

bigger than 1nF，a bigger capacitance CF is needed. The CF can be 47pF or 68pF according to headphone's parasitic capacitance.

3. Direct Drive

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and the headphone amplifier.

HT97180(L) uses a charge pump to create an internal negative supply voltage, allowing the IC's outputs to be biased about PGND. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220uF, typ.) tantalum capacitors, the IC charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier.

4. Input Filters

In addition to the cost and size disadvantages of DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal.

If input capacitors are used, input capacitor C_{IN}, in conjunction with input resistor R_{IN}, forms a high-pass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the high-pass filter is given by:

$$f_{-3dB} = 1/(2\pi R_{IN} C_{IN})$$

Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors with adequately low voltage coefficients, such as X7R ceramic capacitors with a high voltage rating. Capacitors with higher voltage coefficients result in increased distortion at low frequencies.

5. Bias Capacitor

Bypass BIAS with a 0.1uF capacitor to PGND. Do not connect external loads to BIAS.

6. Charge Pump

The HT97180(L) features a low-noise charge pump. The 500kHz switching frequency is well beyond the audio range and, thus, does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. The IC requires a 1uF flying capacitor between C1P and C1N and a 1uF hold capacitor from PVSS to PGND.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

The value of the flying capacitor (C_{FLY}) affects the charge pump's load regulation and output resistance. A C_{FLY} value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C_{FLY} improves load regulation and reduces the charge-pump output

resistance to an extent. Above 1uF, the on-resistance of the switches and the ESR of CFLY and CPVSS dominate.

The hold capacitor value and ESR directly affect the ripple at PVSS. Use a low-ESR 1uF capacitor for C_{PVSS}.

7. Click-pop Suppression

The IC features click-pop suppression circuitry. When entering shutdown, the amplifier outputs are high impedance to ground. This scheme minimizes the energy present in the audio band.

8. Shutdown

The IC features a 1uA lower low-power shutdown mode that reduces power consumption. When the active-low shutdown mode is entered, the device's internal bias circuitry is disabled, the amplifier outputs go high impedance, and BIAS is driven to PGND. The HT97180(L) inputs are driven to PGND.

9. Amplifier Gain

The gain of the HT97180(L) amplifier is set externally. The gain is:

$$A_V = -R_F/R_{IN}$$

Choose feedback resistor values between the 4.7kΩ and 100kΩ range.

There's another version of HT97180(L) that has an internally fixed 6dB gain needs to be pre-booked.

10. Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Connect a 1uF ceramic capacitor from PVDD to PGND and a 1uF ceramic capacitor from SVDD to PGND. Add additional bulk capacitance as required by the application. Locate the bypass capacitor as close as possible to the device.

11. PCB Layout and Grounding

Good PCB layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and route heat away from the device. Good grounding improves audio performance, and prevents any digital switching noise from coupling into the audio.

Connect PGND and SGND together at a single point on the PCB. Connect all components associated with the charge pump (C_{FLY} and C_{PVSS}) to the PGND plane. Connect PVDD and SVDD together at the device. Place capacitors CFLY and CPVSS as close as possible to the device. Ensure the PCB layout is partitioned so that the large switching currents in the ground plane do not return through SGND and the traces and components in the audio signal path.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes. Also, ensure a solid ground plane is used in multilayer PCB designs.

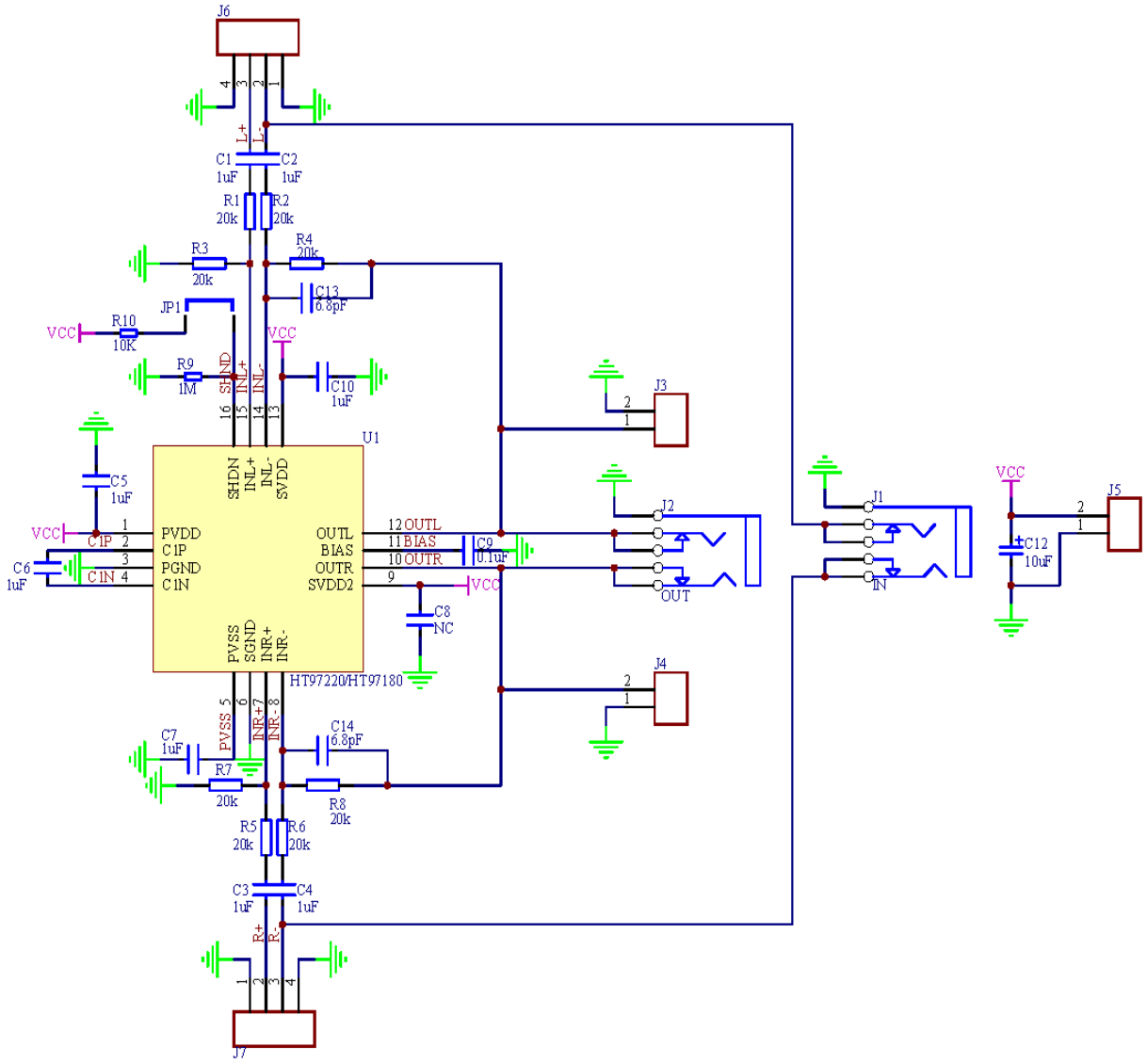


Fig.5 Typical Application of HT97180(L) Demo

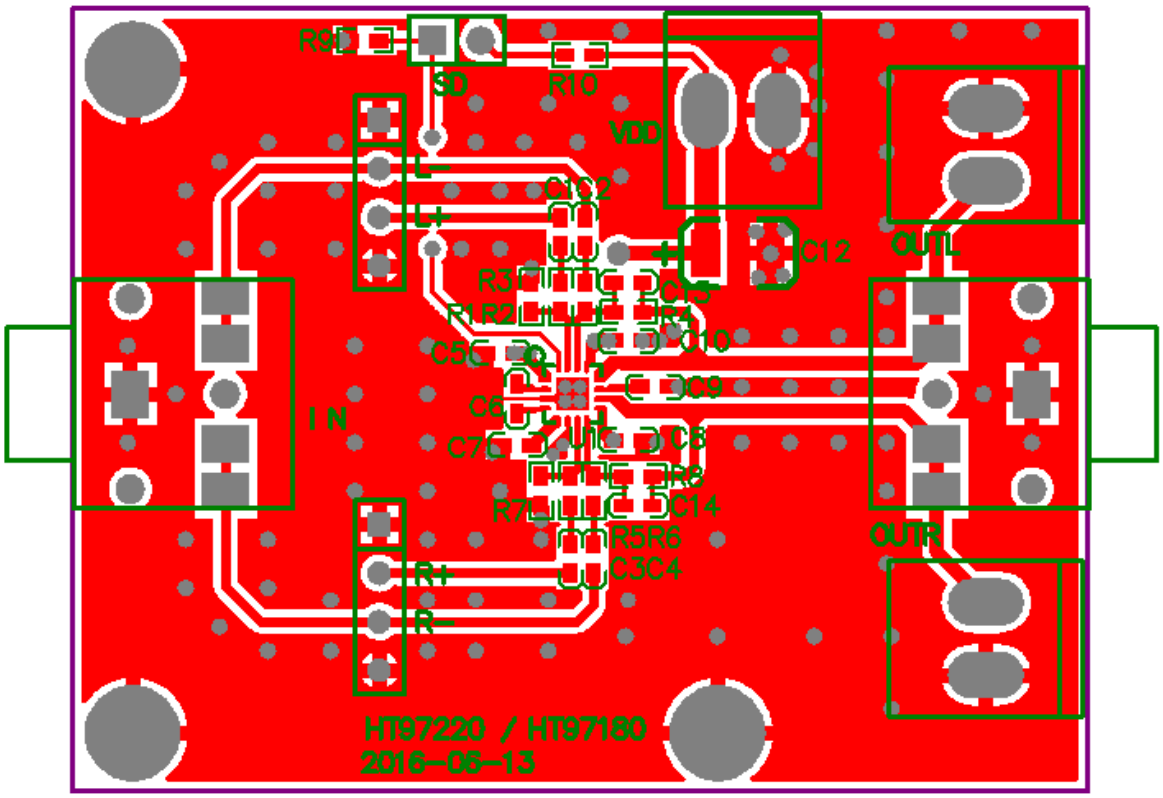


Fig.6 Top View of HT97180(L) Demo Board PCB Layout

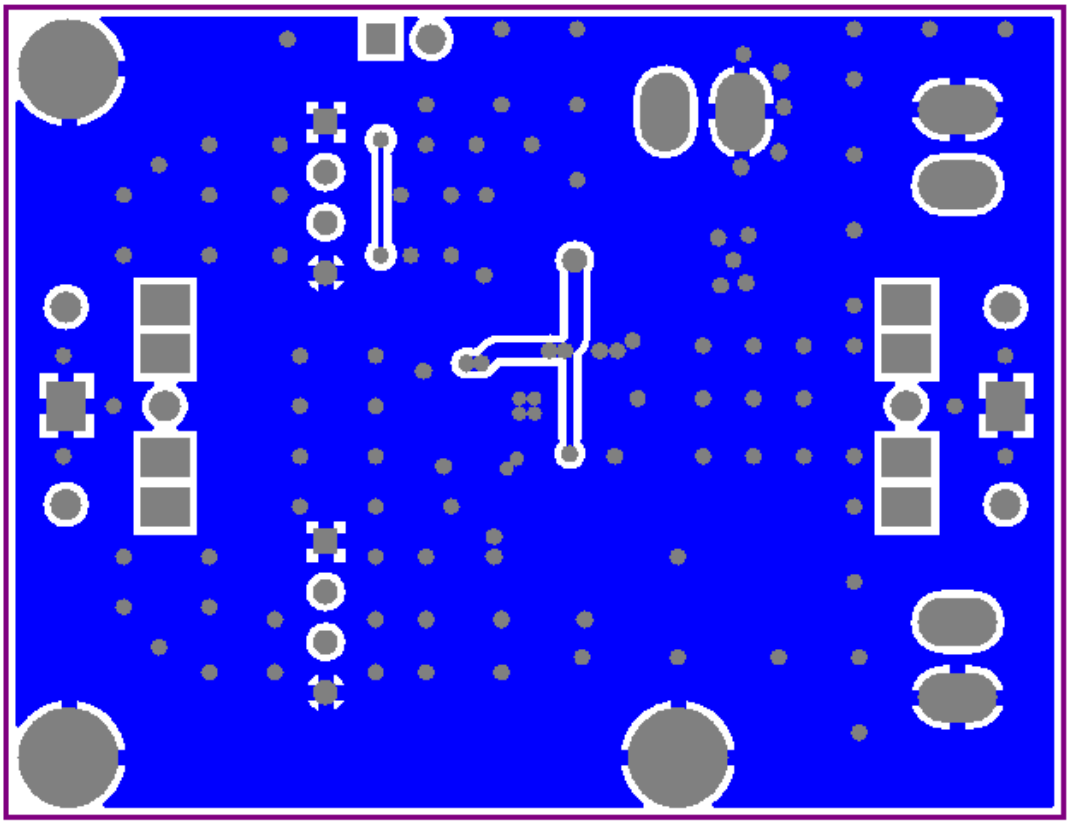
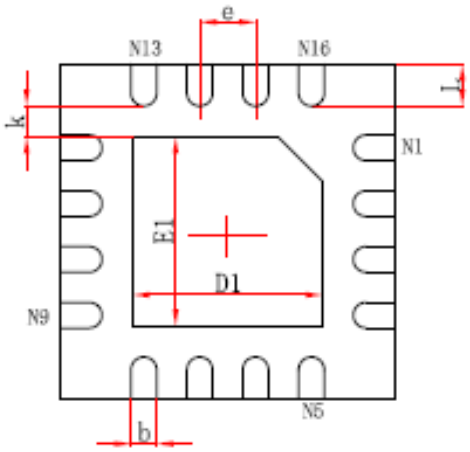
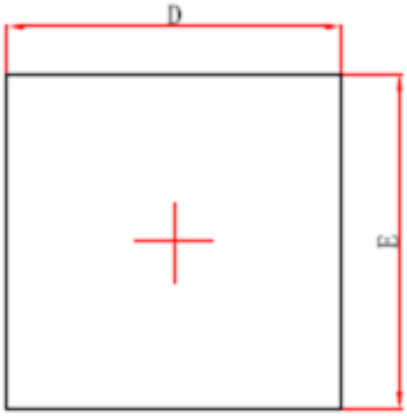
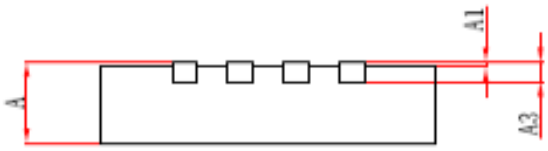


Fig.7 Bottom View of HT97180(L) Demo Board PCB Layout

■ PACKAGE OUTLINE







Symbol	Dimension in Millimeters (mm)	
	Min.	Max.
A	0.700	0.900
A1	0.000	0.050
A3	0.203(REF)	
D	2.900	3.100
E	2.900	3.100
D1	1.600	1.800
E1	1.600	1.800
k	0.200MIN	
b	0.180	0.300
e	0.500TYP	
L	0.300	0.500

IMPORTANT NOTICE

注意

Jiaxing Heroic Electronic Technology Co., Ltd (HT) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any products or services. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

嘉兴禾润电子科技有限公司（以下简称HT）保留对产品、服务、文档的任何修改、更正、提高、改善和其他改变，或停止提供任何产品和服务的权利。客户在下单和生产前应确保所得到的信息是最新、最完整的。

HT assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using HT components.

HT对相关应用的说明和协助以及客户产品的板级设计不承担任何责任。

HT products are not authorized for use in safety-critical applications (such as life support devices or systems) where a failure of the HT product would reasonably be expected to affect the safety or effectiveness of that devices or systems.

HT的产品并未授权用于诸如生命维持设备等安全性极高的应用中。

The information included herein is believed to be accurate and reliable. However, HT assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

本文中的相关信息是精确和可靠的，但HT并不对其负责，也不对任何可能的专利和第三方权利的侵害负责。

Following are URLs and contacts where you can obtain information or supports on any HT products and application solutions:

下面是可以联系到我公司的相关链接和联系方式：

深圳市宝华龙科技有限公司　叶生　13713725986