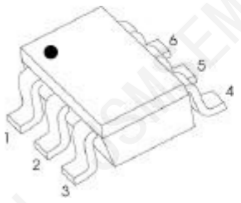
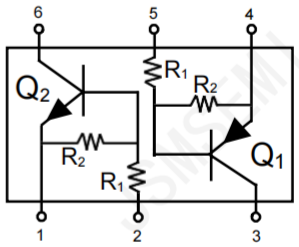
The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base–emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the PUMD3,115-JSM, two complementary BRT devices are housed in the SOT–363 package which is ideal for low power surface mount applications where board space is at a premium.



SOT-363

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- We declare that the material of product compliance with RoHS requirements.



MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	187 (Note 1.) 256 (Note 2.) 1.5 (Note 1.) 2.0(Note 2.)	mW mW/°C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1.) 490 (Note 2.)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	250 (Note 1.) 385 (Note 2.) 2.0 (Note 1.) 3.0(Note 2.)	mW mW/°C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1.) 325 (Note 2.)	°C/W
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	188 (Note 1.) 208 (Note 2.)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

1. FR–4 @ Minimum Pad
2. FR–4 @ 1.0 x 1.0 inch Pad

ORDERING, SHIPPING, DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1(K)	R2(K)	Shipping
PUMD3,115-JSM	SOT-363	11	10	10	3000/Tape&Reel

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	I_{EBO}	–	–	0.5	mAdc
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

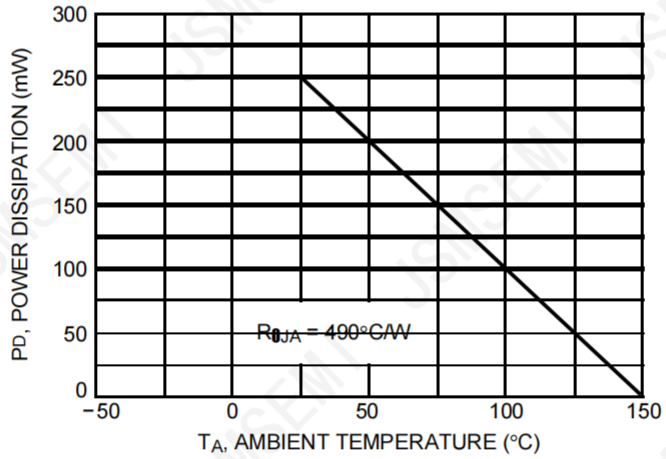


Figure 1. Derating Curve

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q1 (PNP) omitted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)					
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	h_{FE}	35	60	–	
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA) (I_C = 10 mA, I_B = 5 mA) (I_C = 10 mA, I_B = 1 mA)	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kfi) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kfi)	V_{OL}	–	–	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kfi) (V_{CC} = 5.0 V, V_B = 0.050 V, R_L = 1.0 kfi) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kfi)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	7.0	10	13	k fi
Resistor Ratio	R1/R2	0.8	1.0	1.2	

TYPICAL ELECTRICAL CHARACTERISTICS − PUMD3,115-JSM NPN TRANSISTOR

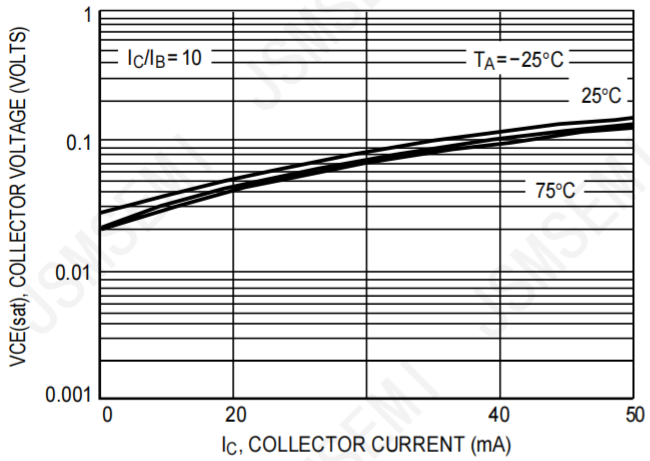


Figure 2. $V_{CE(sat)}$ versus I_C

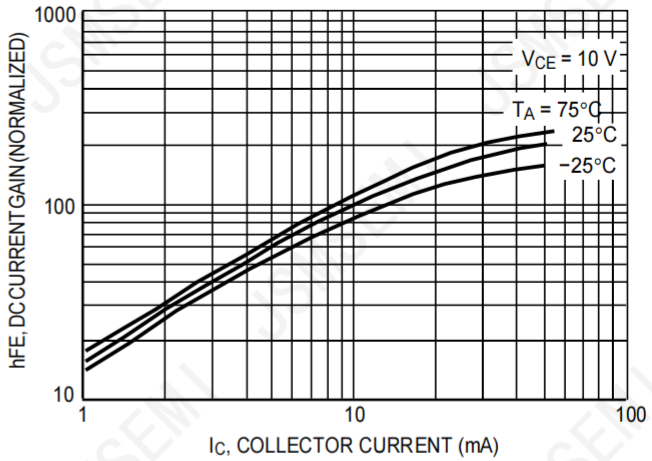


Figure 3. DC Current Gain

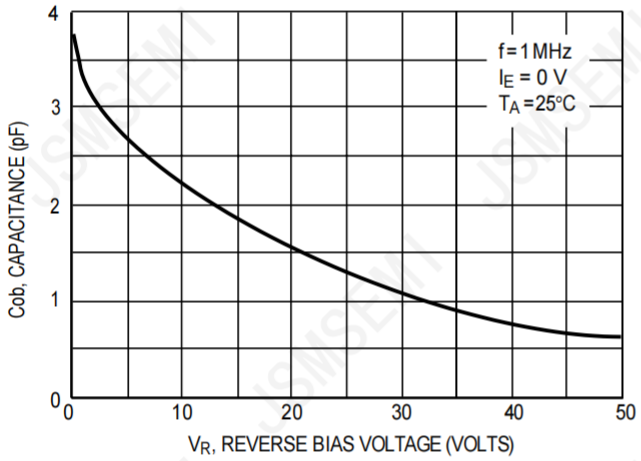


Figure 4. Output Capacitance

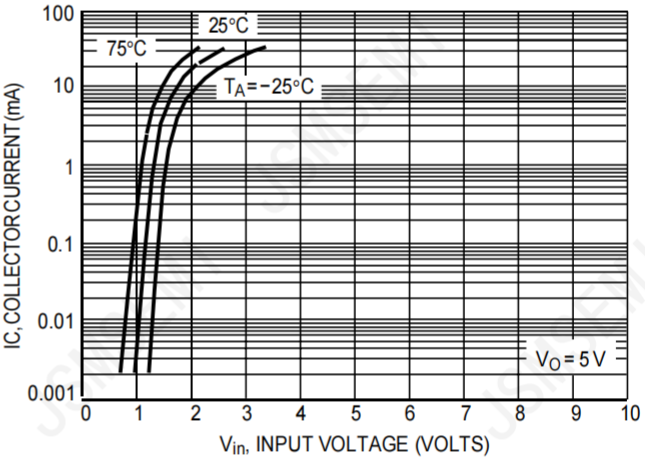


Figure 5. Output Current versus Input Voltage

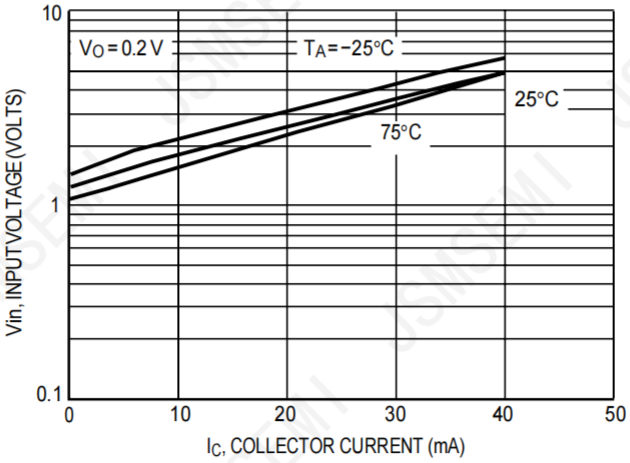


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS – PUMD3,115-JSM PNP TRANSISTOR

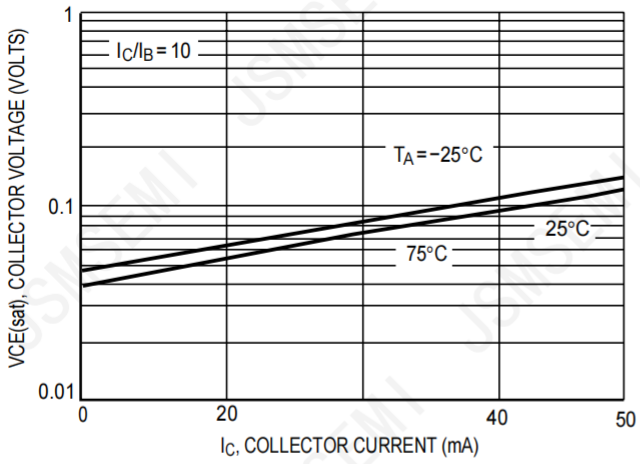


Figure 7. $V_{CE(sat)}$ versus I_C

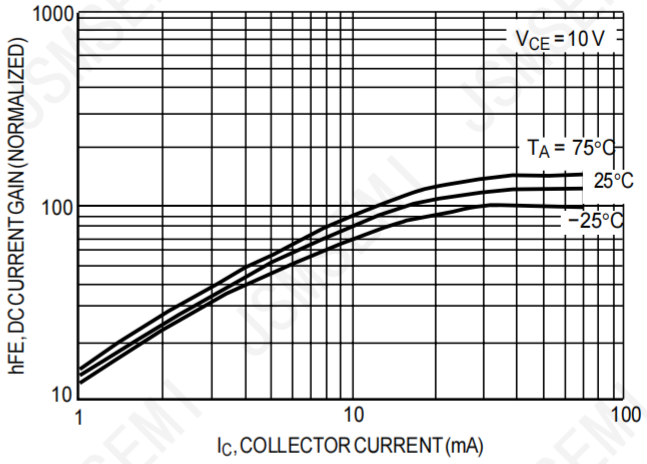


Figure 8. DC Current Gain

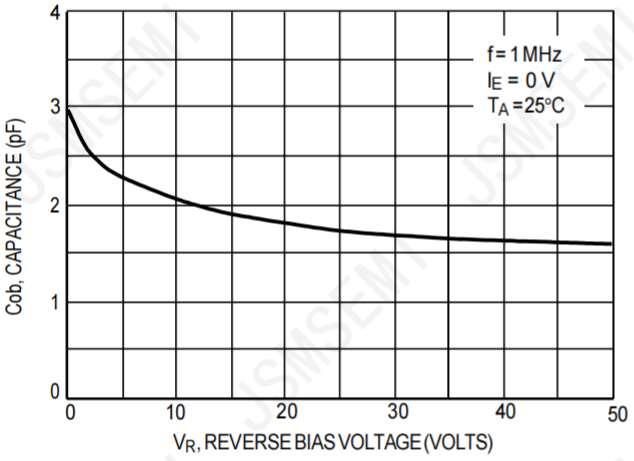


Figure 9. Output Capacitance

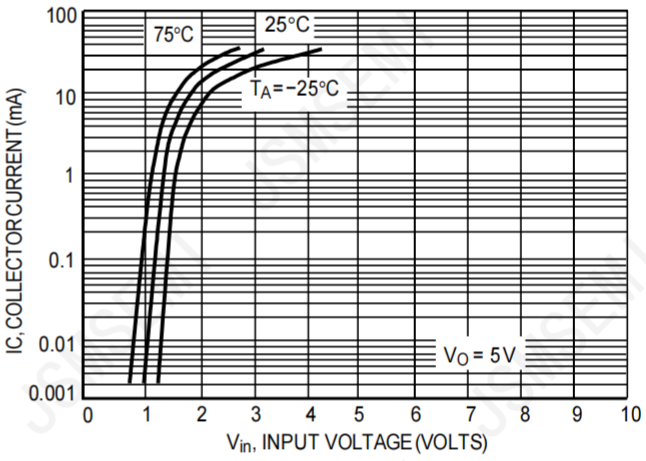


Figure 10. Output Current versus Input Voltage

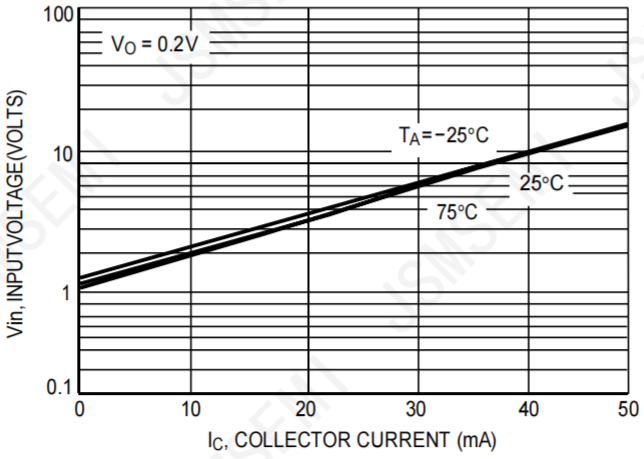
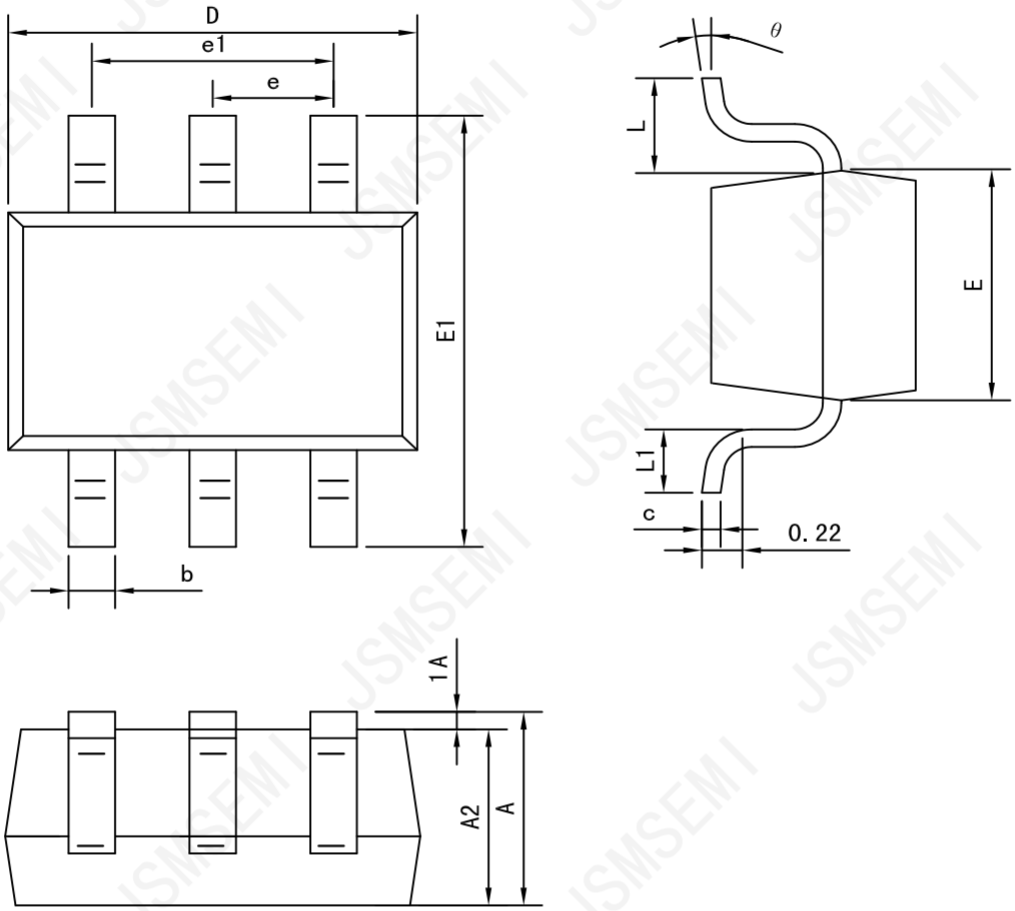


Figure 11. Input Voltage versus Output Current

Package Information

SOT-363



Symbol	Dimension in Millimeters	
	Min	**Max**
A	0.900	1.100
A1	0.000	0.100
A2	0.900	1.000
b	0.150	0.350
c	0.080	0.150
D	2.000	2.200
E	1.150	1.350
E1	2.150	2.450
e	0.650 TYP	
e1	1.200	1.400
L	0.525 REF	
L1	0.260	0.460
θ	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	2/23/2024

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER’S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc.When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com