

N-Channel 80V MOSFET

E080N020HL1

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
80V	20 @ $V_{GS} = 10V$	35

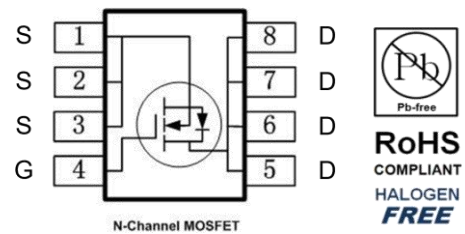
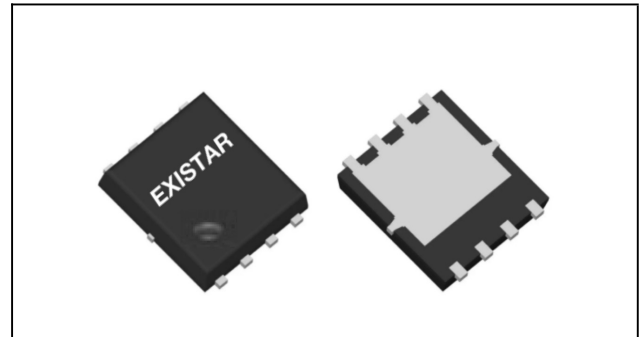
Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- PD charger
- Moto driver

PDFN5X6



Package And Ordering Information

Ordering code	Package	Marking
E080N020HL1	PDFN5x6	E080N020HL1

Ordering Information

Package	Units/ Reel	Reels/ Inner Box	Units/ Inner Box
PDFN5x6	5000	1	5000

Key Performance Parameters

Parameter	Value	Unit
V _{DS} , min @ T _j (max)	80	V
I _D , pulse	140	A
R _{DS(ON)} , max @ V _{GS} =10V	20	mΩ
Q _g	13	nC

Absolute Maximum Ratings at T_j=25°C Unless Otherwise Noted

Parameter		Symbol	Limit	Unit
Drain-source voltage		V _{DS}	80	V
Gate-source voltage		V _{GS}	±20	
Continuous drain current	T _C =25°C	I _D	35	A
	T _C =100°C		-	
Pulsed drain current		I _{D,pulse}	140	
Avalanche energy, single pulse		E _{AS}	22	mJ
Power dissipation	T _C =25°C	P _D	35	W
	T _A =25°C		-	
Operating junction and storage temperature range		T _J , T _{stg}	-55 To 175	°C

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	R _{θJC}	4.3	°C/W
Thermal resistance, junction-to-ambient	Steady state	R _{θJA}	62	

Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Drain to source breakdown voltage	V _{(BR)DSS}	80			V	V _{GS} = 0, I _D = 250 μA
Gate-source threshold voltage	V _{GS(th)}	1.3		2.0	V	V _{DS} = V _{GS} , I _D = 250 μA
Gate-body leakage	I _{GSS}			±100	nA	V _{DS} = 0 V, V _{GS} = ±20 V
Zero gate voltage drain current	I _{DSS}			1	μA	V _{DS} = 80 V, V _{GS} = 0 V
Drain-source on-resistance	R _{DS(on)}		15	20	mΩ	V _{GS} = 10 V, I _D = 12 A
Drain-source on-resistance	R _{DS(on)}		20	25	mΩ	V _{GS} = 4.5 V, I _D = 9 A
Forward transconductance	g _{fs}		-		S	V _{DS} = 5 V, I _D = 30 A

Gate resistance	R _g		2.8		Ω	f=1MHz
Gate Charge						
Total gate charge	Q _g		13		nC	V _{DS} = 40 V, I _D = 20 A, V _{GS} = 10 V
Gate-source charge	Q _{gs}		2.4			
Gate-drain charge	Q _{gd}		2.5			
Dynamic						
Turn-on delay time	t _{d(on)}		7		ns	V _{DS} = 40 V, I _D =20 A, V _{GS} = 10 V, R _{GEN} = 2 Ω
Rise time	t _r		4			
Turn-off delay time	t _{d(off)}		17			
Fall time	t _f		2.6			
Input capacitance	C _{iss}		792		pF	V _{DS} =25 V, V _{GS} = 0 V, f = 100kHz
Output capacitance	C _{oss}		342			
Reverse transfer capacitance	C _{rss}		29			
Body Diode						
Diode forward voltage	V _{SD}			1.3	V	V _{GS} = 0 V, I _S = 20 A
Reverse recovery time	t _{rr}		40		ns	V _R = 40 V, I _S =20 A, di/dt = 100 A/μs
Reverse recovery charge	Q _{rr}		35		nC	

Electrical Characteristics Diagrams

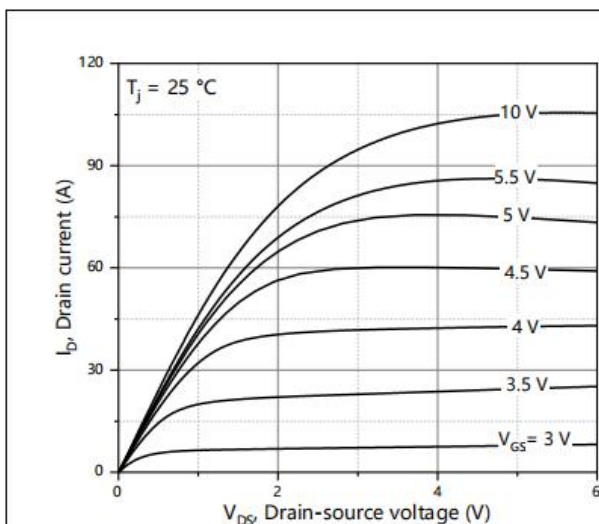


Figure 1. Typ. output characteristics

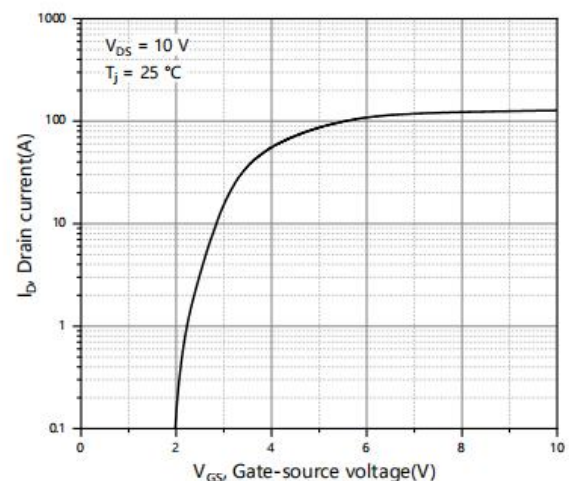


Figure 2. Typ. transfer characteristics

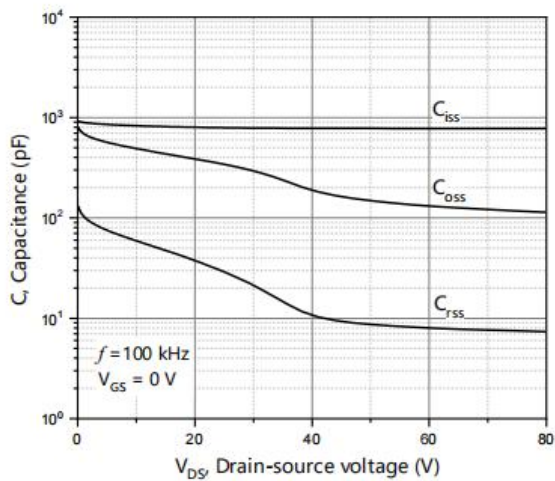


Figure 3. Typ. capacitances

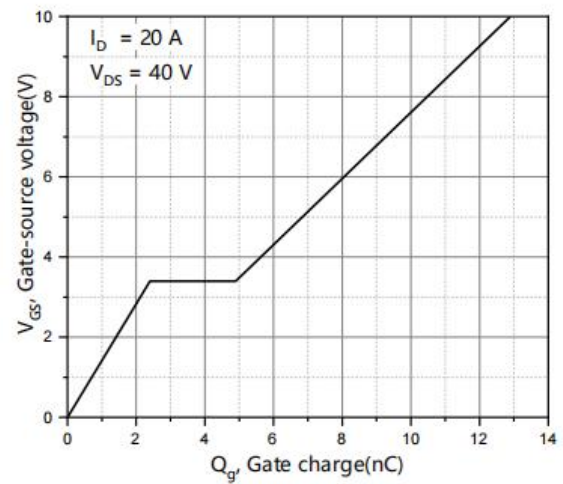


Figure 4. Typ. gate charge

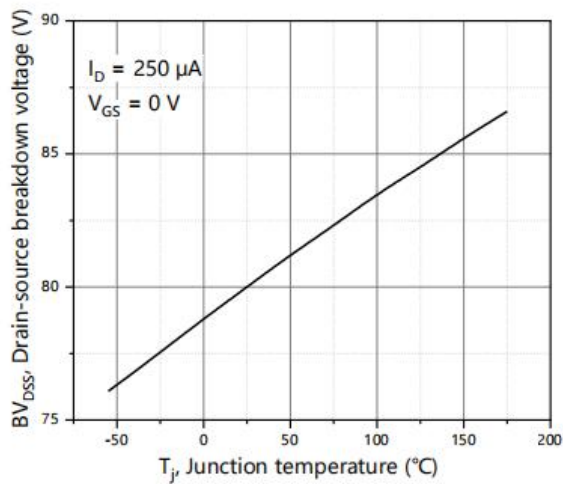


Figure 5. Drain-source breakdown voltage

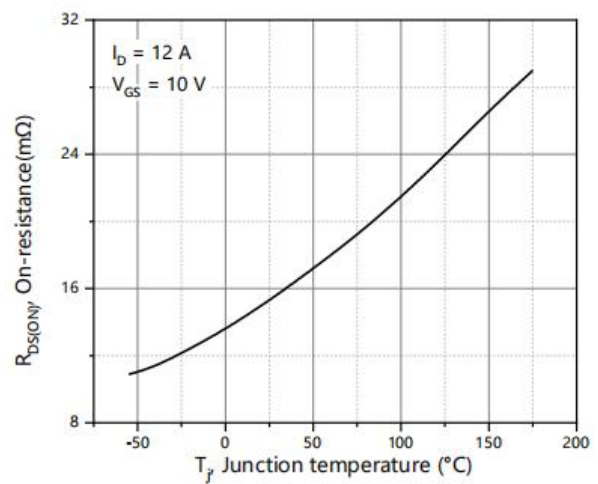


Figure 6. Drain-source on-state resistance

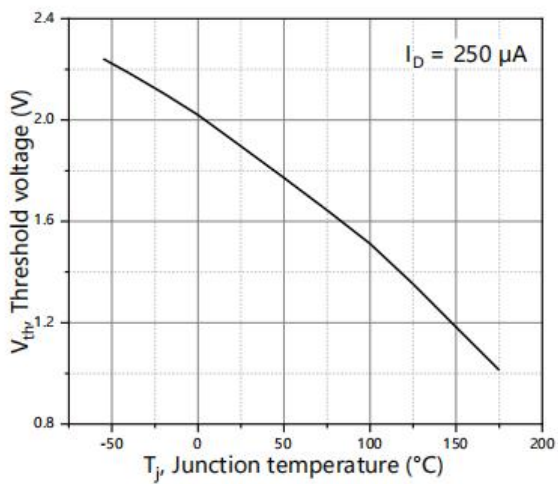


Figure 7. Threshold voltage

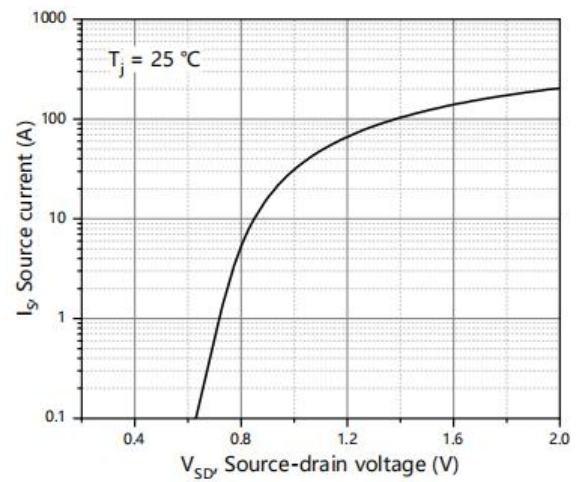


Figure 8. Forward characteristic of body diode

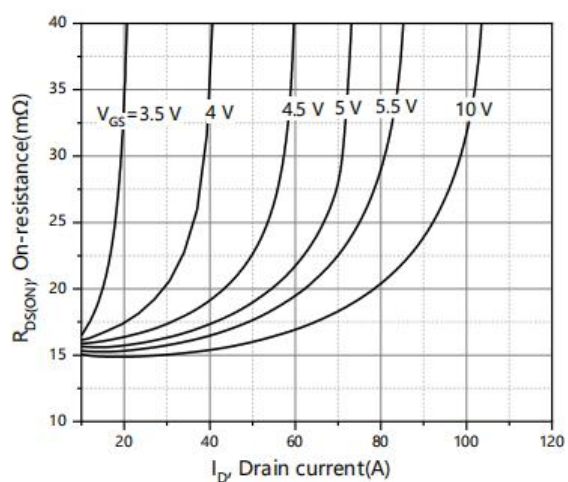


Figure 9. Drain-source on-state resistance

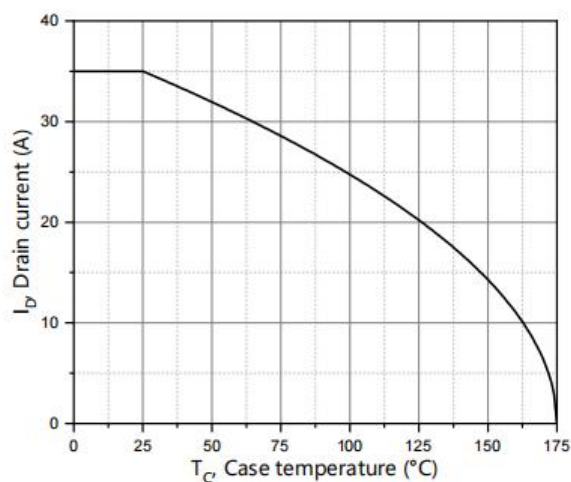


Figure 10. Drain current

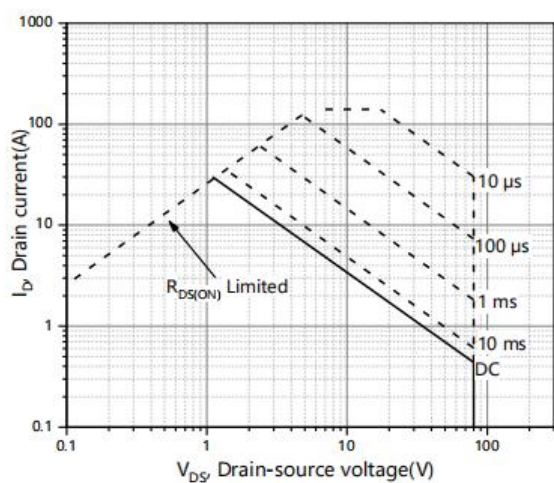


Figure 11. Safe operation area $T_C=25^{\circ}C$

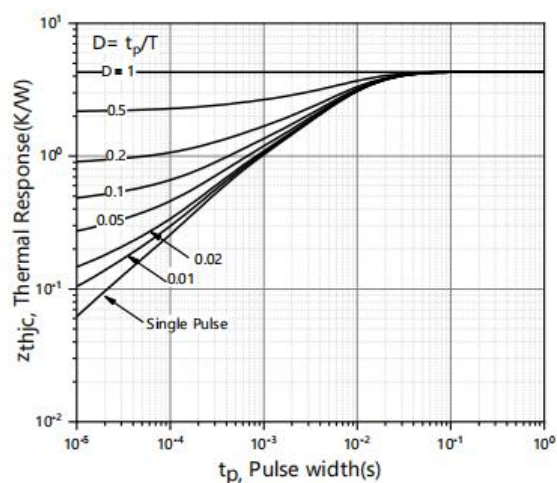


Figure 12. Max. transient thermal impedance

Test circuits and waveforms

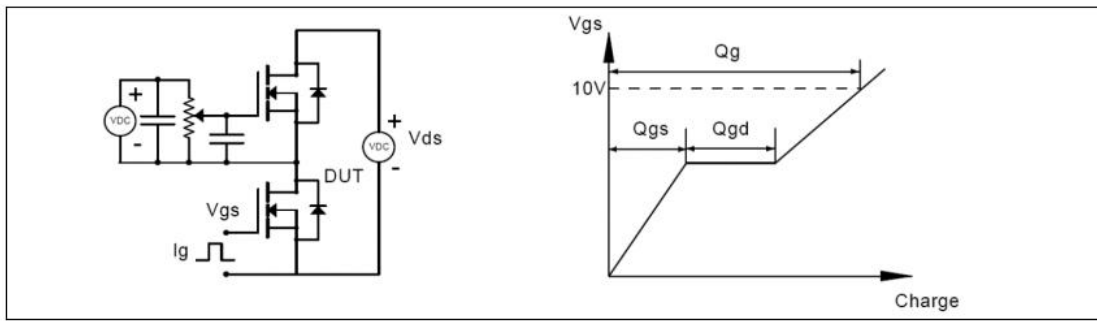


Figure 1. Gate charge test circuit & waveform

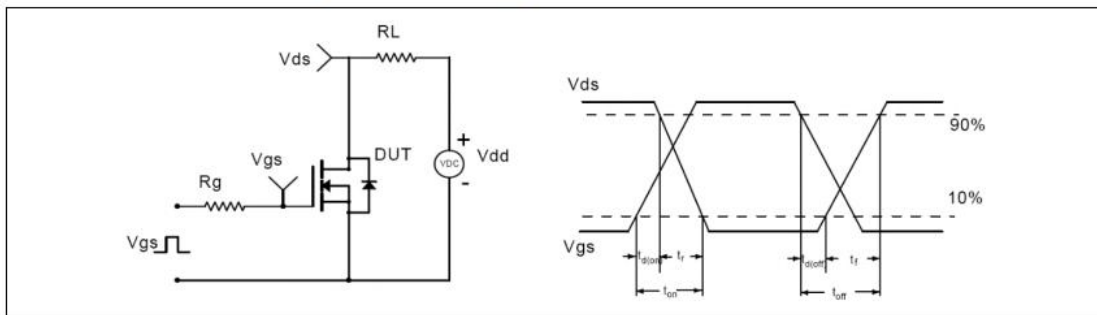


Figure 2. Switching time test circuit & waveforms

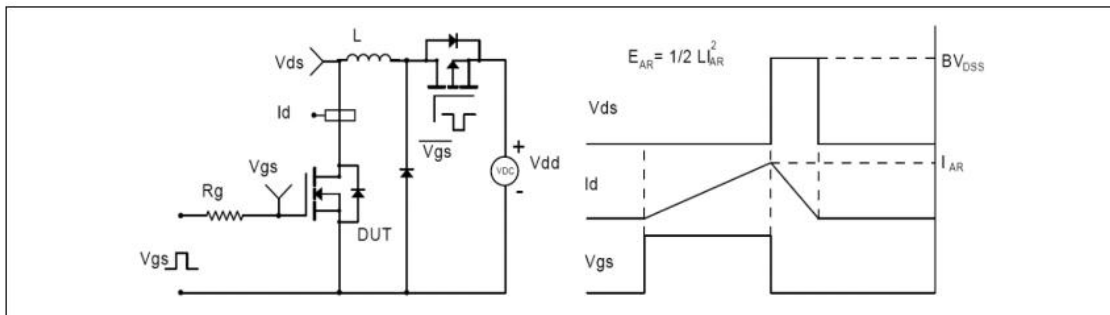


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

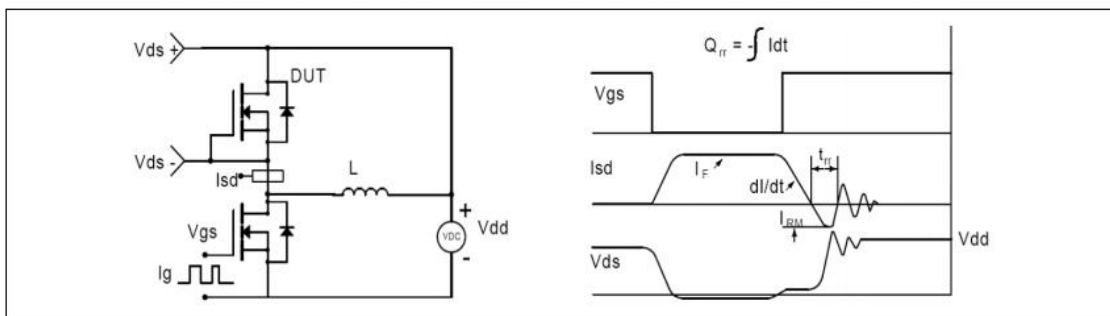
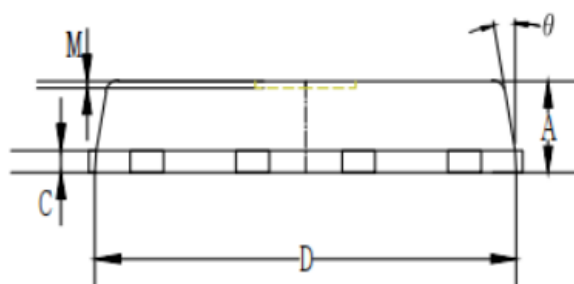
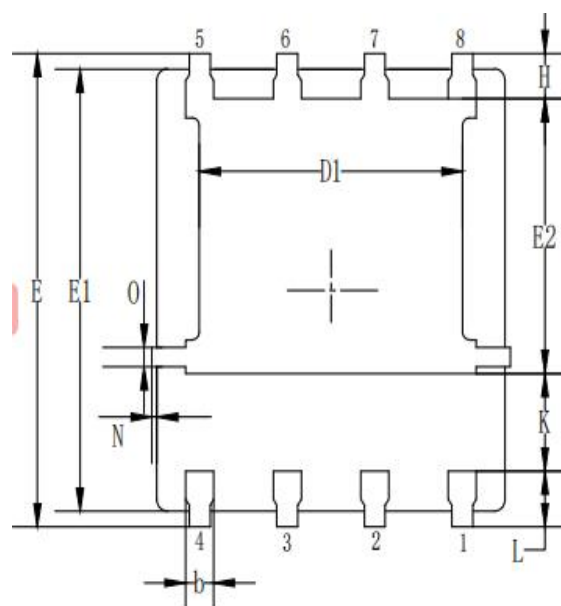
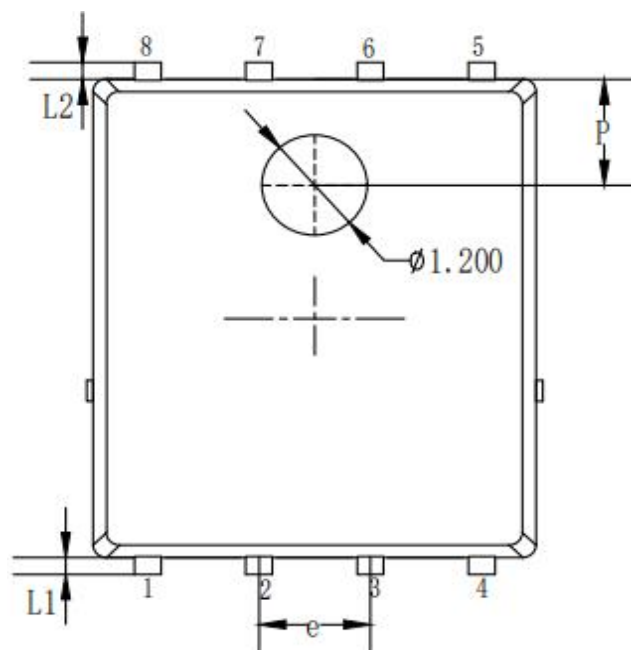


Figure 4. Diode reverse recovery test circuit & waveforms

Package Outline Dimensions



Symbols	Millimeters		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.10
D1	3.72	3.82	3.92
E	6.00	6.15	6.25
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.69	0.75
L1/L2	0.10 ~ 0.20		
θ	8°	10°	12°
M	0.08 REF.		
N	0	-	0.15
O	0.25 REF.		
P	1.28 REF.		

Legal Disclaimer

The information given in this document shall be for illustrative purposes only and shall in no event be regarded as a guarantee of conditions or characteristics. Existar Technologies reserves the right to change any information herein. With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Existar Technologies or its affiliates hereby make no representation or warranty of any kind, expressed or implied, as to any information provided hereunder, including without limitation as to the accuracy, completeness or non-infringement of intellectual property rights of any third party, and they assume no liability for the consequences of use of such information. In addition, any information given in this document is subject to customer's compliance with its obligations stated herein and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Existar Technologies in customer's applications. The information contained herein is exclusively intended for technically trained staff. No license is granted by implication under any patent right, copyright, mask work right, or other intellectual property right. It is customer's sole responsibility to evaluate the suitability of the product for the intended application and the completeness of the product information given herein with respect to such application. In no event shall Existar Technologies or its affiliates be liable to any party for any direct, indirect, special, punitive, incidental or consequential damages of any nature whatsoever, including but not limited to loss of profits and loss of goodwill, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory.