

Features

- Low capacitance for high speed interfaces
- Ultra low leakage: nA level
- Low operating voltage
- Low clamping voltage
- Protects two lines in common and differential mode
- JEDEC SO-8 package
- Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test
Air discharge: $\pm 30\text{kV}$
Contact discharge: $\pm 30\text{kV}$
 - IEC61000-4-5 (Lightning) 100A (8/20 μs)
- RoHS Compliant

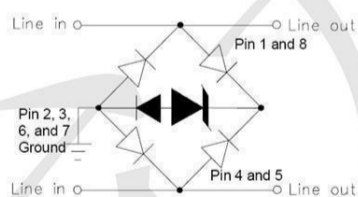
Mechanical Characteristics

- Package: SO-8
- Lead Finish: Matte Tin
- Case Material: "Green" Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below
- Shipping Qty :2500pcs/7Inch Tape & Reel

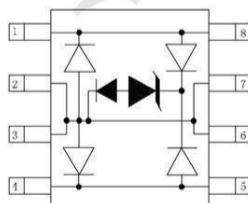
Applications

- T1/E1 Line Cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet
- Set Top Box
- ISDN Interfaces
- Low Voltage Interfaces

Dimensions and Pin Configuration

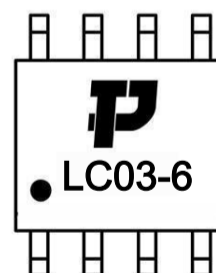


Circuit and Pin Schematic



SO-8 Outline

Marking:



Absolute Maximum Ratings (Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power(8/20μs)	Ppk	2000	W
Peak Pulse Current(8/20μs)	IPP	100	A
Lead Soldering Temperature	TL	260(10 sec.)	°C
Operating Temperature Range	TJ	-55 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Electrical Characteristics (TA=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	VRWM			5	V	
Reverse Breakdown Voltage	VBR	6 .8			V	IT = 1mA
Reverse Leakage Current	IR			25	μA	VRWM = 5V, T=25°C
Clamping Voltage	VC			10	V	IPP = 1A (8 x 20μs pulse) Line to Ground
Clamping Voltage	VC			15	V	IPP = 55A (8 x 20μs pulse) Line to Ground
Clamping Voltage	VC			20	V	IPP = 100A (8 x 20μs pulse) Line to Ground
Junction Capacitance	CJ			25	pF	VR = 0V, f = 1MHz Between I/O pins and Ground
			9	14	pF	VR = 0V, f = 1MHz Between I/O pins

Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise Specified)

Fig1. 8/20 μs Pulse Waveform

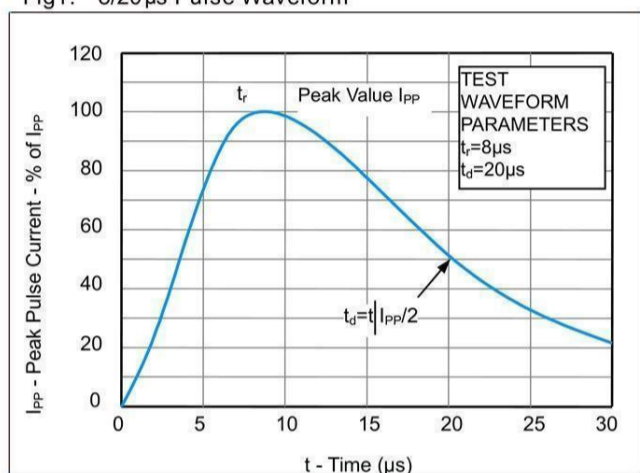


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

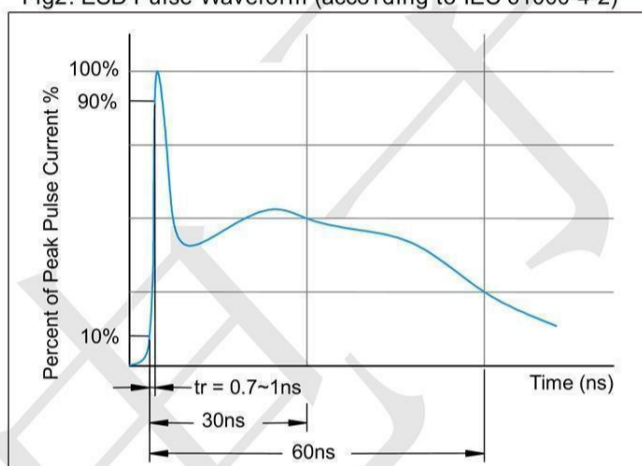
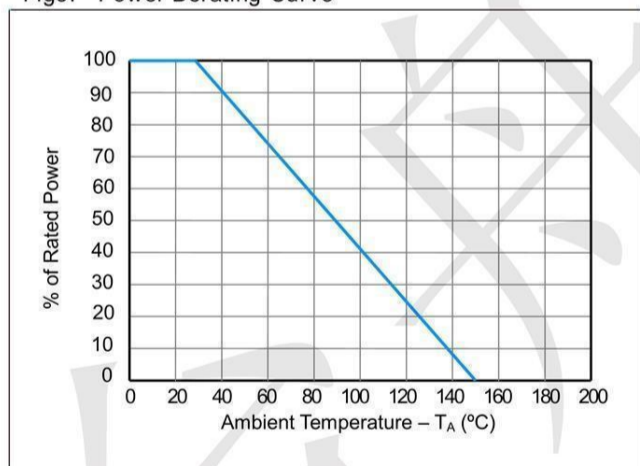
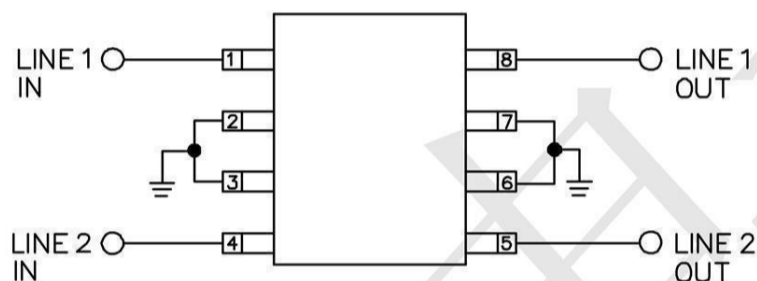


Fig3. Power Derating Curve

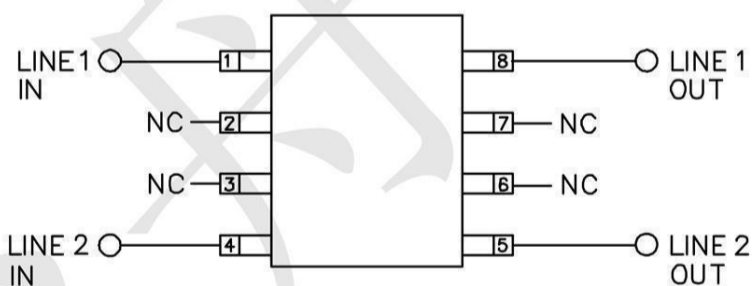


Typical Application

The LC03-6 is designed to protect two high speed data lines (one differential pair) from transient over - voltages which result from lightning and ESD. The device can be configured to protect in differential (Line to Line) and common (Line to Ground) mode. Data line inputs/outputs are connected at pins 1 to 8, and 4 to 5 as shown below. Pins 2, 3, 6, 7 are connected to ground. These pins should be connected directly to a ground plane on the board for the best results, the path length is kept as short as possible to minimize parasitic inductance. In applications where high common voltages are present, differential protection is achieved by leaving pins 2, 3, 6, and 7 not connected.

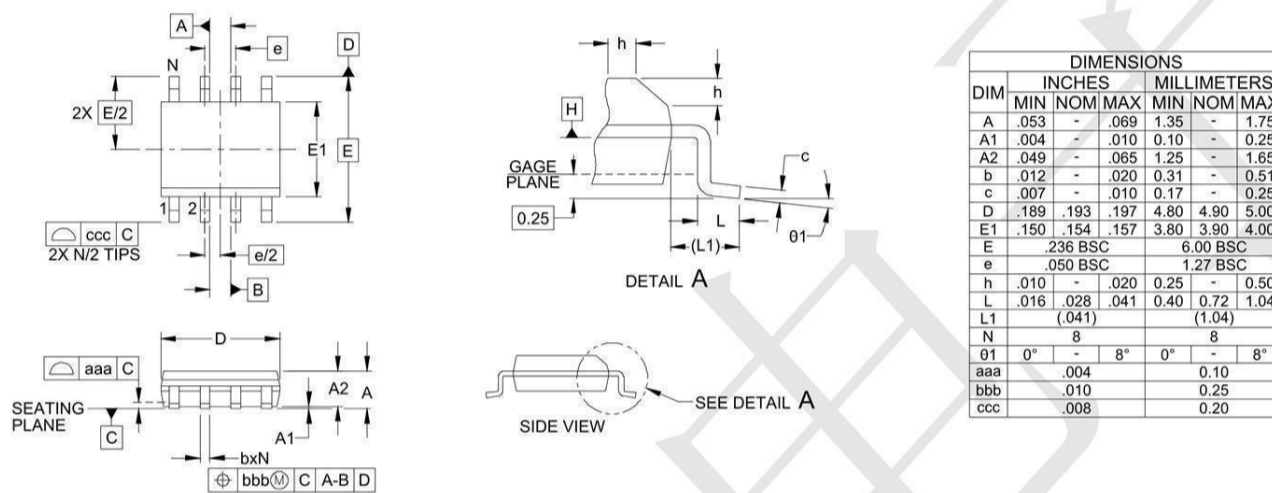


Connection for differential (Line to Line) and common mode protection (Line to Ground)



Connection for differential protection (Line to Line)

SOP-8 Package Outline Drawing



Suggested Land Pattern

