

N-Channel 40V MOSFET

E040N1P5HL1

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
40V	1.5 @ $V_{GS} = 10V$	125

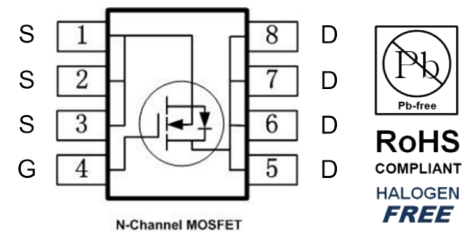
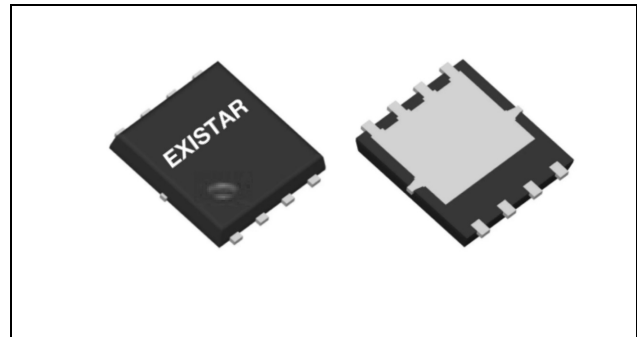
Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- PD charger
- Moto driver

PDFN5X6



Package And Ordering Information

Ordering code	Package	Marking
E040N1P5HL1	PDFN5x6	E040N1P5HL1

Ordering Information

Package	Units/ Reel	Reels/ Inner Box	Units/ Inner Box
PDFN5x6	5000	1	5000

Key Performance Parameters

Parameter	Value	Unit
V _{DS} , min @ T _j (max)	40	V
I _D , pulse	865	A
R _{DS(ON)} , max @ V _{GS} =10V	1.5	mΩ
Q _g	127	nC

Absolute Maximum Ratings at T_j=25°C Unless Otherwise Noted

Parameter		Symbol	Limit	Unit
Drain-source voltage		V _{DS}	40	V
Gate-source voltage		V _{GS}	±20	
Continuous drain current	T _C =25°C	I _D	125	A
	T _C =100°C		-	
Pulsed drain current		I _{D,pulse}	865	
Avalanche energy, single pulse		E _{AS}	870	mJ
Power dissipation	T _C =25°C	P _D	136	W
	T _A =25°C		2	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	R _{θJC}	1	°C/W
Thermal resistance, junction-to-ambient	Steady state	R _{θJA}	62	

Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Drain to source breakdown voltage	V _{(BR)DSS}	40			V	V _{GS} = 0, I _D = 250 μA
Gate-source threshold voltage	V _{GS(th)}	1.3		2.4	V	V _{DS} = V _{GS} , I _D = 250 μA
Gate-body leakage	I _{GSS}			±100	nA	V _{DS} = 0 V, V _{GS} = ±20 V
Zero gate voltage drain current	I _{DSS}			1	μA	V _{DS} = 40 V, V _{GS} = 0 V
Drain-source on-resistance	R _{DS(on)}		1.15	1.5	mΩ	V _{GS} = 10 V, I _D = 40 A
Drain-source on-resistance	R _{DS(on)}		1.6	2.1	mΩ	V _{GS} = 4.5 V, I _D = 30 A

Forward transconductance	gfs		-		S	VDS = 5 V, ID = 30 A
Gate resistance	Rg		3.8		Ω	f=1MHz
Gate Charge						
Total gate charge	Qg		124		nC	VDS = 20 V, ID = 40 A, VGS = 10 V
Gate-source charge	Qgs		25			
Gate-drain charge	Qgd		18			
Dynamic						
Turn-on delay time	td(on)		11		ns	VDS =20 V, ID =40 A, VGS = 10 V, RGEN = 3 Ω
Rise time	tr		93			
Turn-off delay time	td(off)		144			
Fall time	tf		90			
Input capacitance	Ciss		10530		pF	VDS =20 V, VGS = 0 V, f = 1MHz
Output capacitance	Coss		2045			
Reverse transfer capacitance	Crss		950			
Body Diode						
Diode forward voltage	VSD			1.2	V	VGS = 0 V, IF = 40 A
Reverse recovery time	trr		57		ns	VR= 20 V, IS =40 A, di/dt = 100 A/μs
Reverse recovery charge	Qrr		58		nC	

Electrical Characteristics Diagrams

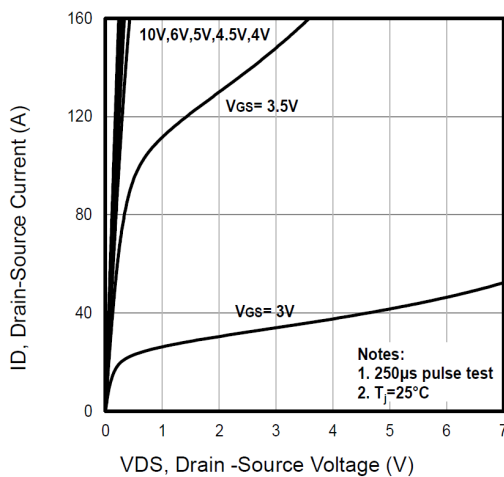


Fig1. Typical Output Characteristics

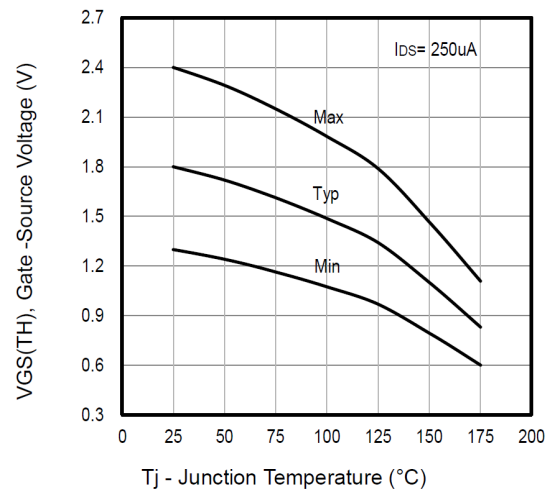
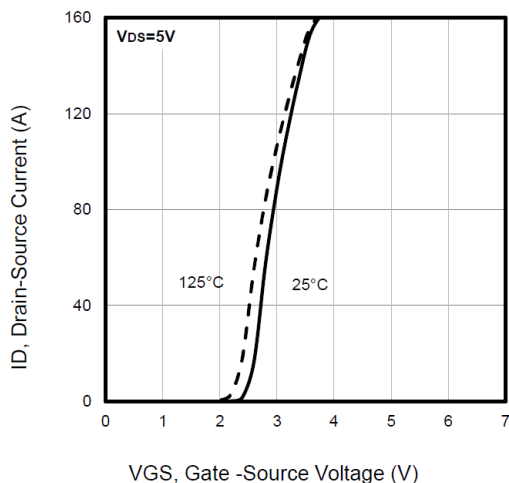
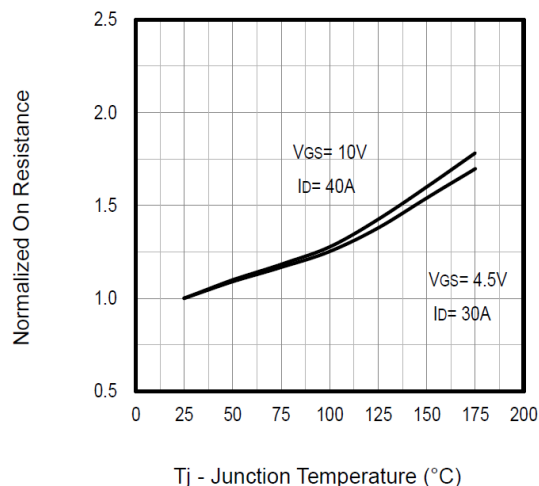
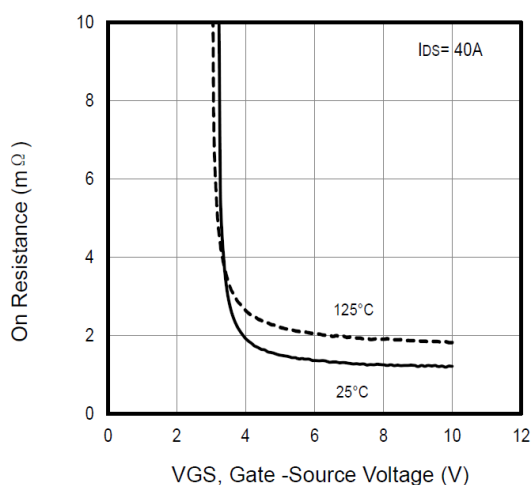
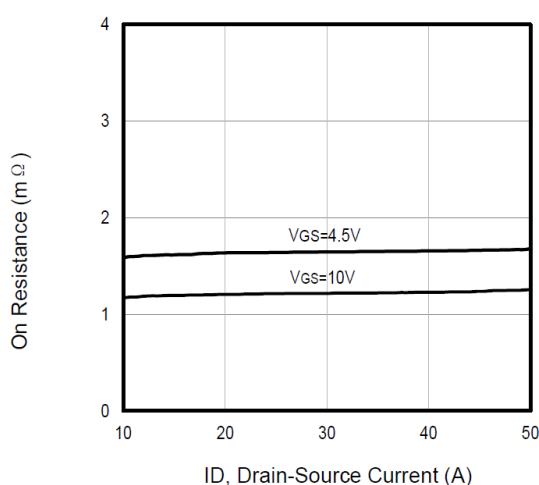
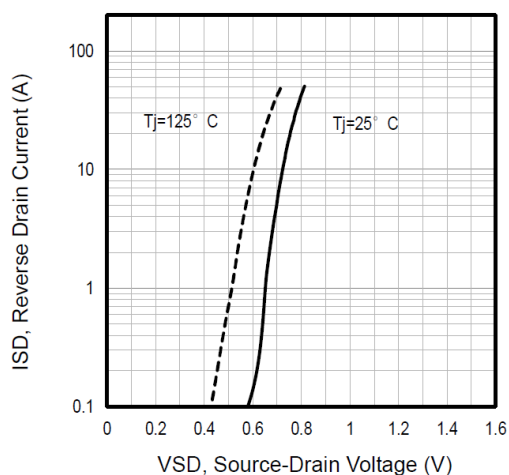
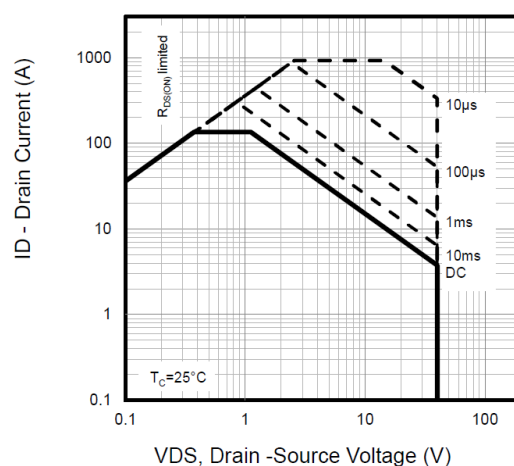


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j


Fig3. Typical Transfer Characteristics

Fig4. Typical Normalized On-Resistance Vs. TJ

Fig5. Typical On Resistance Vs Gate-Source Voltage

Fig6. Typical On Resistance Vs Drain Current

Fig7. Typical Source-Drain Diode Forward Voltage

Fig8. Maximum Safe Operating Area

Test circuits and waveforms

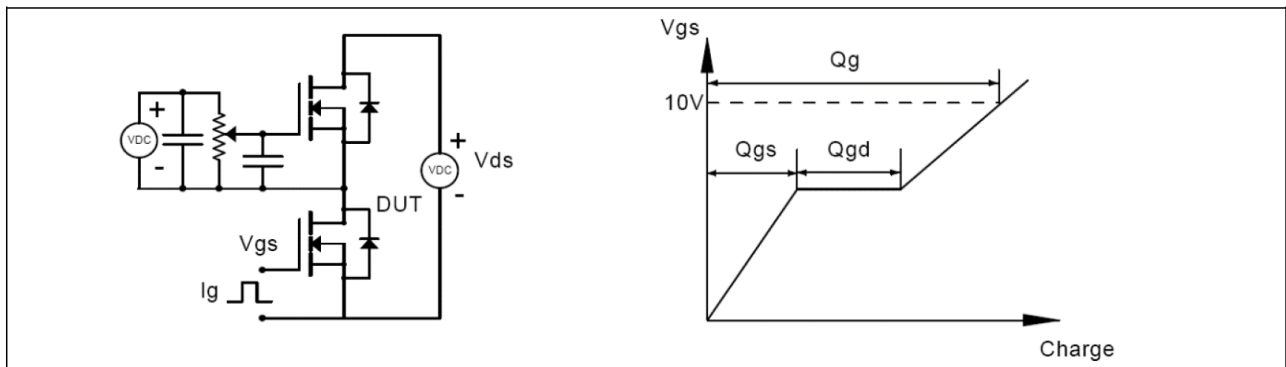


Figure 1. Gate charge test circuit & waveform

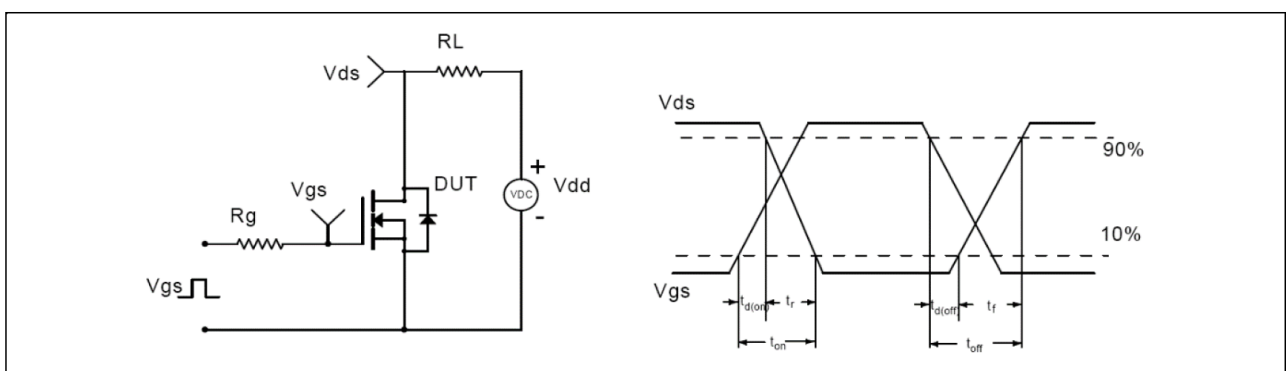


Figure 2. Switching time test circuit & waveforms

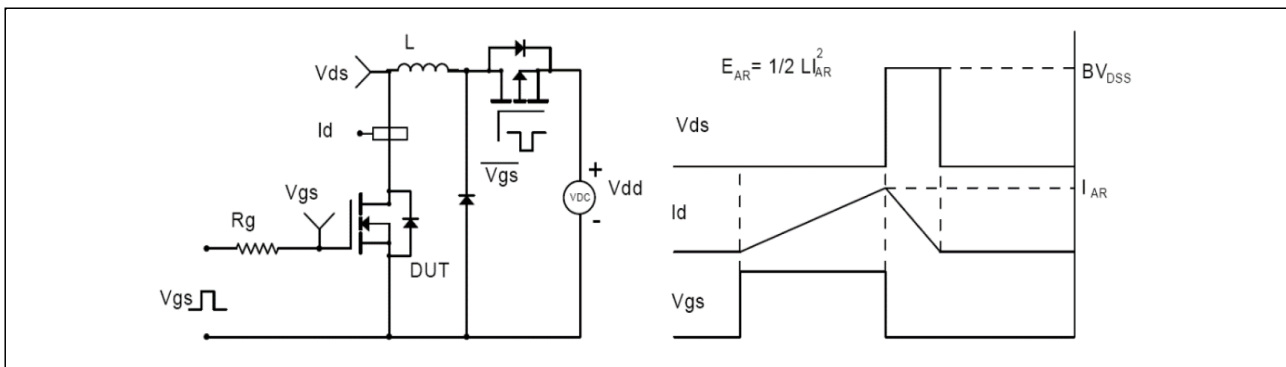


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

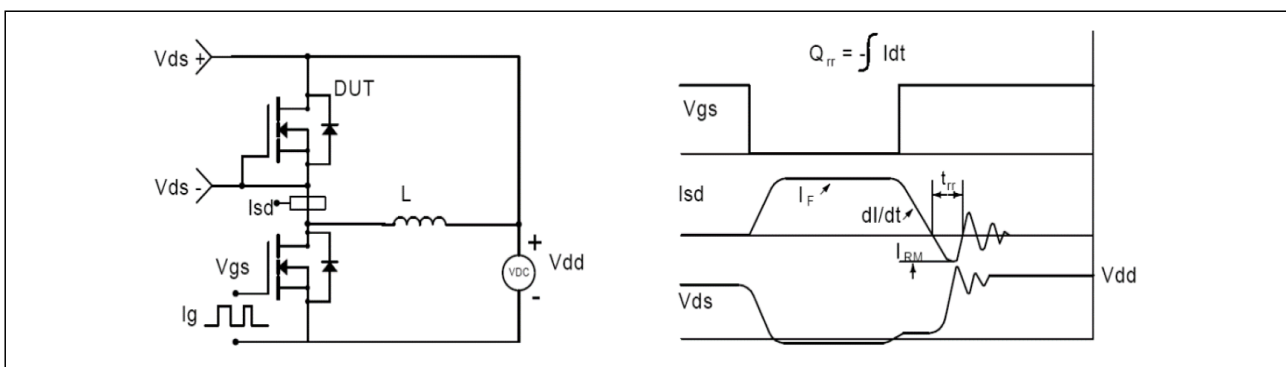
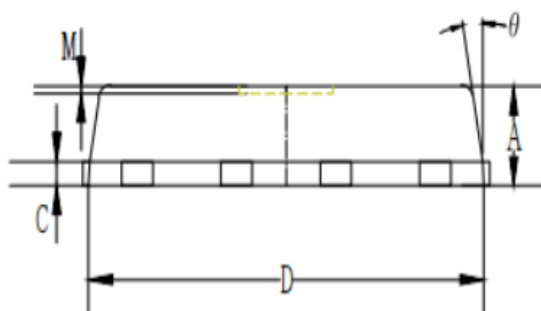
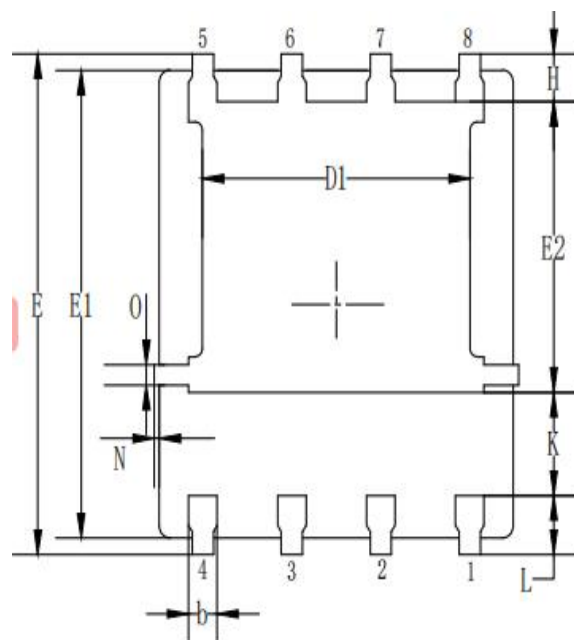
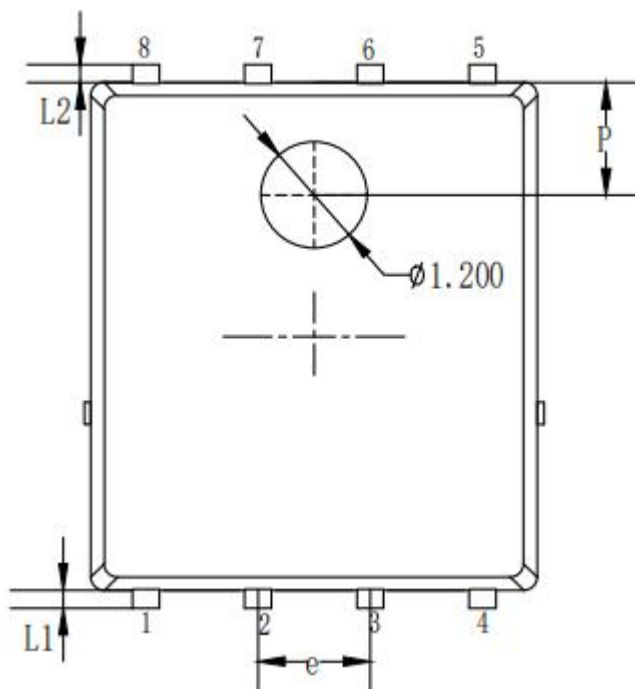


Figure 4. Diode reverse recovery test circuit & waveforms

Package Outline Dimensions



Symbols	Millimeters		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.10
D1	3.72	3.82	3.92
E	6.00	6.15	6.25
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.69	0.75
L1/L2	0.10 ~ 0.20		
θ	8°	10°	12°
M	0.08 REF.		
N	0	-	0.15
O	0.25 REF.		
P	1.28 REF.		

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