UMW HCPL-3120-xxxE

2.5 Amp Output Current IGBT Gate Drive Optocouple

1.Description

The HCPL-3120 is a gate driven optocoupler with an output current of 2.5 A, with an AlGaAs LED, which is coupled to a photosensitive integrated circuit through infrared light. This optocoupler can drive most low-power IGBTs and MOSFETs. In the motor control inverter and high-performance power system applications, it is very suitable for fast switching drive power IGBTs and MOSFETs.

2.Applications

- Uninterrupted Power Supply
- IGBT isolation / power MOSFET gate drive
- Induction heating
- Industrial inverters

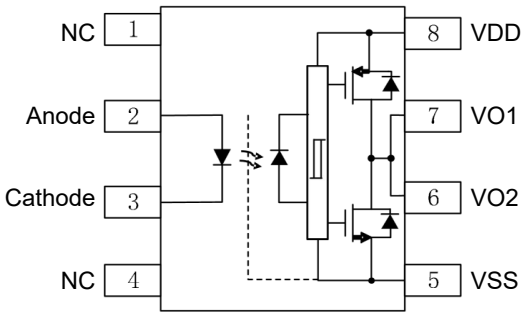
3.Features

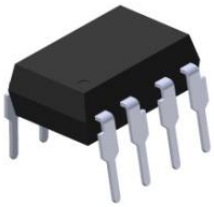
- 35kV/μs minimum Common Mode Rejection
- 2.5A maximum peak output current
- 2A minimum peak output current
- Wide operating V_{CC} Range: 15V~30V
- 400ns maximum propagation delay
- 100ns of pulse width distortion
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Operating temperature range: -40°C~ +110°C

4.Truth Table

LED	V_{CC}-V_{SS} " POSITIVE GOING" (TURN-ON)	V_{CC}-V_{SS} " NEGATIVE GOING" (TURN-OFF)	VO
OFF	0~30V	0~30V	LOW
ON	0~11.5V	0~10V	LOW
ON	11.5~13.5V	10~12V	TRANSITION
ON	13.5~30V	12~30V	HIGH

5.Pinning Information





DIP-8

SOP- 8

Note: 0.1uF bypass capacitor must be connected between pins 5 and 8.

6.Insulation And Safety Related Specifications

Parameter	Symbol	Note	Value	Unit
Creepage Distance	L	Measured from input terminals to output terminals, shortest distance path along body	≥7	mm
Clearance Distance	L	Measured from input terminals to output terminals, shortest distance through air	≥7	mm
Insulation Thickness	DTI	Insulation thickness between emitter and detector	≥0.4	mm
Peak Isolation Voltage	V_{IORM}	DIN/EN/IEC EN60747-5-5.	1500	V_{peak}
Transient Isolation Voltage	V_{IOTM}	DIN/EN/IEC EN60747-5-5.	7000	V_{peak}
Isolation Voltage	V_{ISO}	For 1 min	5000	V_{rms}

7.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Value	Units
Input	Forward Input Current (1)	I_F	25	mA
	Reverse Voltage	V_R	5	V
Output	Peak Output Current (2)	$I_{O(PEAK)}$	2.5	A
	Supply Voltage	V_{DD}-V_{SS}	0 to 35	V
	Output Voltage	V_O	0 to V_{DD}	V
Isolation Voltage		V_{ISO}	5000	V_{rms}
Total Power Dissipation (3)		P_T	295	mW
Output Power Dissipation (4)		P_O	250	mW
Lead Solder Temperature		260°C for 10 sec., 1.6 mm below seating plane		
Operating Temperature		T_{opr}	-40 to 110	°C
Storage Temperature		T_{stg}	-55 to 125	°C
Soldering Temperature		T_{sol}	260	°C

1. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

2. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See Applications section for additional details on limiting I_{OH} peak.

3. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C. The maximum LED junction tem-perature should not exceed 125°C.

4. Derate linearly above 70°C free-air temperature at a rate of 4.8 mW/°C.

8.Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{CC}-V_{SS}	15	30	V
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V
Operating Temperature	T_A	-40	110	°C

9.Electro-optical Characteristics (T_A=25°C)

All minimum and maximum specifications are at recommended operating conditions, unless otherwise noted
All typical values are at T_A=25°C, V_{DD}=30V, and V_{SS}=GND.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Forward Voltage	V_F	I_F=10mA		1.2	1.5	1.8	V
Reverse Current	I_R	V_R=5V				10	μA
High Level Output Current (1) (2)	I_{OH}	V_O=V_{DD}-3V		1	2		A
		V_O=V_{DD}-6V		2			A
Low Level Output Current (1) (2)	I_{OL}	V_O=V_{SS}+3V		1	2		A
		V_O=V_{SS}+6V		2			A
High Level Output Voltage (3) (4)	V_{OH}	I_F=10mA	I_O=-2.5A	V_{DD}-6.25V	V_{DD}-2.5V		V
			I_O=-100mA	V_{DD}-0.3V	V_{DD}-0.1V		V
Low Level Output Voltage	V_{OL}	I_F=0mA	I_O=2.5A		V_{SS}+2.5V	V_{SS}+6.25V	V
			I_O=100mA		V_{SS}+0.1V	V_{SS}+0.3V	V
High Level Power Supply Current	I_{ccH}	V_O=Open, I_F=7 to 16mA			1.8	3.8	mA
Low Level Power Supply Current	I_{ccL}	V_O=Open, I_F=0 to 0.8V			2.1	3.8	mA
Input The Tum On Current	I_{FLH}	I_O=0mA, V_O>5V			2.8	5	mA
Input The Turn Off Voltage	V_{FHL}	I_O=0mA, V_O<5V		0.8			V
UVLO Threshold	V_{UVLO+}	I_F=10mA, V_O>5V		11.5	12.7	13.5	V
	V_{UVLO-}	I_F=10mA, V_O<5V		10	11.2	12	V
UVLO Hysteresis	$UVLO_{HYS}$				1.5		V
Isolation Resistance	R_{ISO}	V_{I-O}=500V, 40~60%R.H.			10^{11}		Ω
Isolation Capacitance	C_{ISO}	V_{I-O}=0V, Freq=1MHZ			1		pF
Propagation Delay Time to Low Output Level (5)	T_{PHL}	I_F=7mA to 16mA Rg=10Ω Cg=10nF F=10KHZ Duty Cycle=50%			100	300	ns
Propagation Delay Time to High Output Level (5)	T_{PLH}				100	300	ns
Pulse Width Distortion (6)	PWD				3	100	ns
Propagation Delay Difference Between Any Two Parts (7)	P_{DD}			-250		250	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Rise Time (10% To 90%)	T_R	I_F=7mA to 16mA,Rg=10Ω,Cg=10NF		80		ns
Output Drop Time(90%~10%)	T_F	F=10KHZ, Duty Cycle=50%		80		ns
UVLO Turn On Delay	$T_{UVLO\ ON}$	I_F=10mA, V_O>5V		1.6		μs
UVLO Turn Off Delay	$T_{UVLO\ OFF}$	I_F=10mA, V_O<5V		0.4		μs
Output High Level Common Mode Transient Immunity (8) (9)	$\|CM_H\|$	T_A=25°C, V_{DD}=30V V_{CM}=2000V, I_F=7~16mA, V_F=0V	35	50		KV/μs
Output Low Level Common Mode Transient Immunity (8) (10)	$\|CM_L\|$	T_A=25°C, V_{DD}=30V V_{CM}=2000V, I_F=7~16mA, V_F=0V	35	50		KV/μs

1. Maximum pulse width = 10μs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See Applications section for additional details on limiting I_{OH} peak.
2. Maximum pulse width = 50μs, maximum duty cycle = 0.5%.
3. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
4. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
5. This load condition approximates the gate load of a 1200 V/75A IGBT.
6. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.
7. The difference between t_{PHL} and t_{PLH} between any two HCPL-3120 parts under the same test condition.
8. Pins 1 and 4 need to be connected to LED common.
9. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O>15.0V).
10. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O<1.0V).

10.1 Typical Characteristic

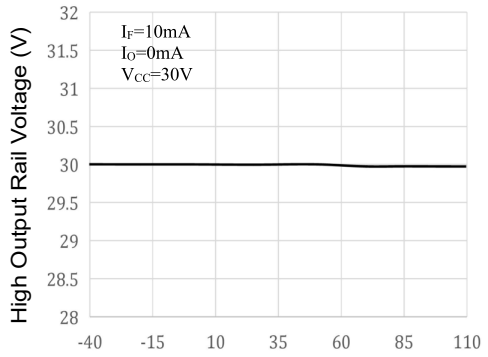


Figure 1: High Output Rail Voltage vs Ambient Temperature

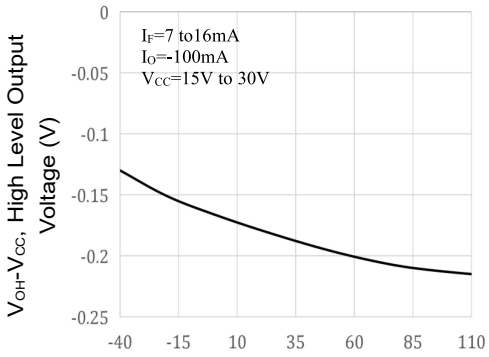


Figure 2: High Level Output Voltage vs Ambient Temperature

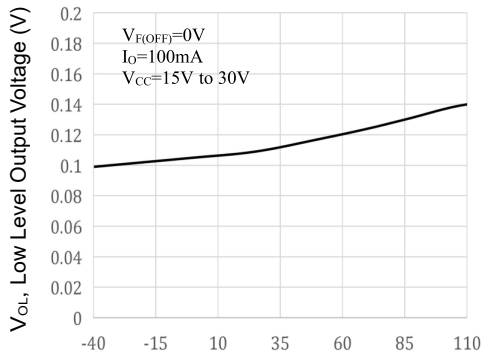


Figure 3: Low Level Output Voltage vs Ambient Temperature

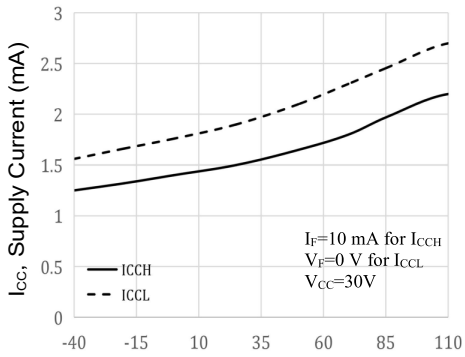


Figure 4: Supply Current vs Ambient Temperature

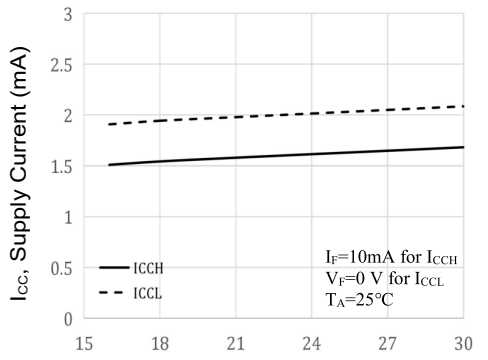


Figure 5: Supply Current vs supply Voltage

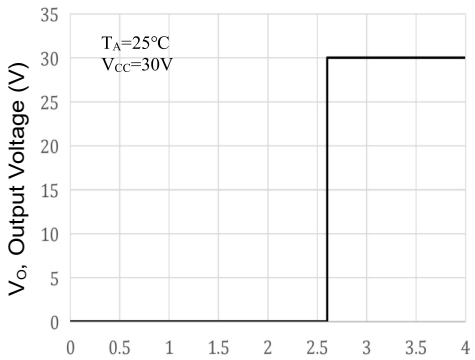


Figure 6: Output Voltage vs Threshold input Current Low to High

10.2 Typical Characteristic

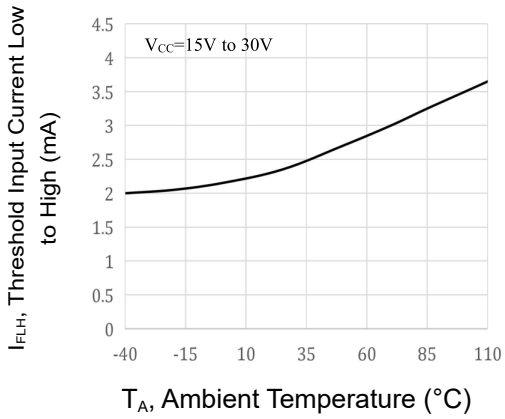


Figure 7: Threshold Input Current Low to High vs Ambient Temperature

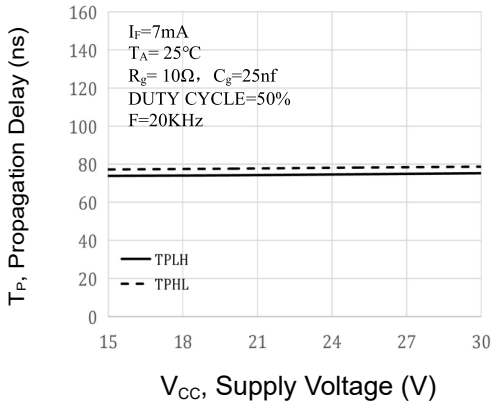


Figure 8: Propagation Delay vs Supply Voltage

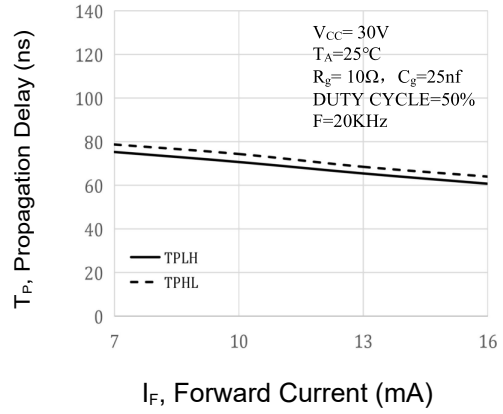


Figure 9: Propagation Delay vs Forward Current

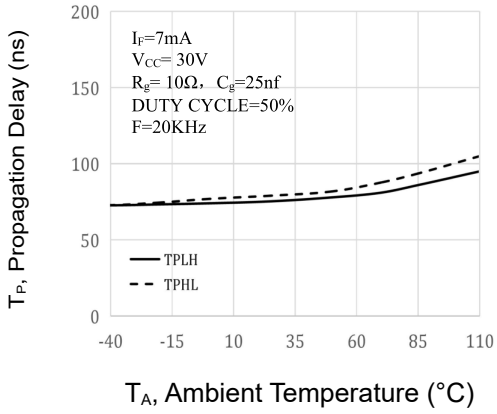


Figure 10: Propagation Delay vs Ambient Temperature

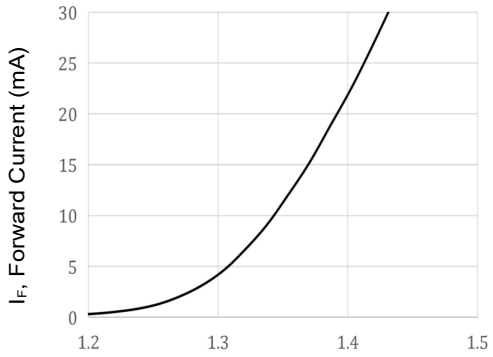


Figure 11: Forward Current vs Forward Voltage

11.Test Circuits Diagrams

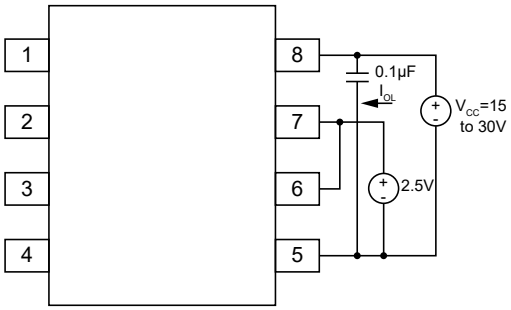


Figure.12 I_{OL} Pulsed Test Circuit

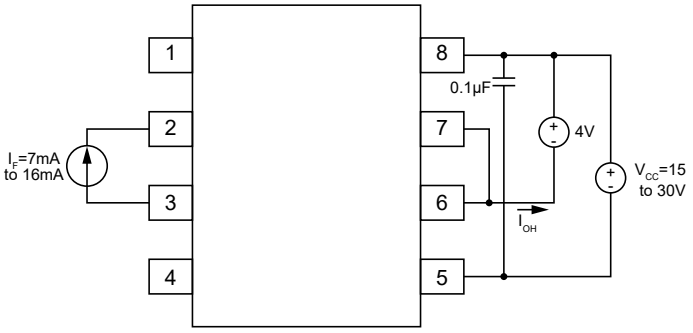


Figure.13 I_{OH} Pulsed Test Circuit

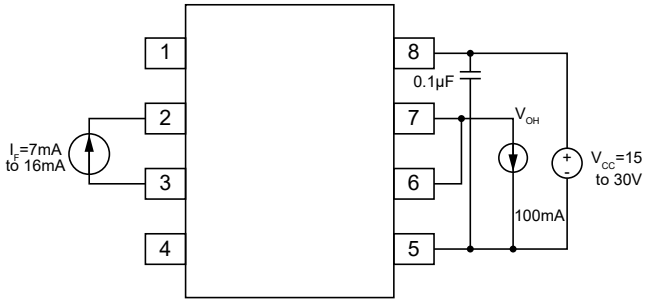


Figure.14 V_{OH} Pulsed Test Circuit

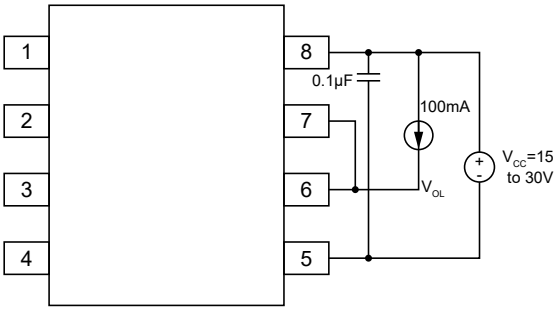


Figure.15 V_{OL} Pulsed Test Circuit

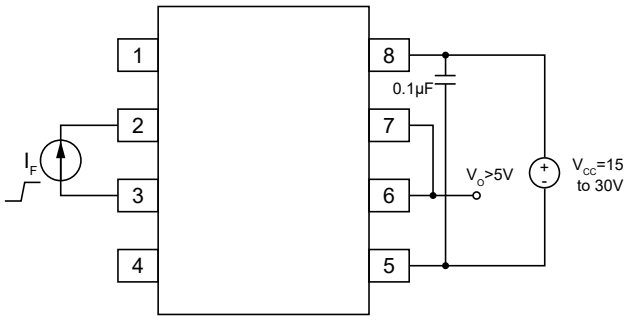


Figure.16 I_{FLH} Test Circuit

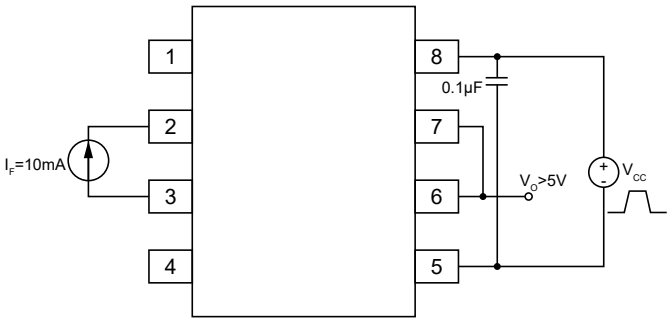


Figure.17 UVLO Test Circuit

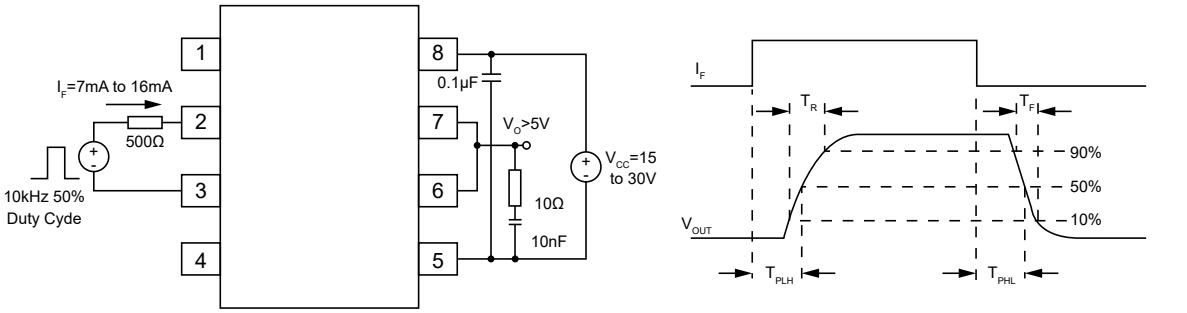


Figure.18 T_{PHL}, T_{PLH}, T_R, T_F Test Circuit

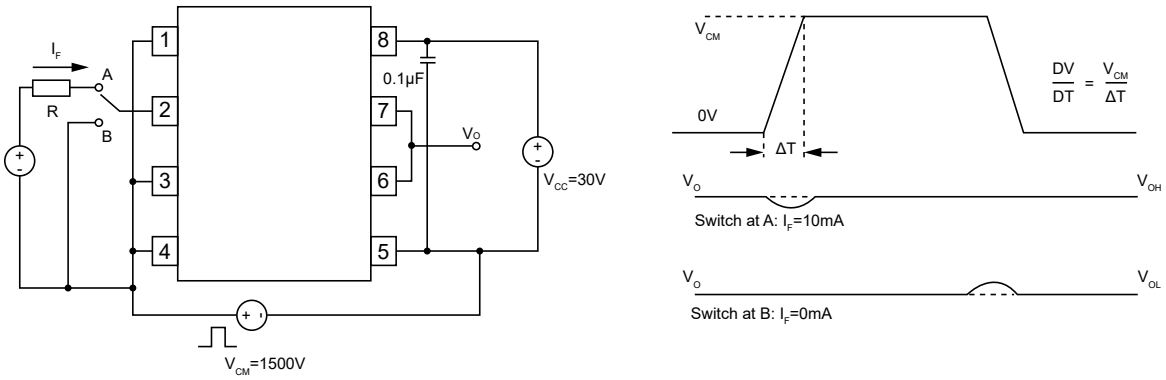
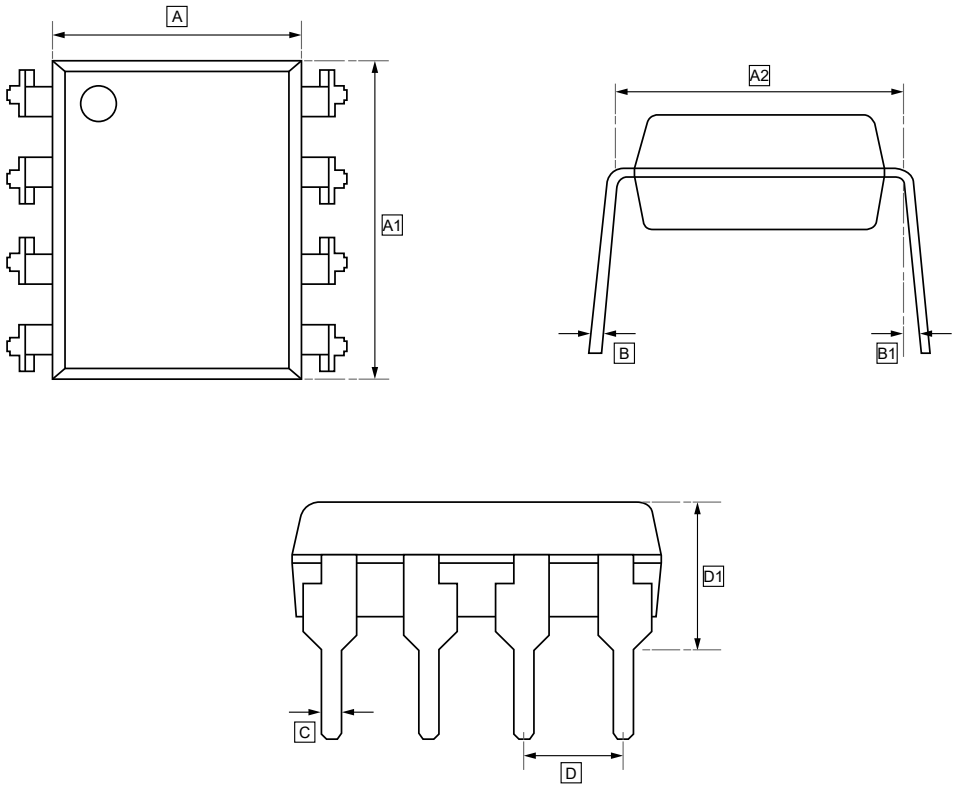


Figure.19 CMR Test Circuit

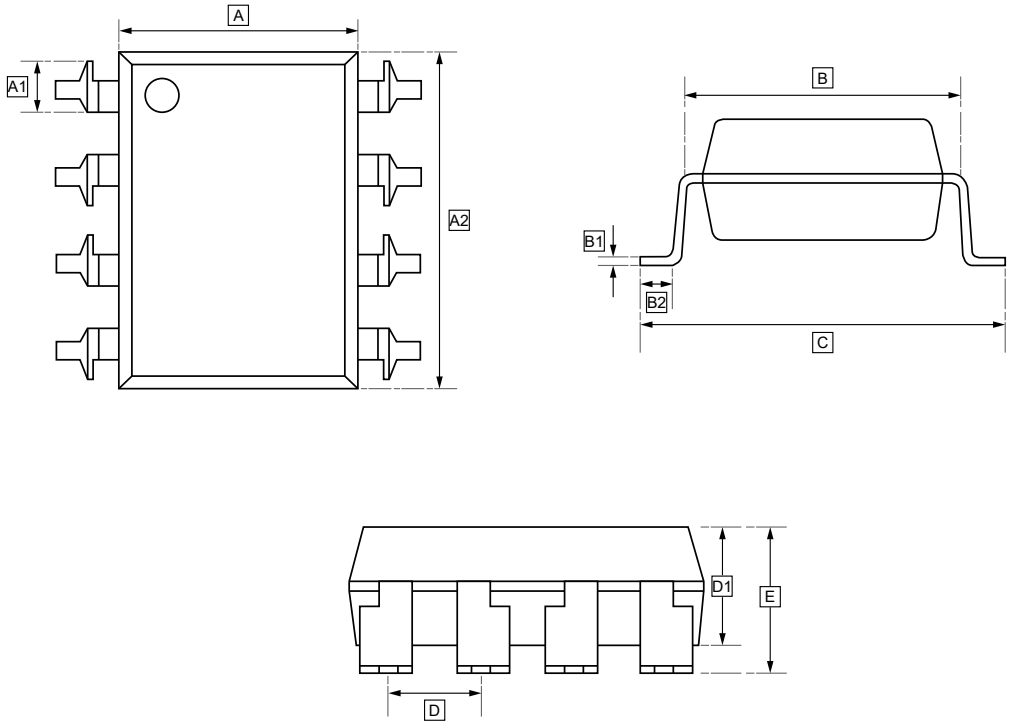
12.1 DIP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	C	D	D1
Min	6.30	9.46	7.62	0.25	5°	0.40	2.54	4.20
Max	6.90	10.06	TYP.		15°	0.60	TYP.	4.80

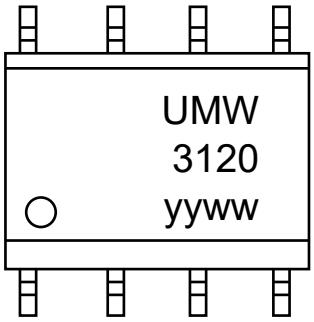
12.2 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	C	D	D1	E
Min	6.30	1.45	9.46	7.62	0.25	0.6	-	2.54	3.20	4.00
Max	6.90		10.06	TYP		-	10.3	TYP	3.80	4.60

13.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW HCPL-3120-000E	3120	DIP-8	2250	Tube and box
UMW HCPL-3120-500E	3120	SOP-8	1000	Tape and reel

14.Disclaimer

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