UMW HCPL-4504-xxxE

1.Description

HCPL4504 devices each consist of an infrared emitting diode, optically coupled to a high speed photo detector transistor. A separate connection for the photodiode bias and output-transistor collector increase the speed by several orders of magnitude over conventional phototransistor couplers by reducing the base-collector capacitance of the input transistor. The devices are packaged in an 8-pin DIP package and available in wide-lead spacing and SMD option

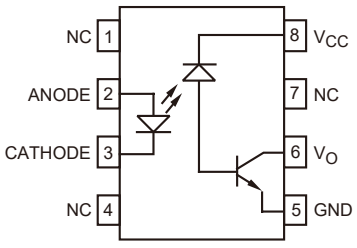
2.Applications

- Line receivers
- Telecommunication equipments
- Power transistor isolation in motor drives
- Replacement for low speed phototransistor photo couplers
- Feedback loop in switch-mode power supplies
- Home appliances
- High speed logic ground isolation

3.Features

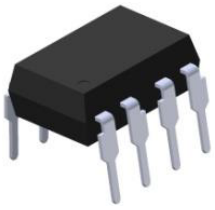
- High speed 1Mbit/s
- High isolation voltage between input and output (Viso=5000 Vrms)
- Guaranteed performance from 0°C to 70°C
- Wide operating temperature range of -55°C to 100°C
- Pb free and RoHS compliant

4.Pinning Information

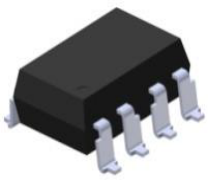


Truth Table

LED	V_O
ON	LOW
OFF	HIGH



DIP-8



SOP- 8

5.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Value	Units
Input	Forward current	I_F	25	mA
	Peak forward current (50% duty, 1ms P.W)	I_{FP}	50	mA
	Peak transient current (≤1μs P.W,300pps)	I_{Ftrans}	1	A
	Reverse voltage	V_R	5	V
	Power dissipation	P_{IN}	45	mW
Output	Power dissipation *1	P_O	100	mW
	Average Output current	$I_{O(AVG)}$	8	mA
	Peak Output current	$I_{IO(PK)}$	16	mA
	Output voltage	V_O	-0.5 to 20	V
	Supply voltage	V_{CC}	-0.5 to 30	V
Total Power Dissipation		P_{TOT}	145	mW
Isolation Voltage *2		V_{ISO}	5000	V_{rms}
Operating Temperature		T_{OPR}	-55 to 100	°C
Storage Temperature		T_{STG}	-55 to 125	°C
Soldering Temperature *3		T_{SOL}	260	°C

*1. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C (SO-8).

*2. AC for 1 minute, R.H.=40 ~ 60% R.H. In this test, pins 1,2,3 & 4 are shorted together,and pins 5,6,7 & 8 are shorted together.

*3. For 10 seconds.

6.Electrical Characteristics (T_A=0 to 70°C unless specified otherwise)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Forward Voltage	V_F	I_F=16mA		1.45	1.7	V
Reverse Voltage	B_{VR}	I_R=10μA	5	20		V
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	I_F=16mA		-1.6		mV/°C
Output						
Logic High Supply Current (1)	I_{CCH}	V_{CC}=15V, I_F=0mA, V_O=Open			1	μA
		T_A=0~70°C			2	μA
Logic Low Supply Current (1)	I_{CCL}	V_{CC}=15V, I_F=16mA, V_O=Open		50	200	μA
Transfer						
Logic High Output Current	I_{OH}	I_F=0mA, V_O=V_{CC}=5.5V		0.001	0.5	μA
		I_F=0mA, V_O=V_{CC}=15V		0.005	1	μA
		T_A=0~70°C, V_O=V_{CC}=15V			50	μA
Logic Low Output Voltage	VOL	I_F=16mA, V_{CC}=4.5V,I_O=2.4mA		0.1	0.4	V
Current Transfer Ratio (2)	CTR	I_F=16mA, V_{CC}=4.5V, I_O=0.4V	26	33	60	%
Isolation Voltage(3) (4) (5)	V_{ISO}	RH<50%, T_A=25°C, I_{I-O}≤50μA	5000			V_{RMS}

7.Switching Characteristics

(T_A=0 to 70°C unless specified otherwise, I_F=16mA, V_{CC}=5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Propagation Delay Time to Logic Low (6)	T_{PLH}	I_F=16mA, R_L=4.1kΩ			1300	1500	ns
		I_F=16mA, R_L=1.9kΩ			600	800	ns
Propagation Delay Time to Logic (7)	T_{PHL}	I_F=16mA, R_L=4.1kΩ			200	1500	ns
		I_F=16mA, R_L=1.9kΩ			200	800	ns
Common Mode Transient Immunity at Logic High (6) (7) (8) (9)	$\|CM_H\|$	R_L=4.1KΩ	T_A=25°C, I_F=0mA, C_L=15pF		10000		V/μs
		R_L=1.9KΩ	|VCM|=10V(Peak)				
Common Mode Transient Immunity at Logic Low (6) (7) (8) (9)	$\|CM_L\|$	R_L=4.1KΩ	T_A=25°C, I_F=16mA		10000		V/μs
		R_L=1.9KΩ	C_L=15pF				

(1) Use of a 0.1 μF bypass capacitor connected between Pins 5 and 8 is recommended.

(2) CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.

(3) Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.

(4) In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (leakage detection current limit, I_{i-o} ≤ 5 μA).

(5) This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.

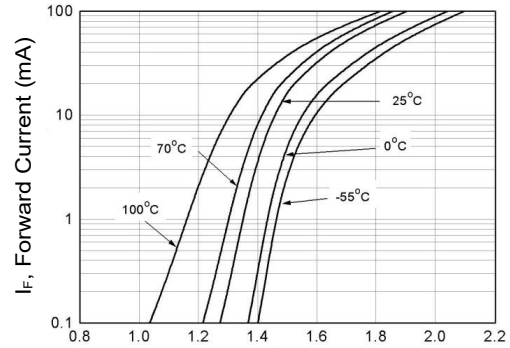
(6) The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.

(7) The R_L = 20 kΩ, C_L = 100 pF load represents an IPM (Intelligent Power Module) load.

(8) Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).

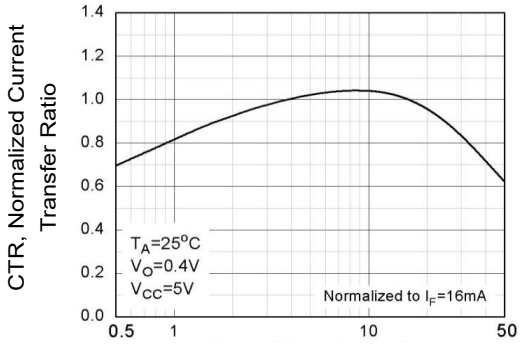
(9) Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 3.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e.,V_O<1.0V).

8.Typical Characteristic



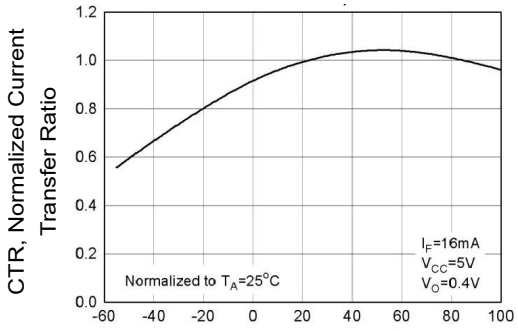
V_F, Forward Voltage (V)

Figure 1: Forward Current vs. Forward Voltage



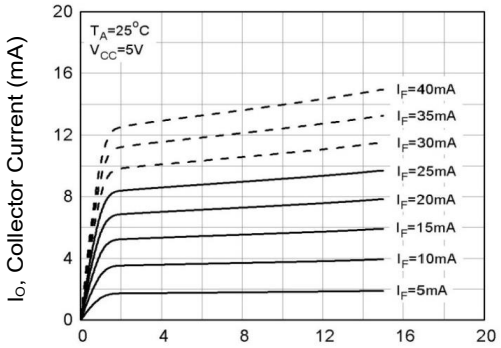
I_F, Forward Current (mA)

Figure 2: Normalized Current Transfer Ratio vs. Forward Current



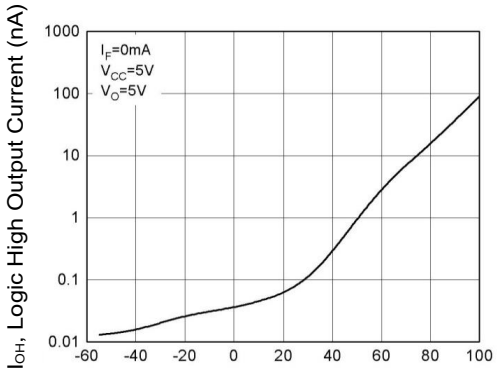
T_A, Ambient Temperature (°C)

Figure 3: Normalized Current Transfer Ratio vs. Ambient Temperature



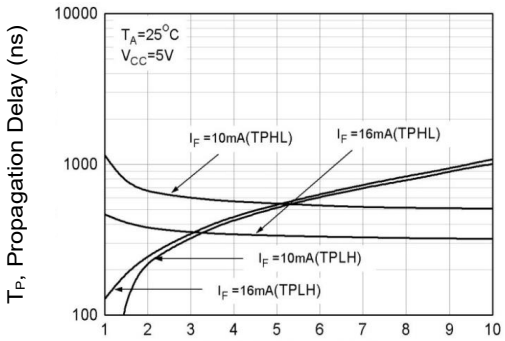
V_O, Collector-Emitter Voltage (V)

Figure 4: Output Current vs Output Voltage



T_A, Temperature (°C)

Figure 5: Logic High Output Current vs. Temperature



R_L, Load Resistance (kΩ)

Figure 6: Propagation Delay vs. Load Resistance

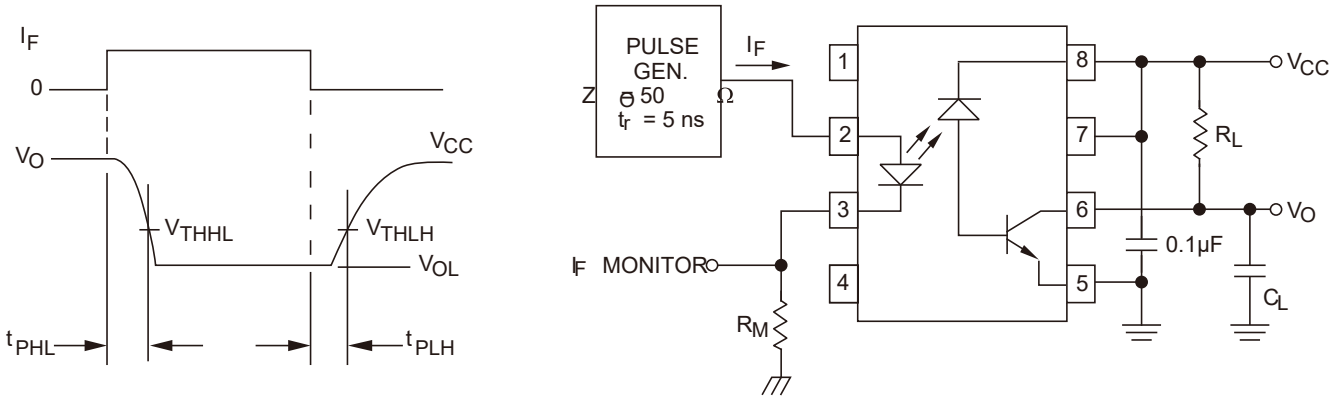


Figure 6: Switching Test Circuit

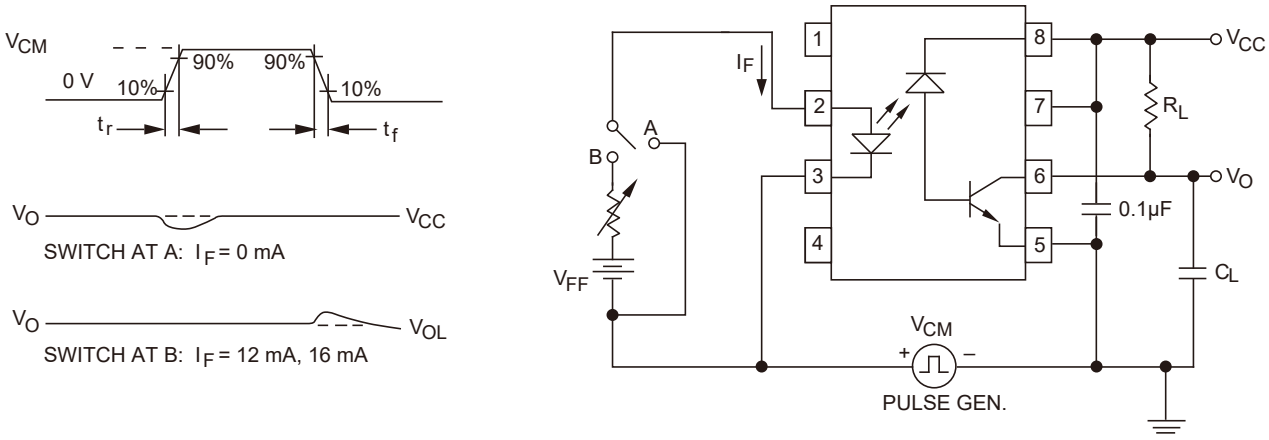
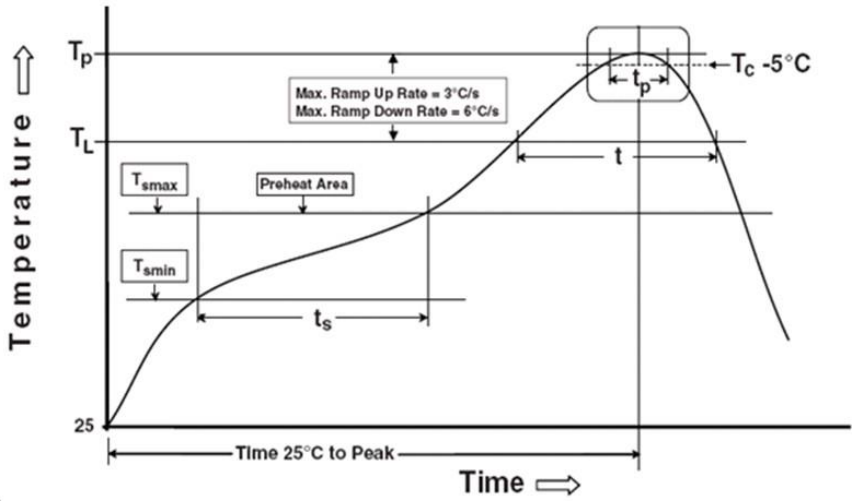


Figure 7: Test Circuit for Transient Immunity and Typical Waveforms

11.Precautions for Use

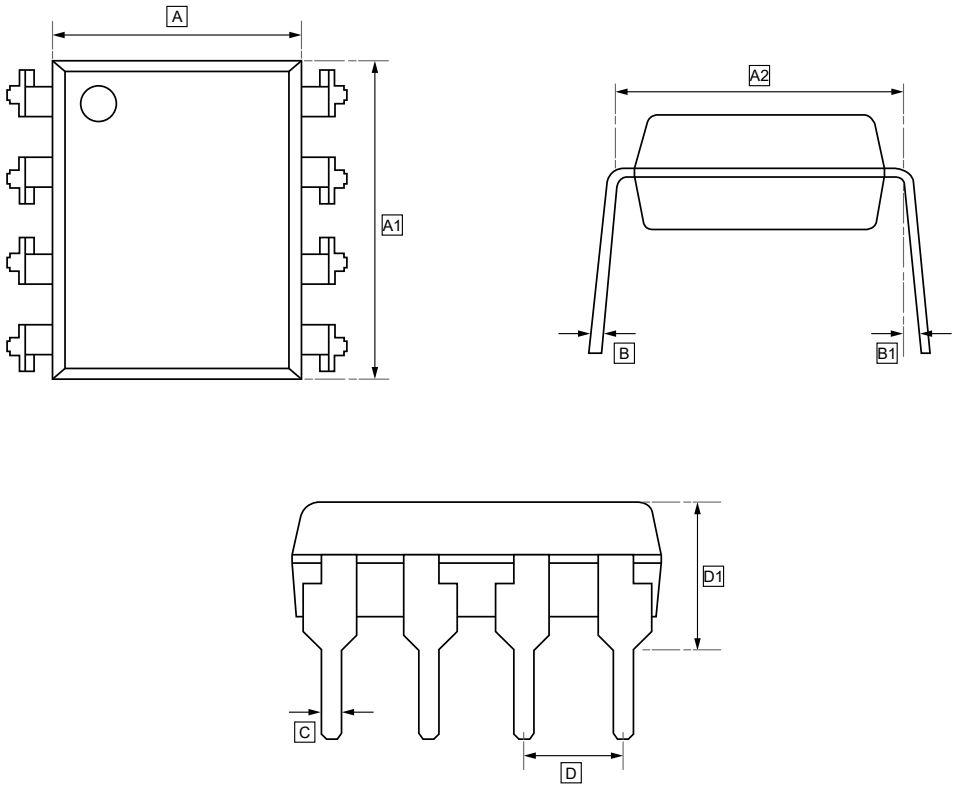


1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile

Preheat	
Temperature min (T_{smin})	150°C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3°C/second max
Other	
Liquidus Temperature (T_L)	216°C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_p)	260°C
Time within 5°C of Actual Peak Temperature: T_p - 5°C	30s
Ramp- Down Rate from Peak Temperature	6°C /second max
Time 25°C to peak temperature	8 minutes max
Reflow times	3 times

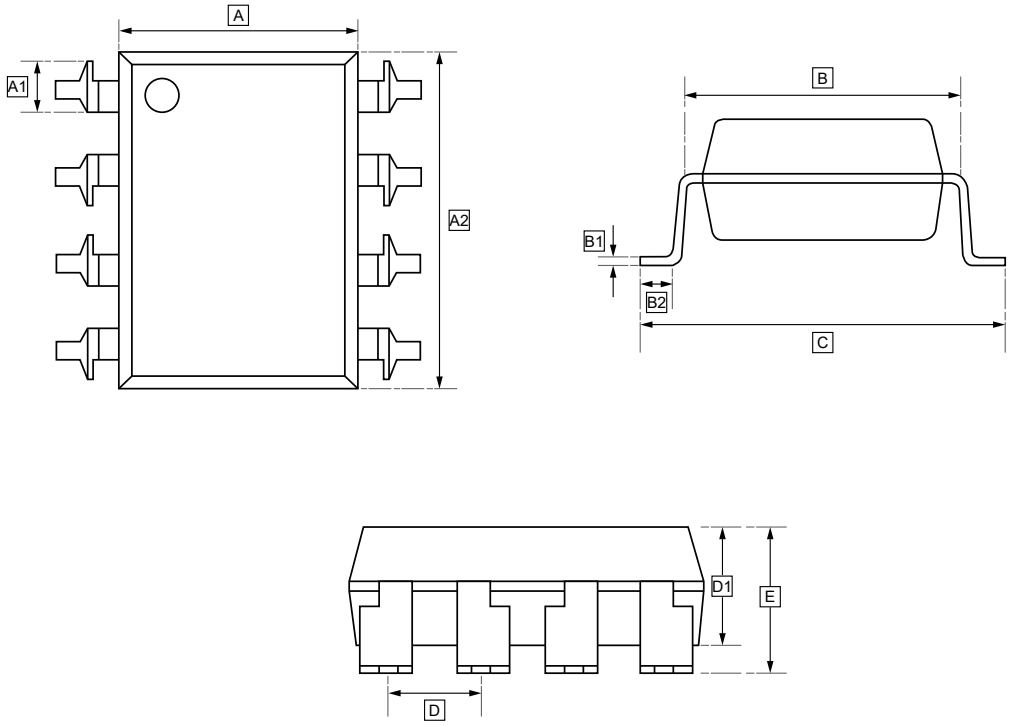
12.1 DIP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	C	D	D1
Min	6.30	9.46	7.62	0.25	5°	0.40	2.54	4.20
Max	6.90	10.06	TYP.		15°	0.60	TYP.	4.80

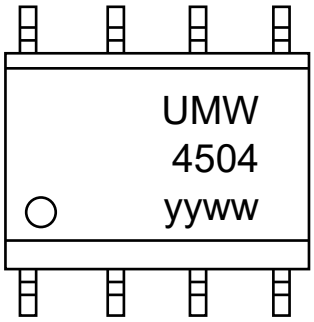
12.2 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	C	D	D1	E
Min	6.30	1.45	9.46	7.62	0.25	0.6	-	2.54	3.20	4.00
Max	6.90		10.06	TYP		-	10.3	TYP	3.80	4.60

13.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW HCPL-4504-000E	4504	DIP-8	2250	Tube and box
UMW HCPL-4504-500E	4504	SOP-8	1000	Tape and reel

14.Disclaimer

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