Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

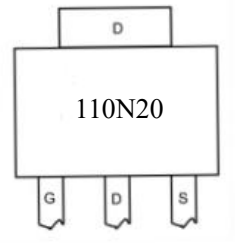
Bvdss	Rdson	ID
200V	8.9mΩ	120A

Application

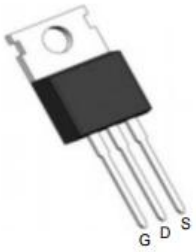
RoHS

- DC-DC Converters
- Power management function
- Synchronous-rectification applications

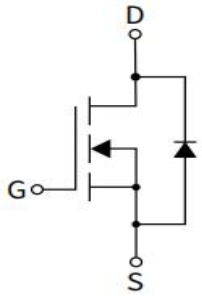
Package



Marking and pin assignment



TO220 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
110N20	S110N20T	TO220	50

Absolute Maximum Ratings (T_C=25℃unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{Gs}	±20	V
Continuous Drain Current[1]	T_C=25℃	I_D	120	A
	T_C=100℃	I_D	80	A
Pulsed Drain Current[2]		I_{DM}	458	A
Single Pulsed Avalanche Energy[3]		E_{As}	320	mJ
Power Dissipation[4]		P_D	355	W
Junction Temperature Range		T_J	-55 ~ 150	℃
Storage Temperature Range		T_{STG}	-55 ~ 150	℃

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient	$R_{\theta JA}$	45	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	0.42	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS110N20T	TO220	1	2	3	Tube

Electrical Characteristics (T_J=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	VB_{DSS}	I_D=250μA, V_{GS}=0V	200	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=200V,V_{GS}=0V,T_J=25℃	-	-	1	μA
		V_{DS}=80V,V_{GS}=0V,T_J=100℃	-	-	100	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS},I_D=250uA	2	3	4	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS}=10V,I_D=60A	-	8.9	10.8	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=60A	-	104	-	S
Diode Forward Voltage[2]	V_{SD}	I_S=60A,V_{GS}=0V	-	-	1.3	V
Diode Continuous Current[1,4]	I_S	V_G=V_D=0V,Force Current	-	--	120	A
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=100V, f=1MHz	-	5270	-	pF
Output Capacitance	C_{oss}		-	460	-	pF
Reverse Transfer Capacitance	C_{rss}		-	24	-	pF
Gate Resistance	R_g	V_{GS}=0V,V_{DS}=0V,f=1MHz	-	3.5	-	Ω
Turn-ON Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=100V, R_G=2.7,I_D=60A	-	35	-	ns
Rise Time	t_r		-	111	-	
Turn-OFF Delay Time	$t_{d(off)}$		-	84	-	
Fall Time	t_f		-	112	-	
Total Gate Charge@V_{GS}=10V	Q_g	V_{GS}=10V, V_{DS}=100V,I_D=60A	-	74	-	nC
Gate Source Charge	Q_{gs}		-	30	-	
Gate Drain Charge	Q_{gd}		-	16	-	
Body Diode Reverse Recovery Time	Trr	IF=17A, dIF/dt=100A/s	-	151	-	ns
Body Diode Reverse Recovery Charge	Qrr		-	779	-	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃

2. The EAS data shows Max. rating . The test condition is V_{DD}=100V,V_{GS}=10V,L=0.5mH，I_{AS}=36A.

3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.

4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.

Typical Performance Characteristics

Fig 1: Output Characteristics

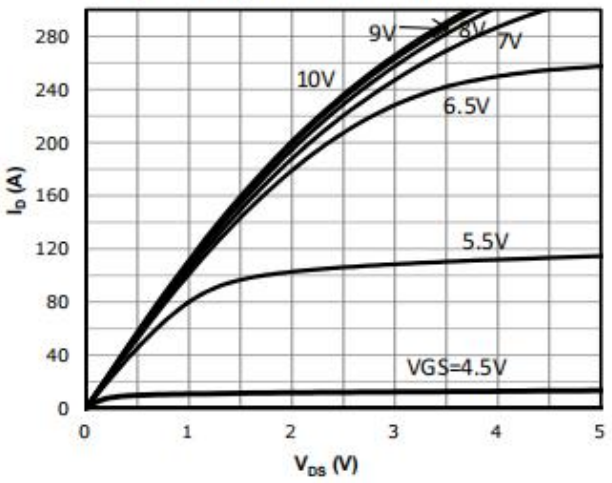


Fig 2: Transfer Characteristics

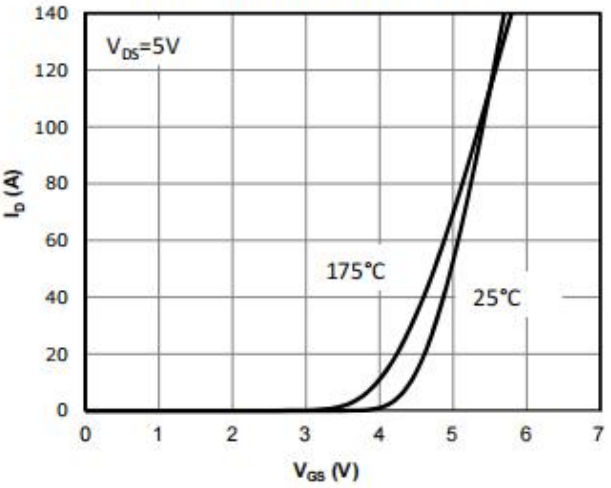


Fig 3: Rds(on) vs Drain Current and Gate Voltage

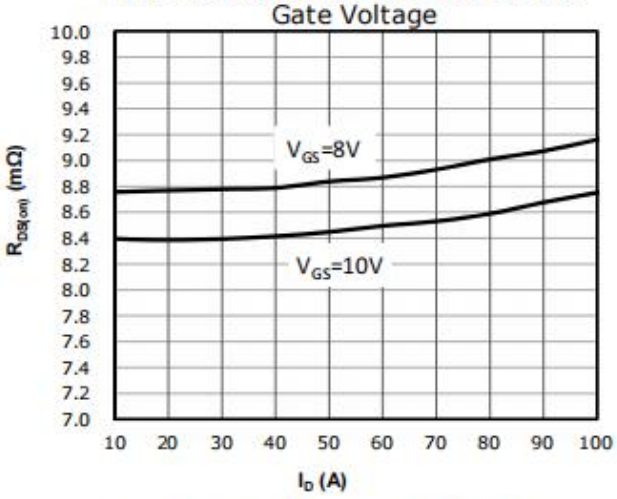


Fig 4: Rds(on) vs Gate Voltage

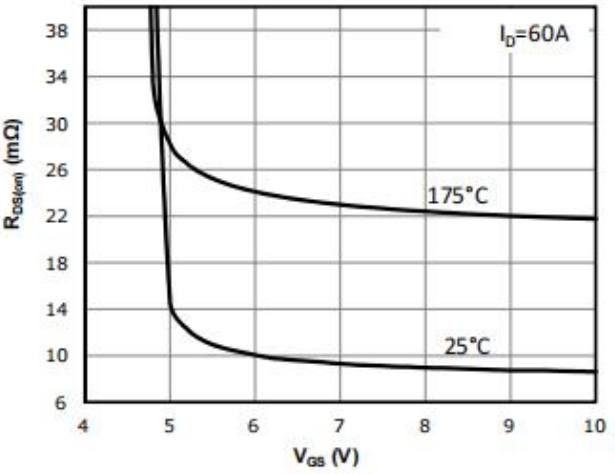


Fig 5: Rds(on) vs. Temperature

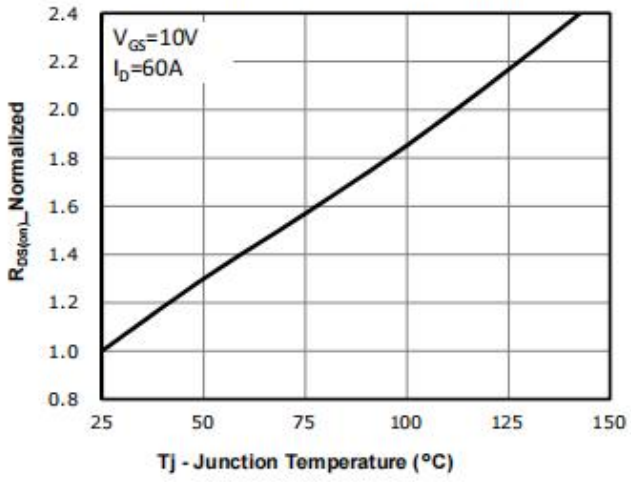


Fig 6: Capacitance Characteristics

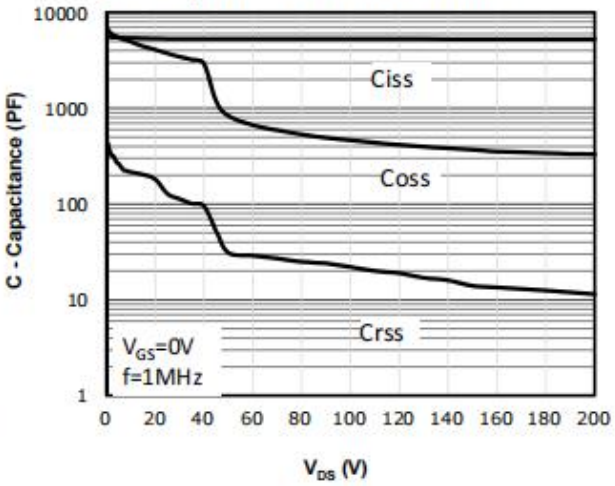


Fig 7: Vgs(th) vs. Temperature

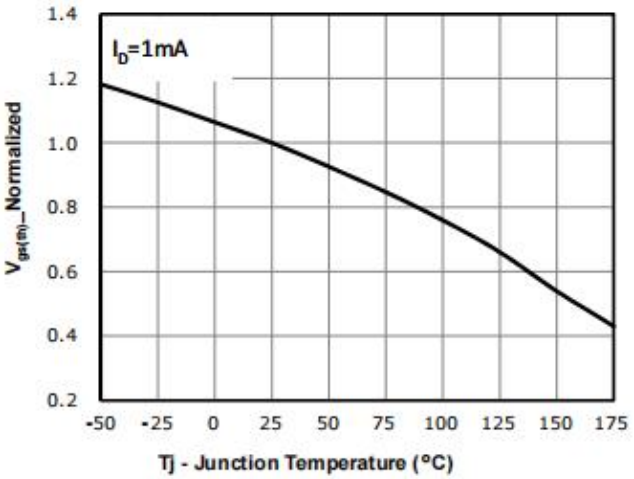


Fig 8: BVdss vs. Temperature

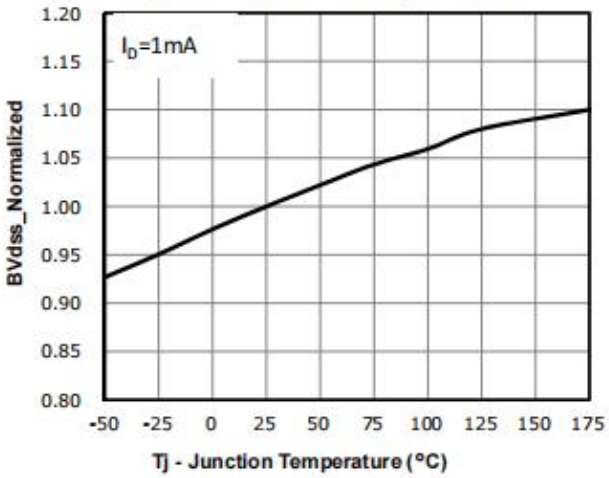


Fig 9: Gate Charge Characteristics

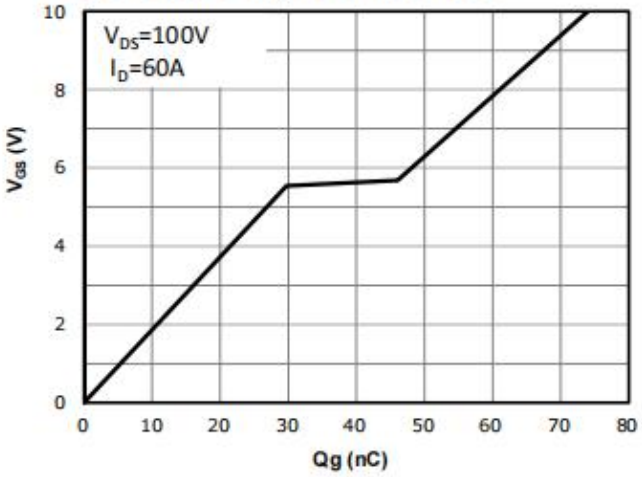


Fig 10: Body-diode Forward Characteristics

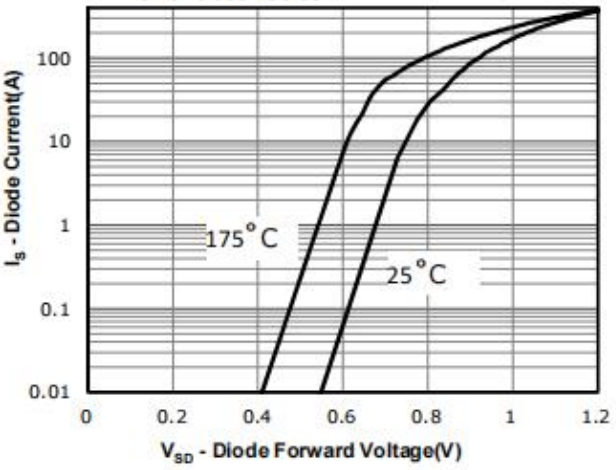


Fig 11: Power Dissipation

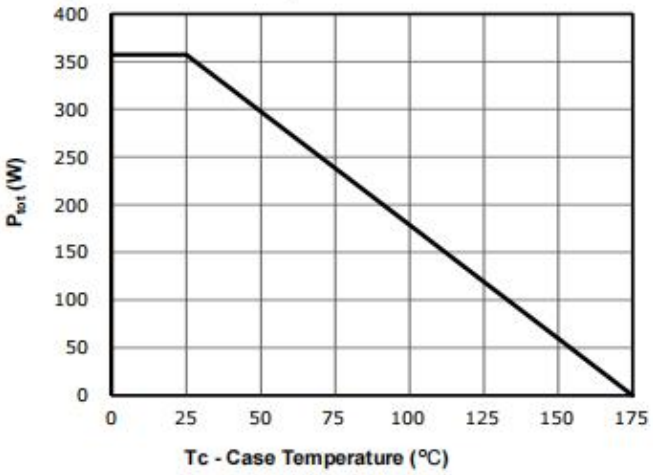


Fig 12: Drain Current Derating

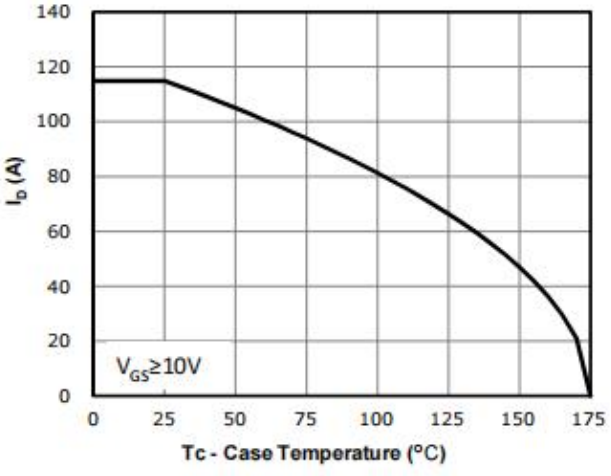


Fig 13: Safe Operating Area

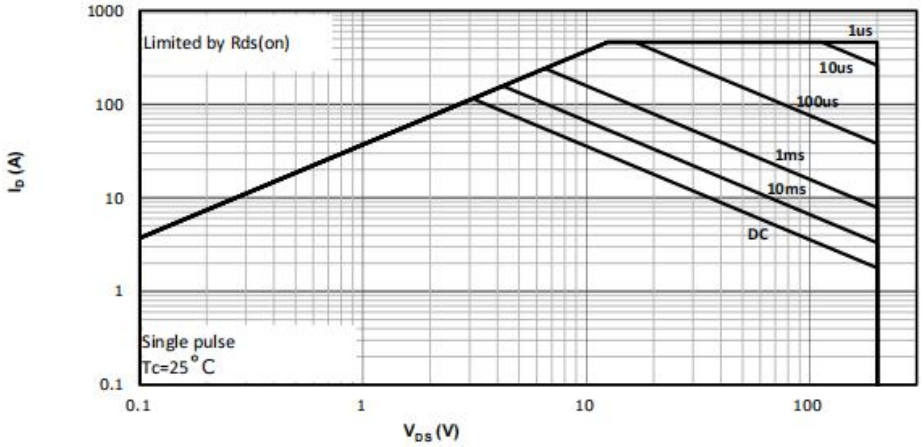
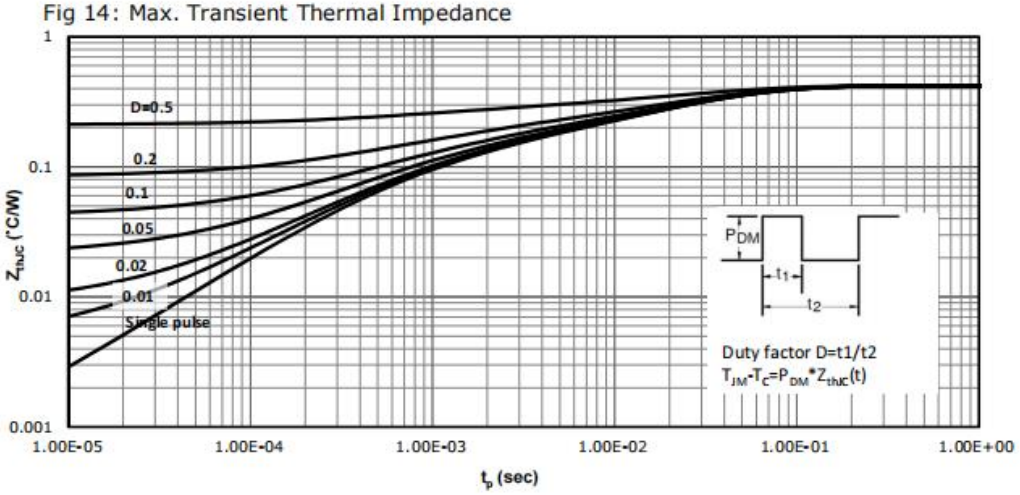
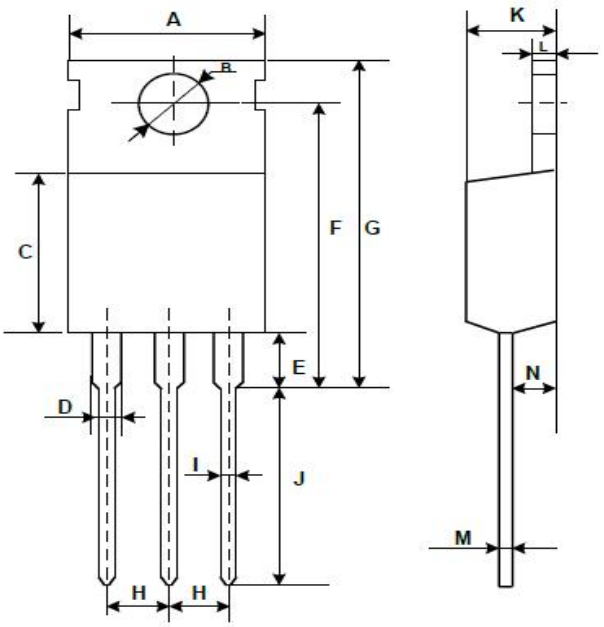


Fig 14: Max. Transient Thermal Impedance



Package Dimensions TO220



OMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60

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