UJ4C075060L8SSB-VB Datasheet
N-Channel 650V (D-S) SiC Power MOSFET

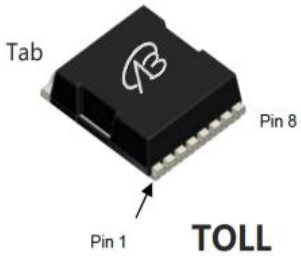
PRODUCT SUMMARY		
V_{DS} (V)	650	
$R_{DS(on)}$ at 25 °C (Ω)	V_{GS} = 18 V	0.055
Q_g (nC)	40	

FEATURES

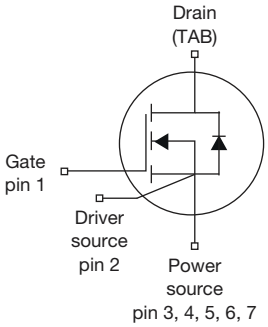
- Low figure-of-merit (FOM) R_{on} x Q_g
- Higher robustness and system reliability
- Kelvin source provides up to 4 times lower switching losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

APPLICATIONS

- Server and telecom power supplies
- EV charging infrastructure
- Solar PV inverters
- DC/DC converter



Top View



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	-10 / +22	
Continuous Drain Current (T_J = 175 °C)	V_{GS} at 18 V	T_C = 25 °C	I_D	35	A
		T_C = 100 °C		25	
Pulsed Drain Current [a]			I_{DM}	95	
Linear Derating Factor				2.1	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	160	mJ
Maximum Power Dissipation			P_D	192	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	150	V/ns
Reverse Diode dV/dt [d]				100	
Soldering Recommendations (Peak Temperature) [c]	for 10 s			260	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 1mH, R_g = 25 Ω.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.78	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 1 mA		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 5 mA		2	-	4.5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = +18 V		-	-	100	nA
		V_{GS} = - 8 V		-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0 V		-	10	-	μA
		V_{DS} = 650 V, V_{GS} = 0 V, T_J = 125 °C		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 18 V	I_D = 20A	-	0.055	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 0 V, I_D = 20 A		-	10	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 600 V, f = 100 KHz		-	1500	-	pF
Output Capacitance	C_{oss}			-	90	-	
Reverse Transfer Capacitance	C_{rss}			-	3	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		-	120	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$			-	160	-	
Total Gate Charge	Q_g	V_{GS} = -5/18 V	I_D = 20 A, V_{DS} = 400 V	-	40	-	nC
Gate-Source Charge	Q_{gs}			-	20	-	
Gate-Drain Charge	Q_{gd}			-	23	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D =20A V_{GS} = -5/15 V		-	12	15	ns
Rise Time	t_r			-	10	13	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	t_f			-	10	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	8.2	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	30	A
Pulsed Diode Forward Current	I_{SM}			-	-	90	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 20 A, V_{GS} = 0		-	-	4.1	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 20 A, dI/dt = 1000 A/μs, V_R = 400 V		-	12	-	ns
Reverse Recovery Charge	Q_{rr}			-	0.06	-	μC
Reverse Recovery Current	I_{RRM}			-	10	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 60 % V_{DSS}.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 60 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

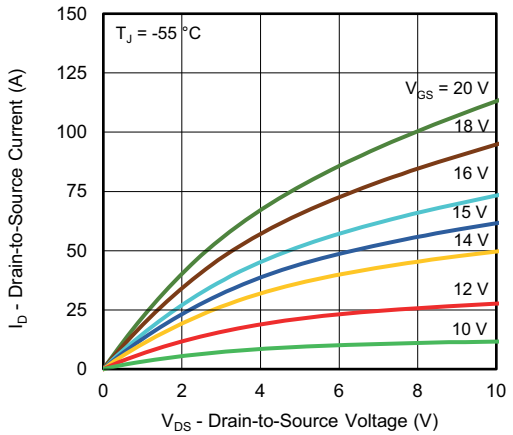


Fig. 1 - Typical Output Characteristics

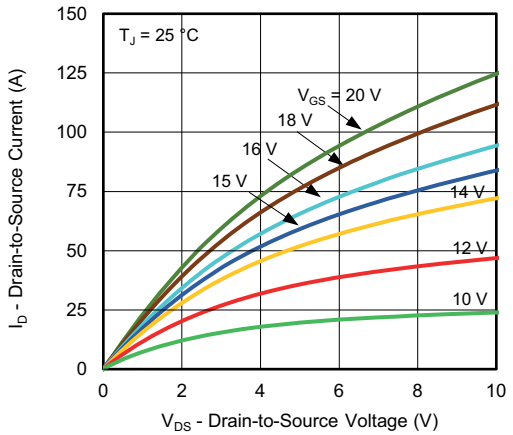


Fig. 2 - Typical Output Characteristics

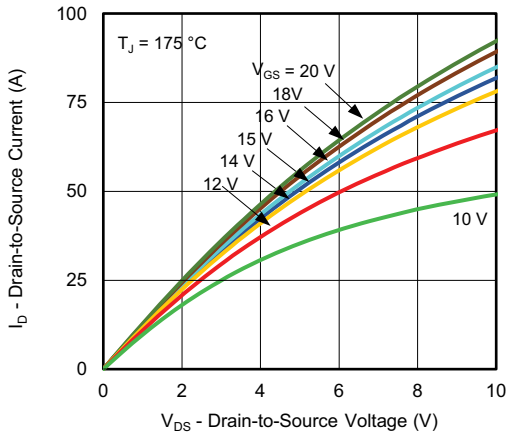


Fig. 3 - Typical Output Characteristics

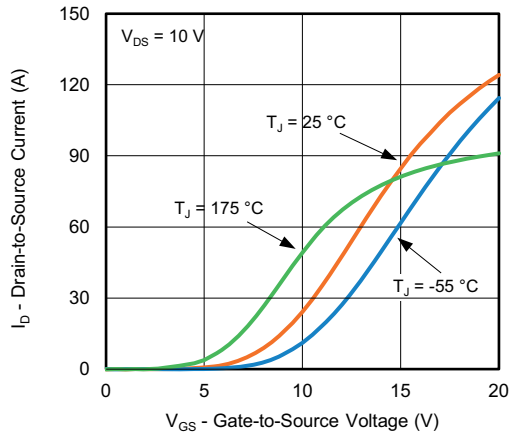


Fig. 4 - Typical Transfer Characteristics

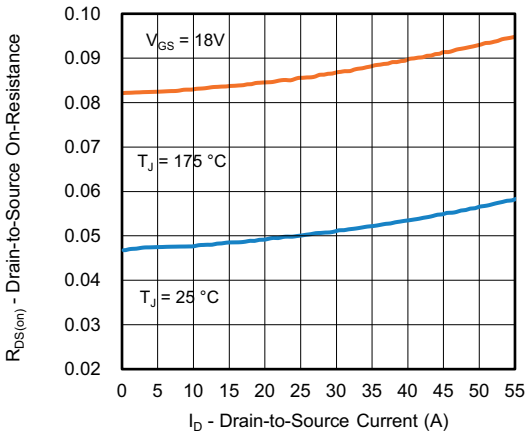


Fig. 5 - Normalized On-Resistance vs. Drain Current

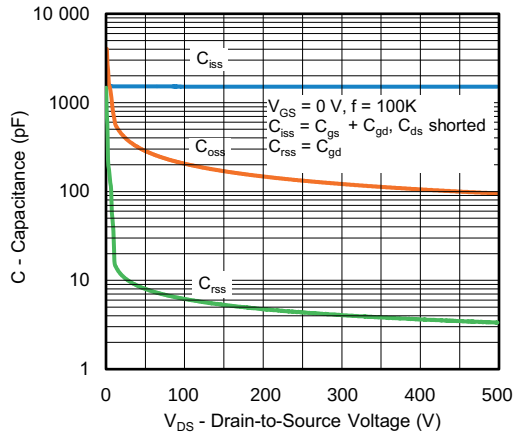


Fig. 6 - Typical Capacitance vs. Drain-to-Source Voltage

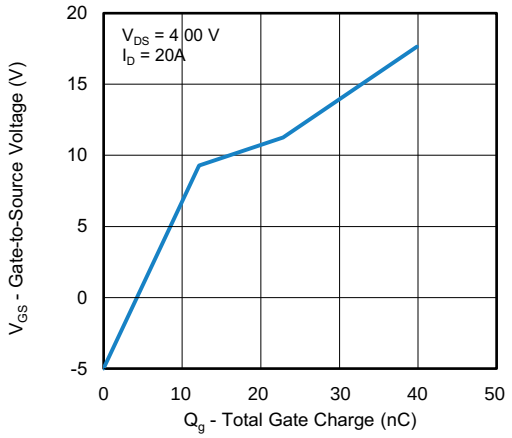


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

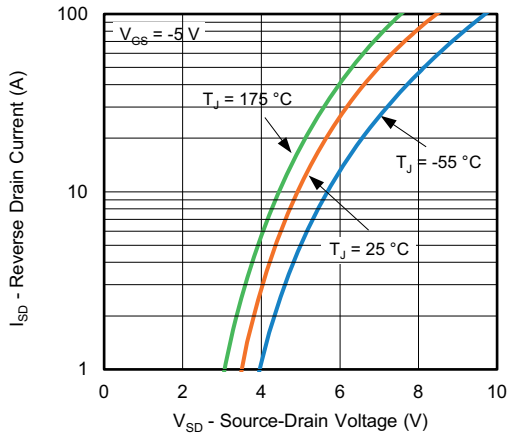


Fig. 10 - Typical Source-Drain Diode Forward Voltage

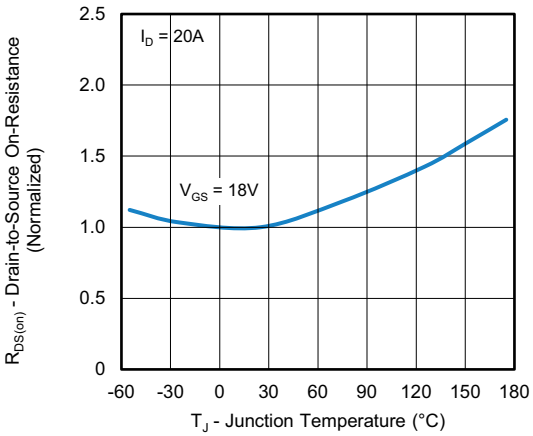


Fig. 8 - Normalized On-Resistance vs. Temperature

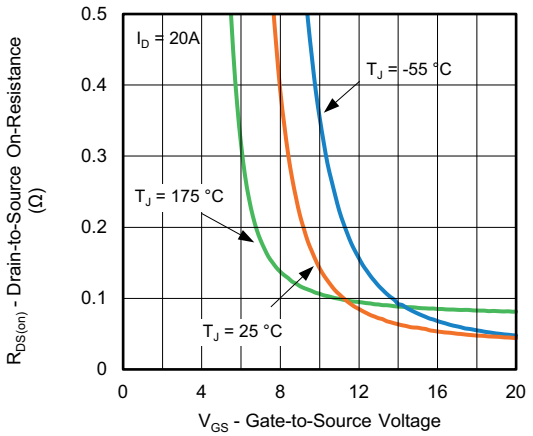


Fig. 11 - On-Resistance vs. Gate-to-Source Voltage

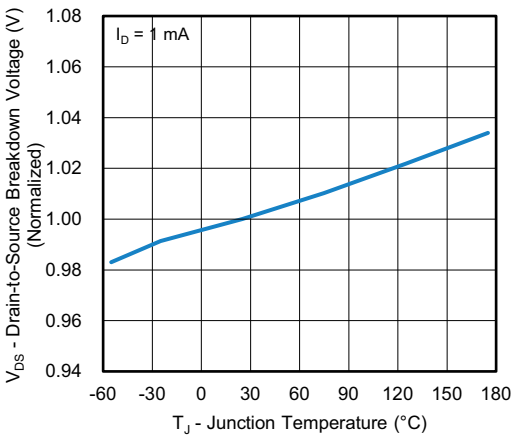


Fig. 9 - Drain-to-Source Voltage vs. Temperature

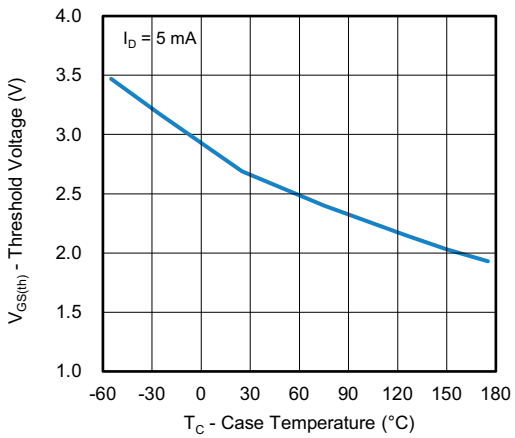


Fig. 12 - Threshold Voltage vs. Case Temperature

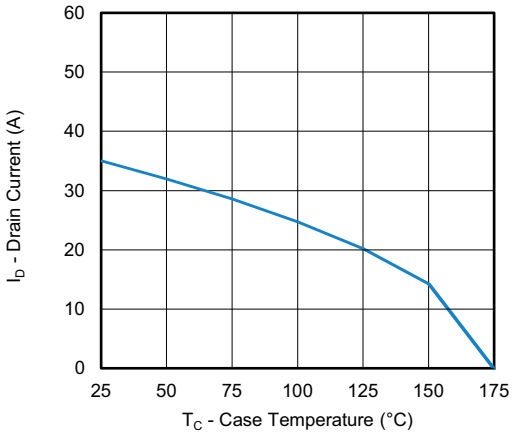


Fig. 13 - Drain Current vs. Case Temperature

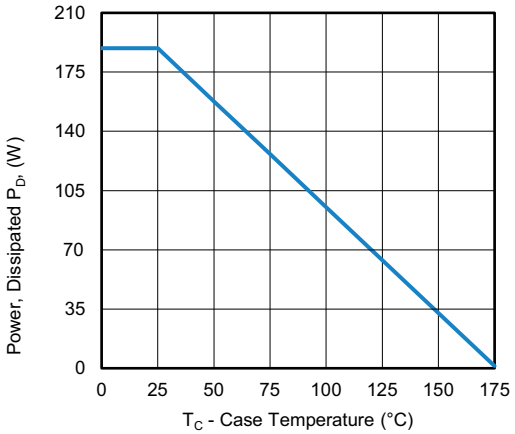


Fig. 15 - Power, Dissipated P_D vs. Case Temperature

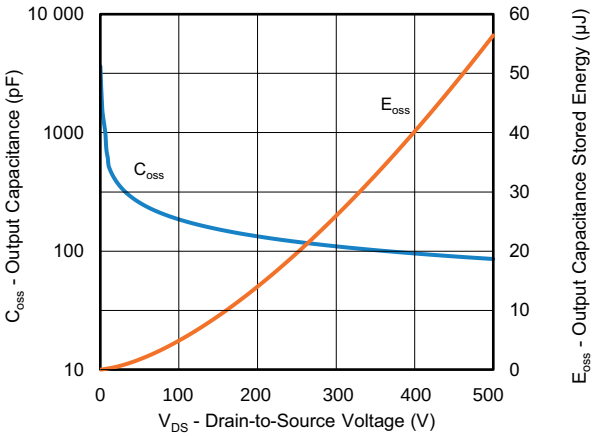


Fig. 14 - Output Capacitance and its Stored Energy vs. Drain-to-Source Voltage

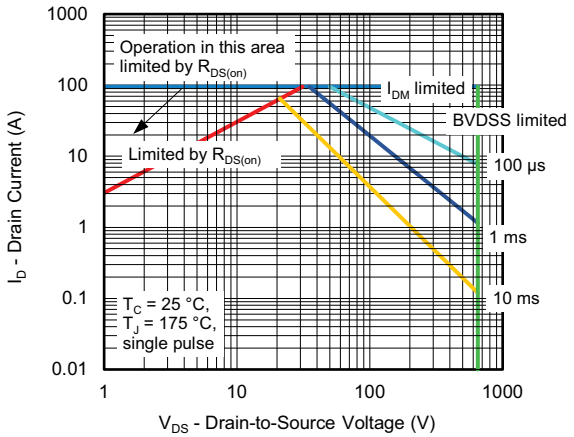


Fig. 16 - Safe Operating Area

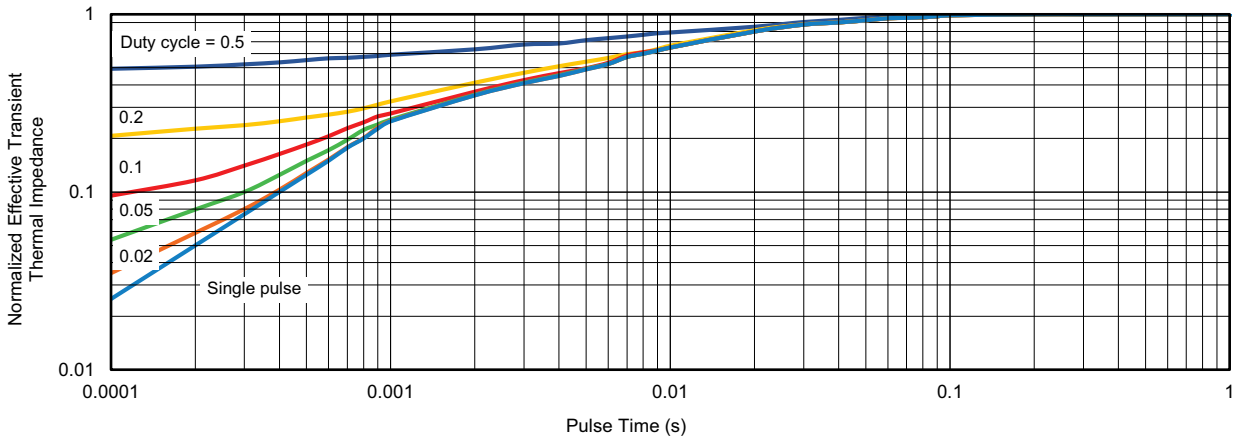


Fig. 17 - Transient Thermal Impedance

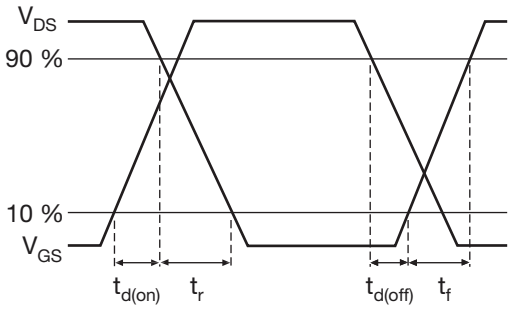


Fig. 18 - Waveforms of Switching Time

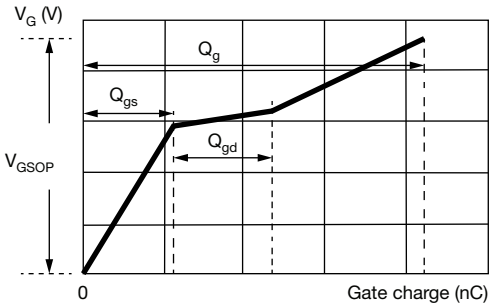


Fig. 21 - Waveforms for Gate Charge

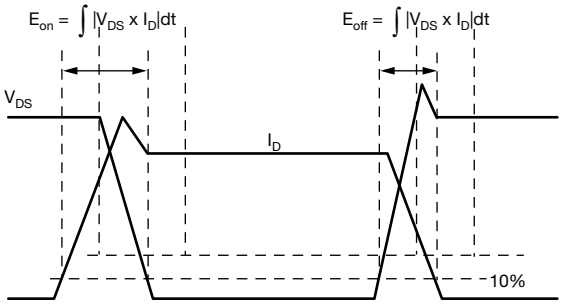


Fig. 19 - Waveforms for Switching Energy

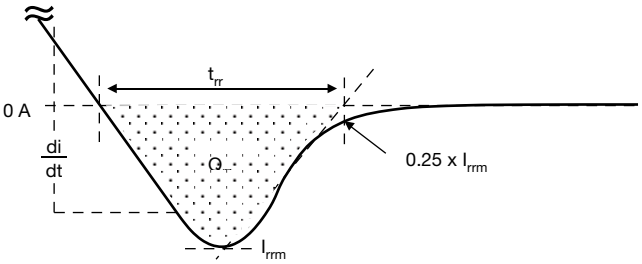


Fig. 22 - Waveforms for Reverse Recovery

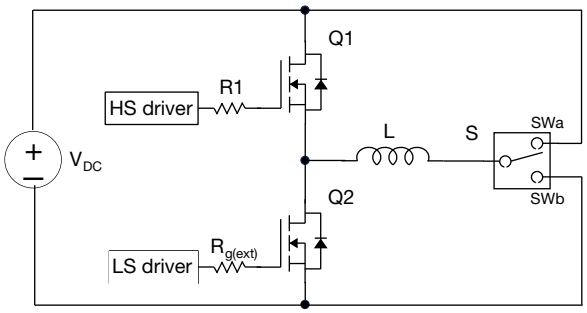


Fig. 20 - Switching and Reverse Diode Characteristics Measurement Circuit

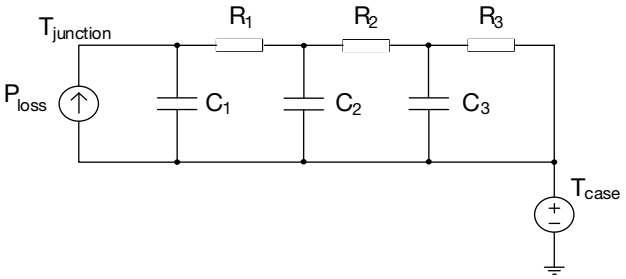
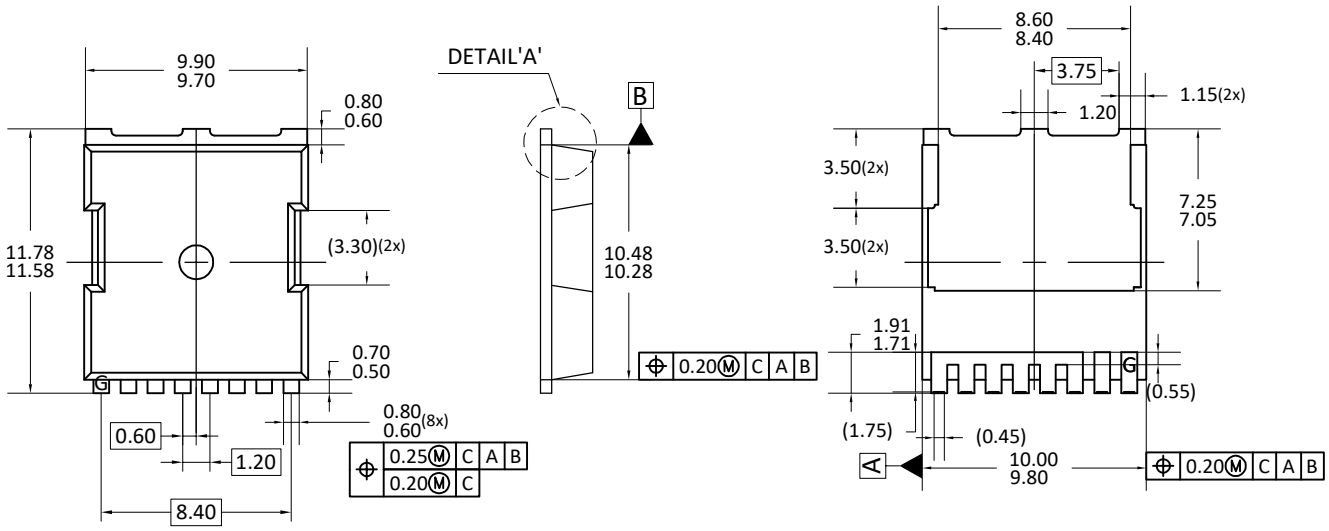
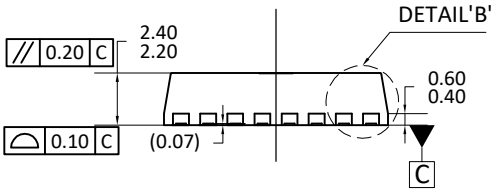


Fig. 23 - Thermal Equivalent Circuit

TOLL PACKAGE OUTLINE



TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

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