

## 250-mA, 3.3-V OUTPUT, LOW- $I_Q$ , LOW-DROPOUT LINEAR REGULATOR

### FEATURES

- Ultralow noise: 9  $\mu$ VRMS, independent of  $V_{OUT}$
- Ultralow quiescent current  
 $I_{GND} = 15 \mu A$  with zero load
- Maximum output current: 250 mA
- Input voltage range: 3.7 V to 5.5 V
- Output voltage: 3.3 V
- Output voltage tolerance:  $\pm 1\%$
- Low shutdown current:  $< 1 \mu A$
- Low dropout: 140 mV
- PSRR performance of 62 dB at 1 kHz
- No additional noise bypass capacitor required
- Stable with 1  $\mu F$  ceramic input and output capacitors
- Current limit and thermal overload protection
- Logic-controlled enable
- 5-Pin SOT-23 Package

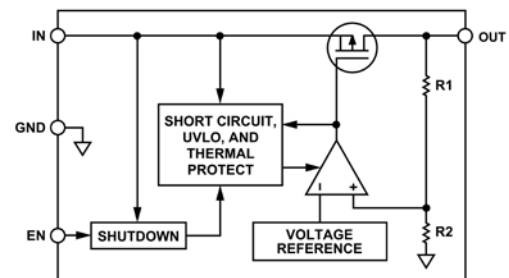
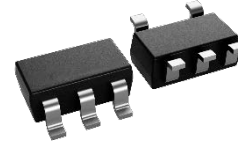


Figure 1. Functional Block Diagram

### APPLICATIONS

- Smartphones
- Tablets
- Communications equipment
- Digital still cameras
- Factory automation

## SPECIFICATIONS

at operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = 5.5\text{V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = 1\mu\text{F}$ , and  $C_{OUT} = 1\mu\text{F}$ , and  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage	$T_A = 25^{\circ}\text{C}$	3.7		5.5	V
$V_{OUT}$	Output voltage	$T_A = 25^{\circ}\text{C}$		3.3		V
	Output voltage accuracy	$I_{OUT} = 10\text{ mA}$ , $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	-1		+1	%
$V_{EN}$	Enable input voltage high	$3.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	2.0		5.5	V
	Enable input voltage low	$3.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	0		0.4	
$I_{OUT}$	Output current		0		250	mA
$I_{GND}$	Operating supply current	$V_{EN} = 5.5\text{ V}$ , $I_{OUT} = 0\text{ mA}$		15	28	$\mu\text{A}$
		$V_{EN} = 5.5\text{ V}$ , $I_{OUT} = 10\text{ mA}$		45	60	
		$V_{EN} = 5.5\text{ V}$ , $I_{OUT} = 250\text{ mA}$		270	320	
$I_G$	Shutdown current	$V_{EN} = \text{GND}$		0.2	0.7	$\mu\text{A}$
		$V_{EN} = \text{GND}$ , $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$			1	
$V_{DROP}$	Dropout voltage	$I_{OUT} = 10\text{ mA}$		10	50	mV
		$I_{OUT} = 100\text{ mA}$		80	100	
		$I_{OUT} = 250\text{ mA}$		140	260	
PSRR	Power-supply rejection ratio	1 KHz, $I_{OUT} = 10\text{ mA}$		62	65	dB
		10 KHz, $I_{OUT} = 10\text{ mA}$		60	64	
		100 KHz, $I_{OUT} = 10\text{ mA}$		55	58	
$OUT_{Noise}$	Output noise voltage	BW=10 Hz to 100 kHz		9	50	$\mu\text{V}_{rms}$
		BW=10 Hz to 100 kHz, $I_{OUT} = 1\text{ mA}$		9	27	
		BW=10 Hz to 100 kHz, $I_{OUT} = 100\text{ mA}$		10	35	

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

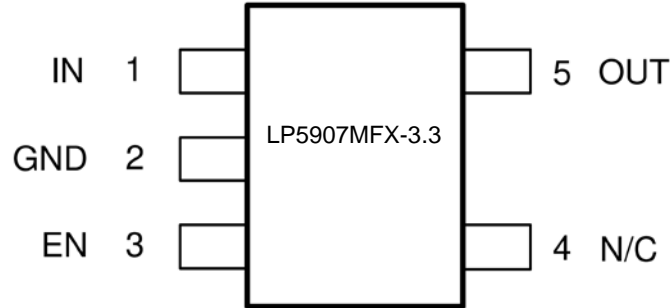


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
IN	1	Regulator Input Supply. Bypass IN to GND with a 1 $\mu$ F or greater capacitor
GND	2	The ground return for the supply and signals.
EN	3	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN.
N/C	4	No Connect. Not connected internally.
OUT	5	Regulated Output Voltage. Bypass OUT to GND with a 1 $\mu$ F or greater capacitor.

## TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the LP5907MFX-3.3. The default minimum recommended value for input/output capacitance is 1  $\mu$ F. In certain applications, input and output capacitors with a capacitance greater than 1  $\mu$ F may be selected. To enable default automatic startup, connect the EN (enable) pin directly to IN.

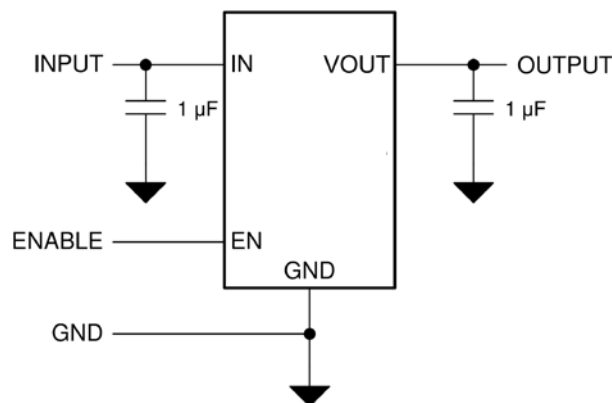
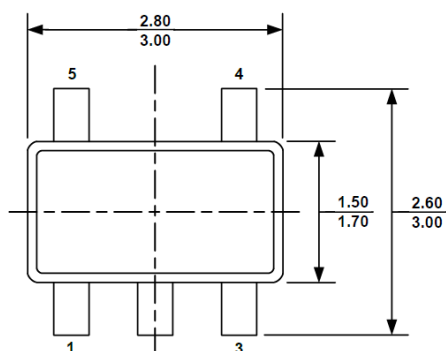
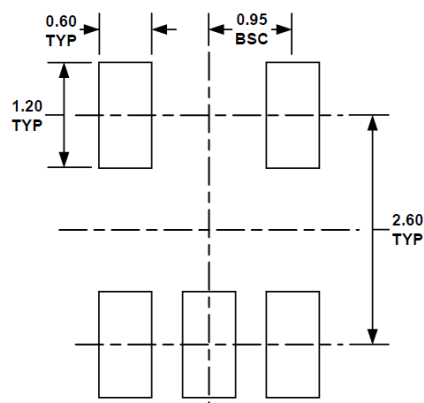


Figure 3. Typical Circuit Configuration

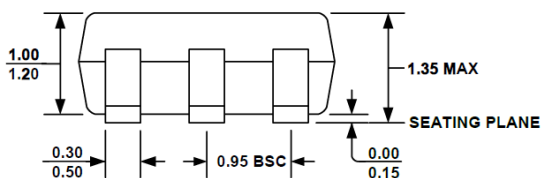
## OUTLINE DIMENSIONS



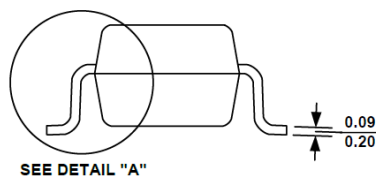
**TOP VIEW**



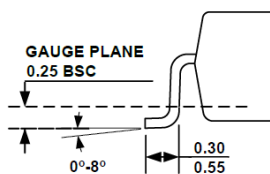
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

## NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.