13.56MHz reader/writer for contactless communication

Feature and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output driver with minimal peripheral components connected to the antenna
- Supports ISO/IEC 14443 A
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports ISO/IEC 14443 A higher rate communication, up to 848 kBd
- Supported host interfaces
  - -SPI up to 10 Mbit/s
  - -I^2C
  - -RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.6 V power supply
- CRC coprocessor

Quick reference data

Table 4-1 Limit parameter

Condition	Min	Max	Unit
Supply voltage			
VDD	-0.5	4	V
Temperature			
Operating temperature	-40	+85	℃

Table 4-2 Main parameter

Symbol	Parameter	Condition		Min	Typ	Max	Unit
VDDA	analog supply voltage	VDD(PVDD) ≤ VDDA = VDDD = VDD(TVDD); VSSA = VSSD = VSS(PVSS) = VSS(TVSS) = 0 V	(1)	2.5	3.3	4	V
VDDD	digital supply voltage			2.5	3.3	4	V
VDD(TVDD)	TVDD supply voltage			2.5	3.3	4	V
VDD(PVDD)	PVDD supply voltage		(1)	2.5	3.3	4	V
VDD(SVDD)	SVDD supply voltage	VSSA = VSSD = VSS(PVSS) = VSS(TVSS) = 0 V		2.5	3.3	4	V
Ipd	power-down current	VDDA=VDDD = VDD(TVDD) = VDD(PVDD) = 3.3 V					
		hard power-down; pin NRSTPD set LOW	(2)	-	1.2	1.5	uA
		soft power-down; RF level detector on	(2)	-	1.5	2.5	uA
IDDD	digital supply voltage	pin DVDD；VDDD = 3.3 V		-	0.9	1.5	uA
IDDA	analog supply voltage	pin AVDD；VDDA = 3.3 V，CommandReg register’s RcvOff bit = 0		-	2.9	4	mA
		pin AVDD；receiver switched off; VDDA = 3.3		-	0.8	1	mA

		V，CommandReg register's RcvOff bit = 1					
IDD(TVDD)			(3)	-	25	30	mA

(1) VDDA, VDDD and VDD(TVDD) must always be the same voltage.

(2) Ipd is the total current for all supplies.

(3)During typical circuit operation, the overall current is below 30 mA

Table 4-3 Recommend value

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDDA	Analog supply voltage	VDD(PVDD) ≤ VDDA = VDDD = VDD(TVDD); VSSA = VSSD = VSS(PVSS) = VSS(TVSS) = 0 V	2.5	3.3	4.0	V
VDDD	Digital supply voltage		2.5	3.3	4.0	V
VDD(TVDD)	TVDD supply voltage		2.5	3.3	4.0	V
VDD(PVDD)	PVDD supply voltage		2.5	3.3	4.0	V
VDD(SVDD)	SVDD supply voltage	VSSA = VSSD = VSS(PVSS) = VSS(TVSS) = 0V	2.5	3.3	4.0	V
	storage temperature	QFN32	-55	-	+125	℃
	operating temperature	QFN32	-40	-	+85	℃

Note:Stresses beyond those Absolute Maximum Ratings may cause permanent damage to the device.

Table 4-4 Version information

Chip code	Description
MFRC52202HN1	-

Block diagram

The analog interface handles the modulation and demodulation of the analog signals. The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host.The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART.

Various host interfaces are implemented to meet different customer requirements.

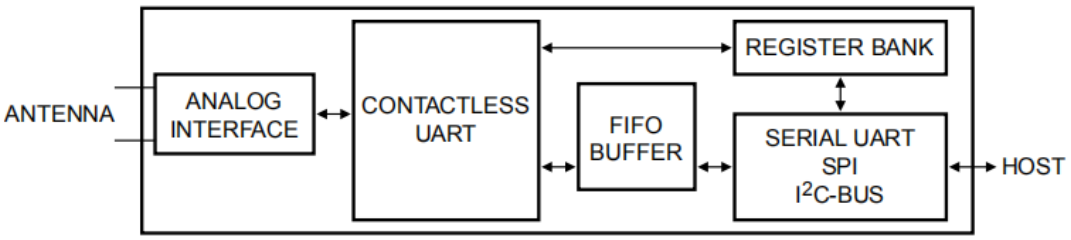

Figure 5-1 Simplified block diagram

Pinning information

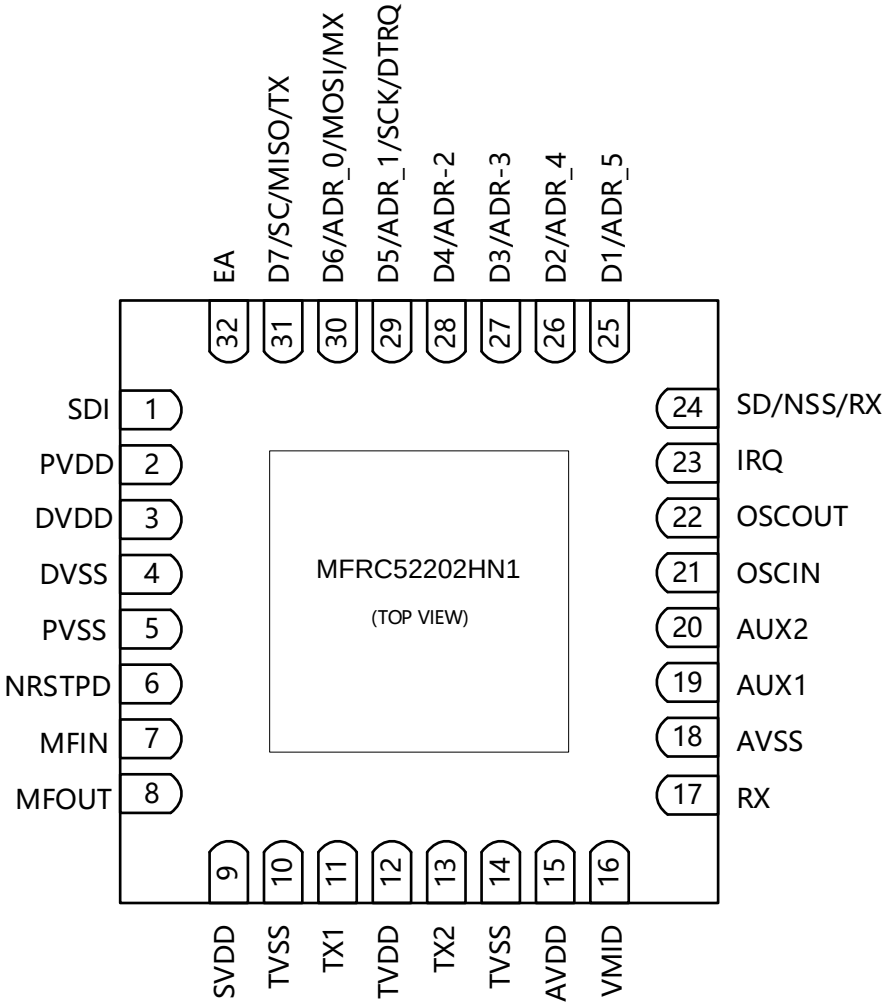

Figure 6-1 Pinning configuration (QFN32L)

Table 6-1 Pinning description

Pin	Symbol	Type[1]	Description
1	SDI	I	I^2C bus input
2	PVDD	P	Pad power supply
3	DVDD	P	Digital Power Supply
4	DVSS	P	Digital Ground
5	PVSS	P	Pad power supply ground
6	NRSTPD	I	Reset and Power Down input: When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are

			disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
7	MFIN	I	Test signal input
8	MFOUT	O	Test signal output
9	SVDD	P	Provides power to the MFIN/MFOUT
10	TVSS	P	Transmitter Ground: supplies the output stage of TX1 and TX2
11	TX1	O	Transmitter 1: delivers the modulated 13.56 MHz energy carrier
12	TVDD	P	Transmitter Power Supply: supplies the output stage of TX1 and TX2
13	TX2	O	Transmitter 2: delivers the modulated 13.56 MHz energy carrier
14	TVSS	P	Transmitter Ground: supplies the output stage of TX1 and TX2
15	AVDD	P	Analog Power Supply
16	VMID	P	Internal Reference Voltage: This pin delivers the internal reference voltage.
17	RX	I	Receiver Input
18	AVSS	P	Analog Ground
19	AUX1	O	Auxiliary Outputs: These pins are used for testing.
20	AUX2	O	Auxiliary Outputs: These pins are used for testing.
21	OSCIN	I	Crystal Oscillator Input: input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (fosc = 27.12 MHz).
22	OSCOUT	O	Crystal Oscillator Output: Output of the inverting amplifier of the oscillator.
23	IRQ	O	Interrupt Request: output to signal an interrupt event
24	SD	I/O	I^2C bus serial data input and output
	NSS	I	SPI input
	RX	I	UART address input
25	D1	I/O	Test port
	ADR_5	I/O	I^2C bus address5 input

26	D2	I/O	Test port
	ADR_4	I	I² C bus address4 input
27	D3	I/O	Test port
	ADR_3	I	I² C bus address3 input
28	D4	I/O	Test port
	ADR_2	I	I² C bus address2 input
29	D5	I/O	Test port
	ADR_1	I	I² C bus address1 input
	SCK	I	SPI seria clock input l
	DTRQ	O	UART makes a request to controller
30	D6	I/O	Test port
	ADR_0	I	I² C bus address0 input
	MOSI	I/O	SPI Master Out Slave In
	MX	O	UART for the output of the controller
31	D7	I/O	Test port
	SCL	I/O	I² C bus clock input/output
	MISO	I/O	SPI Master In Slave Out
	TX	O	UART Data output to controller
32	EA	I	External address input：can be used to define the I² C address

1) Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground

2) DVSS is the connection of heatsink pad on package underside.

Functional description

The 52202 transmission module supports the Read/Write mode for ISO/IEC 14443 A using various transfer speeds and modulation protocols.

Table7-1 Communication overview for ISO/IEC 14443 A reader/writer

Communication direction	Signal type	Transfer speed			
		106kBd	212kBd	424kBd	848kBd
Reader to card (send data from the 52202 to a card)	reader side modulation	100%ASK	100%ASK	100%ASK	100%ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	（128/13.56）μs	（64/13.56）μs	（32/13.56）μs	（16/13.56）μs
Card to reader (52202 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16	13.56MHz/16
	bit encoding	Manchester	BPSK	BPSK	BPSK

The 52202's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A protocol. Figure 7-1 shows the data coding and framing according to ISO/IEC 14443 A.

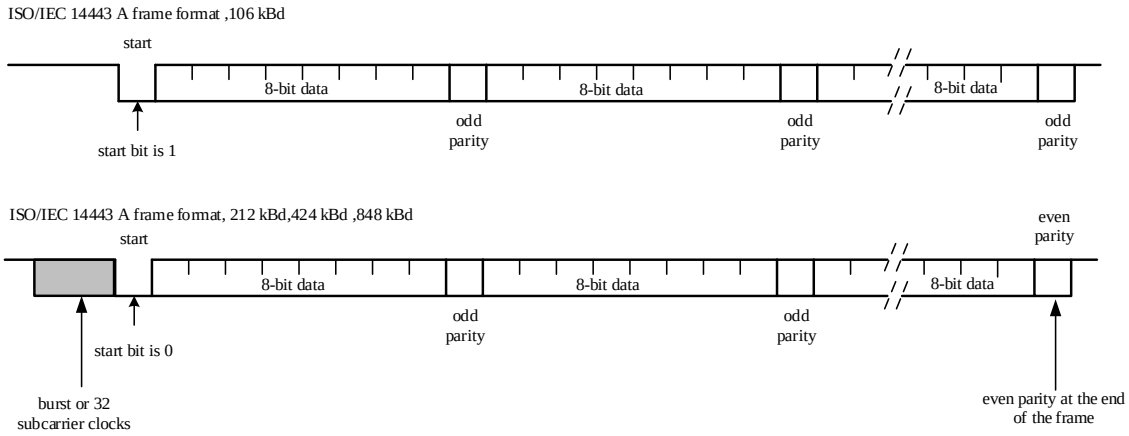

Figure 7-1 Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally based on the transmission rates.

Automatic parity generation can be switched off using the ManualRCVReg register's ParityDisable bit.

Digital interfaces

Automatic microcontroller interface detection

The 52202 supports direct interfacing of hosts using SPI, I² C or serial UART interfaces. The 52022 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The 52202 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 7-1 shows the different connection configurations.

Table 7-2 Connection protocol for detecting different interface types

Pin	Interface types		
	UART（input）	SPI（output）	I² C（I/O）
SD	RX	NSS	SD
SDI	0	0	1
EA	0	1	EA
D7	TX	MISO	SC
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

SPI

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the 52202 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface

communication.

An interface compatible with SPI enables high-speed serial communication between the 52202 and a microcontroller. The implemented interface is in accordance with the SPI standard.

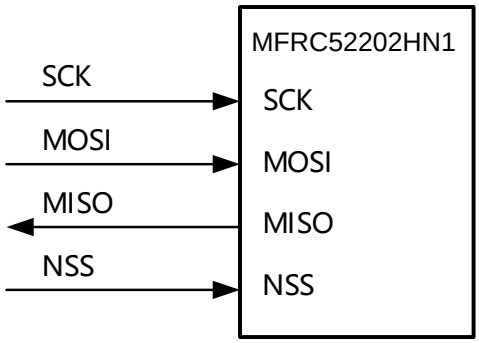

Figure 7-2 SPI connection to host

The 52022 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the 52202 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the 52202 on the falling clock edge and is stable during the rising clock edge.

SPI read data

Reading data using SPI requires the byte order . It is possible to read out up to n-data bytes.The first byte sent defines both the mode and the address.

Table7-3 MOSI and MISO byte order

Line	Byte0	Byte1	Byte2	To	Byte n	Byte n+1
MOSI	address 0	address 1	address 2	…	address n	00
MISO	X	data 0	data 1	…	data n-1	data n

NOTE: The MSB must be sent first.

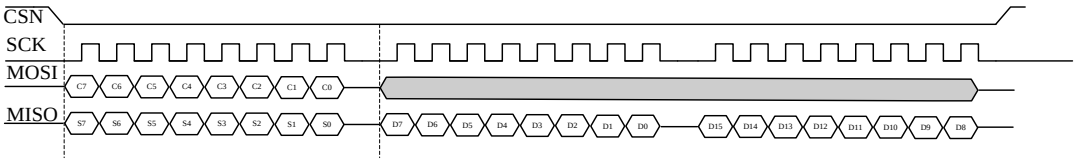

Figure 7-3 SPI read timing

SPI write data

To write data to the 52202 using SPI requires the byte order shown in Table 7-4. It is possible to write up to n data bytes by only sending one address byte.The first send byte defines both the mode and the address byte.

Table7-4 MOSI and MISO Byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n+1
MOSI	address 0	data 0	data 1	…	data n-1	data n
MISO	X	X	X	…	X	X

NOTE: The MSB must be sent first.

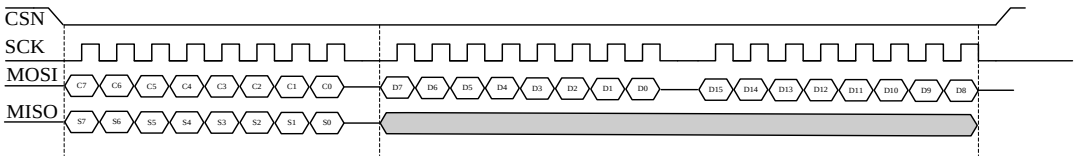

Figure 7-4 SPI write timing

SPI timing

SPI typical timing is shown in Figure 7-5 and SPI typical timing parameter is shown in Table 7-5.

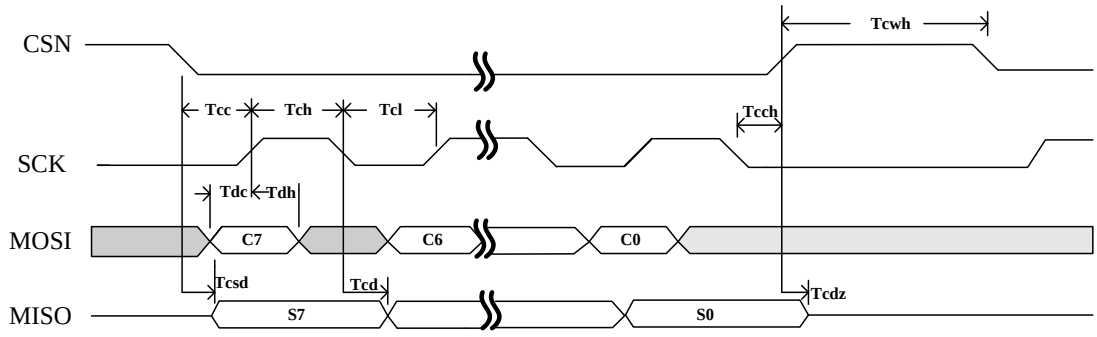

Figure 7-5 SPI typical timing

Table 7-5 SPI typical timing parameter

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

SPI address byte

The address byte has to meet the following format.The MSB of the first byte defines the mode used. To read data from the 52202the MSB is set to logic 1. To write data to the 52202the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

Table7-6　Address byte format

7（MSB）	6：1	0（LSB）
1=read/0=write	Address	0

UART interface

Connection to a host

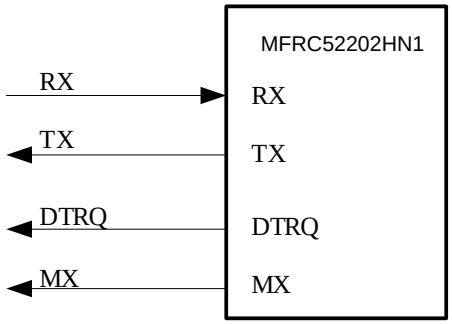

Figure7-6 UART connection to microcontrollers

NOTE: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

Selectable UART transfer speeds

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register. Different transfer speeds and relevant registers setting are shown in Table 7-7.

Table7-7 Selectable UART transfer speeds

Transfer speed （kBd）	SeriaSpeedReg value		Transfer speed accuracy （%）
	Decimal	Hexadecimal	
7.2	250	FAh	-0.25
8.6	235	EBh	0.32
14.4	218	DAh	-0.25
19.2	203	CBh	0.32

38.4	171	ABh	0.32
57.6	154	9Ah	-0.25
115.2	122	7Ah	-0.25
128	116	74h	-0.06
230.4	90	5Ah	-0.25
460.8	58	3Ah	-0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

The selectable transfer speeds shown in table above are calculated according to the following equations:

When BR_T0[2:0] = 0：

$$\text{transfer speed} = (27.12 \times 10^6) / (\text{BR\_T0} + 1)$$

When BR_T0[2:0] > 0：

$$\text{transfer speed} = (27.12 \times 10^6 \times 2^{(\text{BR\_T0} - 1)}) / (\text{BR\_T1} + 33)$$

NOTE: Transfer speed more than 1228.8kBd is not supported.

UART framing

Table7-8 UART framing

Bit	Length	Value
Start	1bit	0
Data	8bits	Data
Stop	1bit	1

NOTE: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

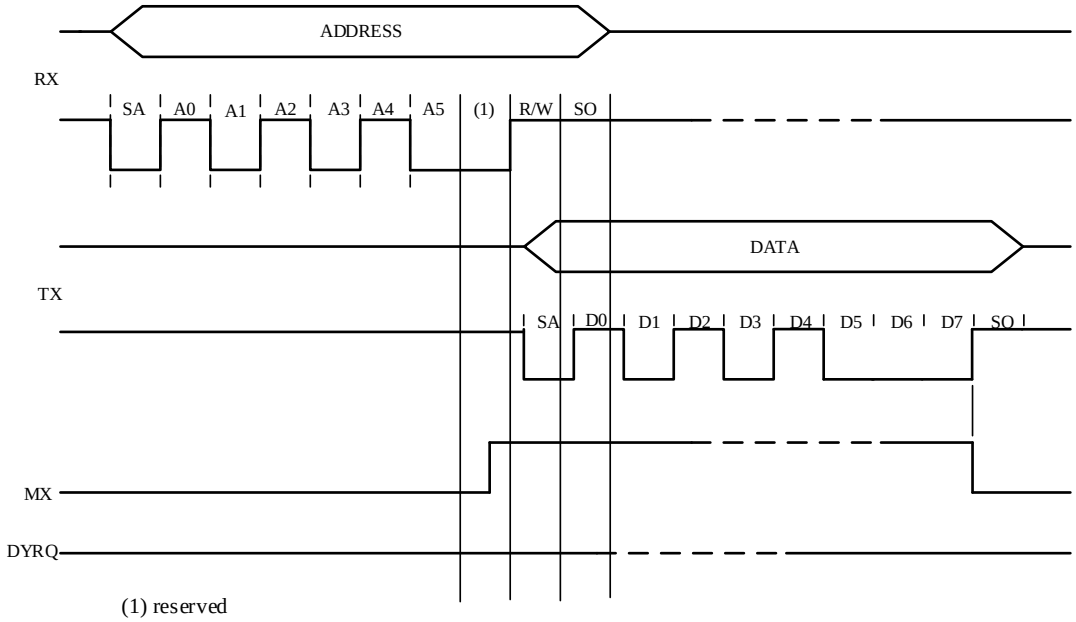

Figure 7-7 UART read timing

Read data: To read data to the 52202 using the UART interface, the structure shown in Table 7-9 must be used. The first byte sent defines both the mode and the address.

Table7-9 Read data byte order

Pin	Byte0	Byte1
RX	address	-
TX	-	data 0

Write data: To write data to the 52202 using the UART interface, the structure shown in Table 7-10 must be used. The first byte sent defines both the mode and the address.

Table7-10 Write data byte order

Pin	Byte0	Byte1
RX	address0	data 0
TX	-	address0

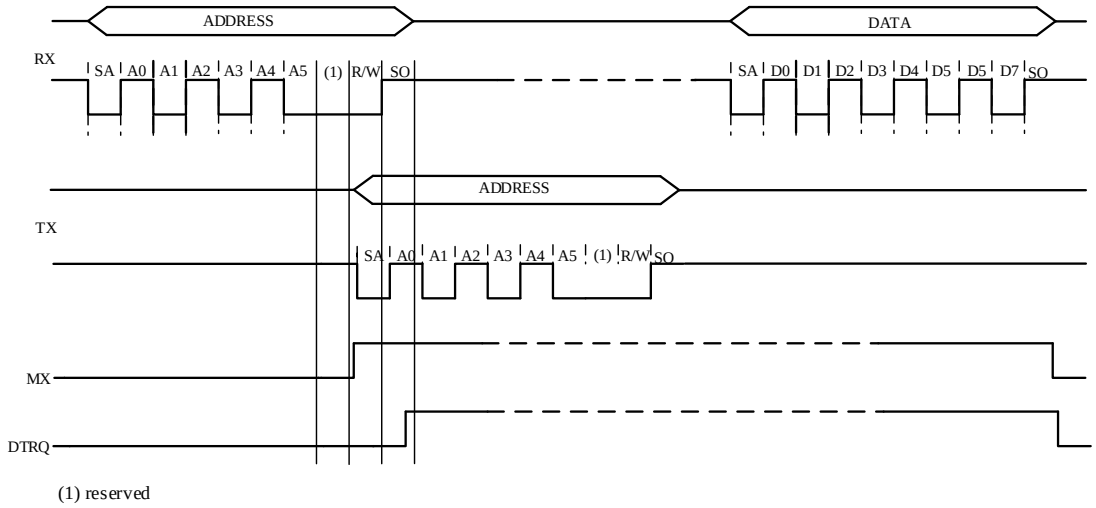

Figure 7-8 UART write timing

I²C

I² C is compatible

FIFO

An 64x8 bit FIFO buffer is used in the 52202. It buffers the input and output data stream between the host and the 52202's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

The 52202 can generate two interrupts signal to know the condition of the FIFO buffer in time: HiAlertIRq 和 LoAlertIRq.

If the maximum number of WaterLevel[5:0] bits (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. If it

enables interrupt,the HiAlertIRq will be generated.

$$HiAlert = (64 - FIFOLength) \leq WaterLevel$$

If the number of WaterLevel[5:0] bits (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1.If it enables interrupt,the LoAlertIRq will be generated.

$$LoAlert = FIFOLength \leq WaterLevel$$

Interrupt request system

The 52202 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ.

Table7-11 Interrupt sources

Interrupt flag	Interrupt source	Trigger action
IRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIRqReg	command execution finishes
HiAlertIRq	FIFO	the FIFO buffer is almost full
LoAlertIRq	FIFO	the FIFO buffer is almost empty
ErrIRq	Contactless UART	an error is detected

Power reduction modes

Hard power -down

Hard power-down mode is enabled when pin NRSTPD is LOW. After exiting hard power-down mode, all registers will be reset.

Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's

PowerDown bit is set to logic 1. During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

Transmitter power -down mode

The Transmitter Power-down mode switches off the internal antenna drivers thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

Command set

General description

The 52202 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code to the CommandReg register.

General characteristics

1) Except for the Transmive command, commands that require a data bit stream (or data byte stream) as input immediately process any data in the FIFO buffer. When the Transmive command is executed, the sending of data is initiated by the StartSend bit of the BitFramingReg register.

2) Commands that require a certain number of parameters are only processed when the correct number of parameters are received from the FIFO buffer.

3) At the beginning of the command, the FIFO buffer will not be automatically cleared. It supports writing command parameters and data bytes to the FIFO buffer, and then starting the command.

4) The host writes a new command code to the CommandReg register to interrupt the currently executing command, such as the Idle command.

Command overview

Table8-1 command overview

Command	Command code	Description
Idle	0000	no action, cancels current command execution
Mem	0001	Store 25 bytes in FIFO buffer
Generate RandomID	0010	IDgenerates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self test
Transmit	0100	transmits data from the FIFO buffer

NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
SoftReset	1111	resets the MFRC52202HN1

Register mapping

Table 9-1 52202 register mapping

Address (Hex)	Mnemonic	Bit	Type	Reset Value	Description
00h	reserved			00h	reserved for future use
01h	CommandReg			20h	starts and stops command execution
	reserved	7:6	-		write 0 by default
	RcvOff	5	R/W		1: analog part of the receiver is switched off
	PowerDown	4	D		1: Soft Power-down mode entered 0: 52202 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the 52202 is ready. NOTE: The PowerDown bit cannot be set when the SoftReset command is activated
	Command[3:0]	3:0	D		activates a command based on the Command value; reading this register shows which command is executed
02h	CommIEnReg			80h	enable and disable interrupt request control bits
	IRqInv	7	R/W		1：signal on pin IRQ is inverted with respect to the Status1Reg register's IRq bit 0：signal on pin IRQ is equal to the IRq bit; in combination with the DivIEnReg register's IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state
	TxIEn	6	R/W		1: allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ
	RxIEn	5	R/W		1：allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ
	IdleEn	4	R/W		1：allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ

	HiAlertIEn	3	R/W		1：allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ
	LoAlertIEn	2	R/W		1：allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ
	ErrIEn	1	R/W		1：allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ
	TimerIEn	0	R/W		1：allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ
03h	DivIEnReg			00h	enable and disable interrupt request control bits
	IRQPushPull	7	R/W		1：pin IRQ is a standard CMOS output pin 0：pin IRQ is an open-drain output pin
	reserved	6:5	-		write 0 by default
	SiginActIEn	4	R/W		1: allows MFIN interrupt request to be propagated to pin IRQ
	reserved	3	-		reserved for future use
	CRCIEn	2	R/W		1: allows the CRC interrupt request, indicated by the DivIrqReg register's CRCIRq bit, to be propagated to pin IRQ
	reserved	1:0	-		reserved for future use
04h	CommIRqReg			14h	interrupt request bits
	Set1	7	W		1: indicates that the marked bits in the ComIrqReg register are set 0: indicates that the marked bits in the ComIrqReg register are cleared
	TxIRq	6	D		1: set immediately after the last bit of the transmitted data was sent out
	RxIRq	5	D		1: receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are

					available in the FIFO
	IdleIRq	4	D		1: if a command terminates, for example, when the CommandReg changes its value from any command to the Idle command； if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set; if the microcontroller starting the Idle command does not set the IdleIRq bit
	HiAlertIRq	3	D		1：the Status1Reg register’s HiAlert bit is set the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
	LoAlertIRq	2	D		1: Status1Reg register’s LoAlert bit is set the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
	ErrIRq	1	D		1: any error bit in the ErrorReg register is set
	TimerIRq	0	D		1: the timer decrements the timer value in register TCounterValReg to zero
05h	DivIRqReg			x0h	interrupt request bits
	Set2	7	W		1：indicates that the marked bits in the DivIrqReg register are set 0：indicates that the marked bits in the DivIrqReg register are cleared
	reserved	6:5	-		reserved for future use
	SiginActIRq	4	D		1：MFIN active this interrupt bit will be set to logic 1when detecting a rising edge or a falling edge
	reserved	3	-		reserved for future use
	CRCIRq	2	D		1：the CalcCRC command is active and all data is

					processed
	reserved	1:0	-		reserved for future use
06h	ErrorReg			00h	error bits showing the error status of the last command executed
	WrErr	7	R		1：data is written into the FIFO buffer by the host if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface
	TempErr	6	R		1: internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off
	reserved	5	-		reserved for future use
	BufferOvfl	4	R		1：the host or a 52202’s internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full
	CollErr	3	R		1：a bit-collision is detected cleared automatically at receiver start-up phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd
	CRCErr	2	R		1:the RxModeReg register’s RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase
	ParityErr	1	R		1：parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A communication at 106 kBd
	ProtocolErr	0	R		1：SOF is incorrect automatically cleared during receiver start-up phase bit

					is only valid for 106 kBd
07h	Status1Reg			21h	communication status bits
	reserved	7	-		reserved for future use
	CRCOk	6	R		1：the CRC result is zero the CRCOk bit is undefined for data transmission and reception: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1
	CRCReady	5	R		1：the CRC calculation has finished; only valid for the CRC coprocessor calculation using the CalcCRC command
	IRq	4	R		indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers
	TRunning	3	R		1：MFRC523's timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock NOTE: in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register's TGated[1:0] bits; this bit is not influenced by the gated signal
	reserved	2	-		reserved for future use
	HiAlert	1	R		1：the alert level for the number of bytes in the FIFO buffer (FIFO Length[6:0]) is: HiAlert = (64-FIFOLength)≤WaterLevel Example: FIFO Length = 60, WaterLevel = 4 -> HiAlert = 1

					FIFO Length = 59, WaterLevel = 4 -> HiAlert = 0
	LoAlert	0	R		1：the alert level for number of bytes in the FIFO buffer (FIFO Length[6:0]) is: LoAlert = FIFOLength≤WaterLevel Example： FIFO Length = 4, WaterLevel = 4 -> LoAlert = 1 FIFO Length = 5, WaterLevel = 4 -> LoAlert = 0
08h	Status2Reg			00h	receiver and transmitter status bits
	TempSensClear	7	R/W		1：clears the temperature error if the temperature is below the alarm limit of 125 °C
	reserved	6:3	-		reserved
	ModemState[2:0]	2:0	R		shows the state of the transmitter and receiver state machines: 000：idle 001：wait for the BitFramingReg register's StartSend bit 010：TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1. The minimum time for TxWait is defined by the TxWaitReg register 011：transmitting 100：RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1. The minimum time for RxWait is defined by the RxWaitReg register 101：wait for data 110：receiving
09h	FIFODataReg			xxh	input and output of 64 byte FIFO buffer
	FIFOData[7:0]	7:0	D		data input and output port for the internal 64-byte FIFO

					buffer. FIFO buffer acts as parallel in/parallel out converter for all serial data stream inputs and outputs
0Ah	FIFOLevelReg			00h	number of bytes stored in the FIFO buffer
	FlushBuffer	7	W		1：immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit. Reading this bit always returns 0
	FIFOLevel[6:0]	6:0	R		indicates the number of bytes stored in the FIFO buffer. Writing to the FIFODataReg register increments and reading decrements the FIFOLevel value
0Bh	WaterLevelReg			08h	level for FIFO underflow and overflow warning
	reserved	7:6	-		reserved for future use
	WaterLevel[5:0]	6:0	R/W		defines a warning level to indicate a FIFO buffer overflow or underflow: Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel[5:0] bits Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel[5:0] bits in the FIFO buffer
0Ch	ControlReg			10h	miscellaneous control registers
	TStopNow	7	W		1：timer stops immediately. reading this bit always returns it to 0
	TStartNow	6	W		1：timer starts immediately. reading this bit always returns it to 0
	reserved	5:3	-		reserved for future use
	RxLastBits[2:0]	2:0	R		indicates the number of valid bits in the last received byte. If this value is zero, the whole byte is valid
0Dh	BitFramingReg			00h	adjustments for bit-oriented frames

	StartSend	7	W		1：starts the transmission of data only valid in combination with the Transceive command
	RxAlign[2:0]	6:4	R/W		used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example: 0：LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1 1：LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2 7：LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0 these bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0
	reserved	3	-		reserved for future use
	TxLastBits[2:0]	2:0	R/W		used for transmission of bit oriented frames: defines the number of bits of the last byte that will be transmitted. 000b indicates that all bits of the last byte will be transmitted
0Eh	CollReg			xxh	bit position of the first bit-collision detected on the RF interface
	ValuesAfterColl	7	R/W		0：all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1
	reserved	6	-		reserved for future use
	CollPosNotValid	5	R		1：no collision detected or the position of the collision is out of the range of CollPos[4:0]
	CollPos[4:0]	4:0	R		shows the bit position of the first detected collision in a received frame only data bits are interpreted example:

					00h：indicates a bit-collision in the 32nd bit 01h：indicates a bit-collision in the 1st bit 08h：indicates a bit-collision in the 8th bit these bits will only be interpreted if the CollPosNotValid bit is set to logic 0
0Fh	reserved			08h	reserved for future use
10h	reserved			00h	reserved for future use
11h	ModeReg			3Fh	defines general modes for transmitting and receiving
	MSBFirst	7	R/W		1：CRC coprocessor calculates the CRC with MSB first. In the CRCResultReg register the values for the CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed NOTE: during RF communication this bit is ignored
	reserved	6	-		reserved for future use
	TxWaitRF	5	R/W		1：transmitter can only be started if an RF field is generated
	reserved	4	-		reserved for future use
	PolSigin	3	R/W		define the polarity of pin MFIN
	reserved	2	-		reserved for future use
	CRCPreset	1:0	R/W		defines the preset value for the CRC coprocessor for the CalcCRC command NOTE: during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers 00：0000h 01：6363h 10：A671h 11：FFFFh
12h	TxModeReg			00h	defines transmission data rate and framing

	TxCRCEn	7	R/W		1：enables CRC generation during data transmission NOTE: it can only be set to logic 0 at 106 kBd
	TxSpeed[2:0]	6:4	D		defines the bit rate during data transmission. 52202 handles transmission rates up to 848 kBd 000:106kBd 001:212kBd 010:424kBd 011:848kBd 100-111：reserved
	InvMod	3	R/W		1：modulation of transmitted data is inverted
	reserved	2:0	-		reserved
13h	RxModeReg			00h	defines transmission data rate and framing
	RxCRCEn	7	R/W		1：enables CRC generation during data transmission NOTE: it can only be set to logic 0 at 106 kBd
	RxSpeed[2:0]	6:4	D		defines the bit rate during data transmission. 52202 handles transmission rates up to 848 kBd 000:106kBd 001:212kBd 010:424kBd 011:848kBd 100-111：reserved
	RxNoErr	3	R/W		1：modulation of transmitted data is inverted
	RxMultiple	2	R/W		reserved
	reserved	1:0	-		defines transmission data rate and framing
14h	TxControlReg			80h	controls the antenna driver pins TX1 and TX2
	InvTx2RFOn	7	R/W		1：output signal on pin TX2 inverted when driver TX2 is enabled
	InvTx1RFOn	6	R/W		1：output signal on pin TX1 inverted when driver TX1 is enabled

	InvTx2RFOff	5	R/W		1：output signal on pin TX2 inverted when driver TX2 is disabled
	InvTx1RFOff	4	R/W		1：output signal on pin TX1 inverted when driver TX1 is disabled
	Tx2CW	3	R/W		1：output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier 0：Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier
	reserved	2	-		reserved for future use
	Tx2RFEn	1	R/W		1：output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data
	Tx1RFEn	0	R/W		1：output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data
15h	TxAutoReg			00h	controls the setting of the transmission modulation
	reserved	7	-		reserved for future use
	Force100ASK	6	R/W		1：forces 100 % ASK modulation independently of the ModGsPReg register setting
	reserved	5:0	-		reserved for future use
16h	TxSelReg			10h	selects the internal sources for the antenna driver
	reserved	7:6	-		reserved for future use
	DriverSel[1:0]	5:4	R/W		selects the input of drivers TX1 and TX2 00：3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode 01：modulation signal (envelope) from the internal encoder, Miller pulse encoded 10：reserved 11：HIGH; the HIGH level depends on the setting of bits InvTx1RFOn/InvTx1RFOff and

					InvTx2RFOn/InvTx2RFOff
	SigOutSel	3:0	R/W		select input signal to pin MFOUT
17h	RxSelReg			84h	selects internal receiver settings
	UARTSel[1:0]	7:6	R/W		selects the input of the contactless UART 00：constant LOW 01: Manchester with subcarrier from pin MFIN 10: modulated signal from the internal analog module, default 11: reserved
	RxWait[5:0]	5:0	R/W		after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this ‘frame guard time’ any signal on pin RX is ignored this parameter is ignored by the Receive command all other commands, such as Transceive use this paramet the counter starts immediately after the external RF field is switched on
18h	RxThresholdReg				selects thresholds for the bit decoder
	MinLevel[3:0]	7:4	R/W		defines the minimum signal strength at the decoder input that will be accepted. If the signal strength is below this level it is not evaluated
	reserved	7:4	-		reserved for future use
	CollLevel[2:0]	3:0	R/W		defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit
19h	DemodReg				defines demodulator settings
	AddIQ[1:0]	7:6	R/W		defines the use of I-channel and Q-channel during reception NOTE: the FixIQ bit must be set to logic 0 to enable

					the following settings: 00：selects the stronger channel 01：selects the stronger channel and freezes the selected channel during communication 10：reserved 11：reserved
	FixIQ	5	R/W		1：if the bits of AddIQ are set to X0, the reception is fixed to I-channel if the bits of AddIQ are set to X1, the reception is fixed to Q-channel
	TPrescalEven	4	R/W		set the frequency mode
	TauRcv[1:0]	3:2	R/W		changes the time-constant of the internal PLL during data reception
	TauSync[1:0]	1:0	R/W		changes the time constant of the internal PLL during burst
1Ah	reserved			00h	reserved for future use
1Bh	reserved			00h	reserved for future use
1Ch	MifNFCReg			62h	controls communication transmit parameters
	reserved	7:2	-		reserved
	TxWait	1:0	R/W		defines the additional response time.
1Dh	ManualRCVReg			00h	controls communication receive parameters
	reserved	7:5	-		reserved for future use
	ParityDisable	4	R/W		1: generation of the parity bit for transmission and the parity check for receiving is switched off. The received parity bit is handled like a data bit
	reserved	3:0	-		reserved for future use
1Eh	reserved			00h	reserved for future use
1Fh	SerialSpeedReg			EBh	select speed of serial UART interface
	BR_T0[2:0]	7:5	R/W		adjust transfer speed, see chapter for more details
	BR_T1[4:0]	4:0	R/W		adjust transfer speed, see chapter for more details

20h	reserved			00h	reserved for future use
21h	CRCResultReg (higher bits)			FFh	shows the MSB and LSB values of the CRC calculation
	CRCResultMSB [7:0]	7:0	R		shows the value of the CRCResultReg register's most significant byte. Only valid if Status1Reg register's CRCReady bit is set to logic 1
22h	CRCResultReg (lower bits)			FFh	shows the MSB and LSB values of the CRC calculation
	CRCResultLSB [7:0]	7:0	R		shows the value of the least significant byte of the CRCResultReg register. Only valid if Status1Reg register's CRCReady bit is set to logic 1
23h	GsNOffReg			88h	Selects the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched off.
	CWGsNOff	7:4	R/W		The value of this register defines the conductance of the output N-driver during times of no modulation. Note: The conductance value is binary weighted. During soft Power-down mode the highest bit is forced to 1. The value of the register is only used if the driver is switched off. Otherwise the bit value CWGsNOn of register GsNOnReg is used.
	ModGsNOff	3:0	R/W		The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. Note: The conductance value is binary weighted. During soft Power-down mode the highest bit is forced to 1. The value of the register is only used if the driver is switched off. Otherwise the bit value ModGsNOn of register GsNOnReg is used
24h	ModWidthReg			26h	controls the ModWidth setting

	ModWidth[7:0]	7:0	R/W		defines the width of the Miller modulation as multiples of the carrier frequency (ModWidth + 1 / fclk). The maximum value is half the bit period
25h	reserved			87h	reserved for future use
26h	RFCfgReg			48h	configures the receiver gain
	reserved	7	-		reserved for future use
	RxGain[2:0]	6:4	R/W		defines the receiver's signal voltage gain factor: 000：18dB 001：23dB 010：18dB 011：23dB 100：33dB 101：38dB 110：43dB 111：48dB
	reserved	3:0	-		reserved for future use
27h	GsNOnReg			88h	selects the conductance of the antenna driver pins TX1 and TX2 for modulation
	CWGsNOn	7:4	R/W		The value of this register defines the conductance of the output N-driver during times of no modulation. This may be used to regulate the output power and subsequently current consumption and operating distance. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1. NOTE: This value is only used if the driver TX1 or TX2 are switched on. Otherwise the value of the bits CWGsNOff of register GsNOffReg is Used.

	ModGsNOn	3:0	R/W		The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1. NOTE: This value is only used if the driver TX1 or Tx2 are switched on. Otherwise the value of the bits ModsNOff of register GsNOffReg is used.
28h	CWGsPReg			20h	defines the conductance of the p-driver output when not active
	reserved	7:6	-		Reserved for future use
	CWGsP	5:0	R/W		The value of this register defines the conductance of the output P-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1.
29h	ModGsPReg			20h	defines the conductance of the p-driver output during modulation
	reserved	7:6	-		Reserved for future use
	ModGsP	5:0	R/W		The value of this register defines the conductance of the output P-driver for the time of modulation. This may be used to regulate the modulation index. NOTE: The conductance value is binary weighted. NOTE: During soft Power-down mode the highest bit is forced to 1.
2Ah	TModeReg			00h	defines settings for the internal timer

	TAuto	7	R/W		1：the timer starts automatically at the end of the transmission in all communication modes at all speeds or when InvTxnRFOn bits are set to logic 1 and the RF field is switched on 0：indicates that the timer is not influenced by the protocol
	TGated[1:0]	6:5	R/W		The internal timer is running in gated mode. Note: In the gated mode, the bit TRunning is 1 when the timer is enabled by the register bits. This bit does not influence the gating signal. 00：Non gated mode 01：Gated by pin MFIN 10：Gated by AUX1 11：-
	TAutoRestart	4	R/W		1：timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero 0：timer decrements to 0 and the ComIrqReg register's TimerIRq bit is set to logic 1
	TPrescaler_Hi [3:0]	3:0	R/W		defines the higher 4 bits of the TPrescaler value
2Bh	TPrescalerReg			00h	defines the lower 8 bits of the TPrescaler value
	TPrescaler_Lo [7:0]	7	R/W		defines the lower 8 bits of the TPrescaler value
2Ch	TReloadReg (higher bits)			00h	defines the 16-bit timer reload value
2Dh	TReloadReg (lower bits)			00h	defines the 16-bit timer reload value
2Eh	TCounterValReg (higher bits)			xxh	timer value higher 8 bits

2Fh	TCounterValReg (lower bits)			xxh	timer value lower 8 bits

NOTE：R/W：Read/Write；D：Dynamic；R：Only Read；W：Only Write；

Typical application schematic

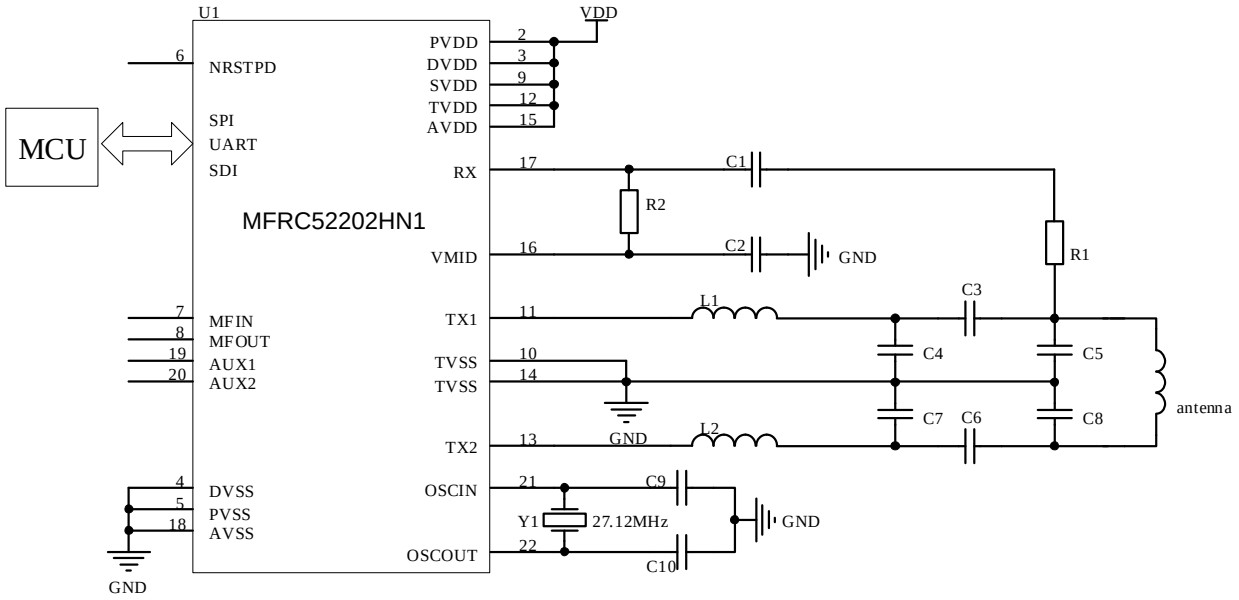

Figure 10-1 Typical application diagram 1

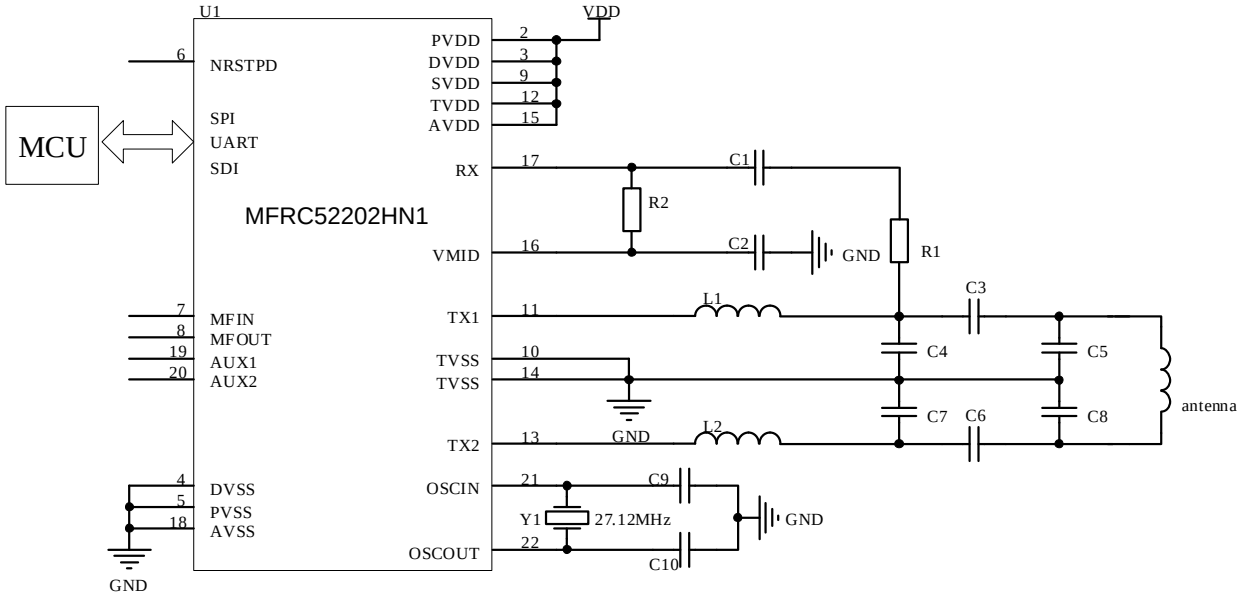

Figure 10-2 Typical application diagram 2

NOTE: When working with button batteries, it is recommended to add a 100μF large capacitor to the power supply;

Package outline

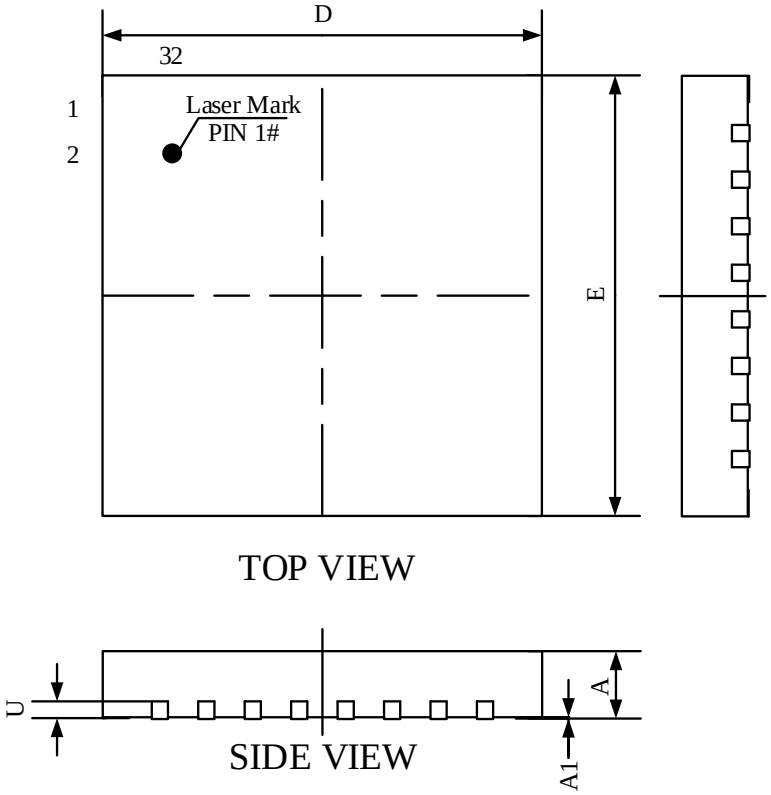

Figure 11-1 Package（QFN32L）

Table11-1 Package outline

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.2	0.05
b	0.20	0.25	0.30
b1	0.20	0.25	0.30
c	0.203REF		
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Nd	3.5BSC		
Ne	3.5BSC		
E	4.90	5.0	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
L1	0.15REF		
K	0.35REF		
K1	0.225REF		

Order information

Table13-1 MFRC52202HN1 order example

order code	package	container	minimum
52202 -Sample	5×5mm 32-pin QFN	Box/Tube	5
MFRC52202HN1	5×5mm 32-pin QFN	Tape and reel	4K