Quad 16-/12-Bit, Low-Power, High-Performance DACs

Features

- Quad, 16-/12-Bit Pin Compatible DACs
- — TPC116S4: 16 Bits
  — TPC112S4: 12 Bits
- Low Power Consumption (800 μA typ)
- Differential Nonlinearity: ±1 LSB (Max)
- Glitch Energy: 2 nV-s
- Power-on Reset to Zero
- Supply Range: 2.7 V to 5.5 V
- Buffered Rail-to-Rail Output Operation
- Safe Power-on Reset (POR) to Zero DAC Output
- Fast 30-MHz, 3-Wire SPI/QSPI/MICROWIRE-Compatible Serial Interface
- Schmitt-Trigger Inputs for Direct Optocoupler Interface
- SYNC Interrupt Facility
- High-Performance Drop-in Compatible with TLV5614
- Available in TSSOP16 Package

Applications

- Gain and Offset Adjustment
- Process Control and Servo Loops
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Automatic Test Equipment

Description

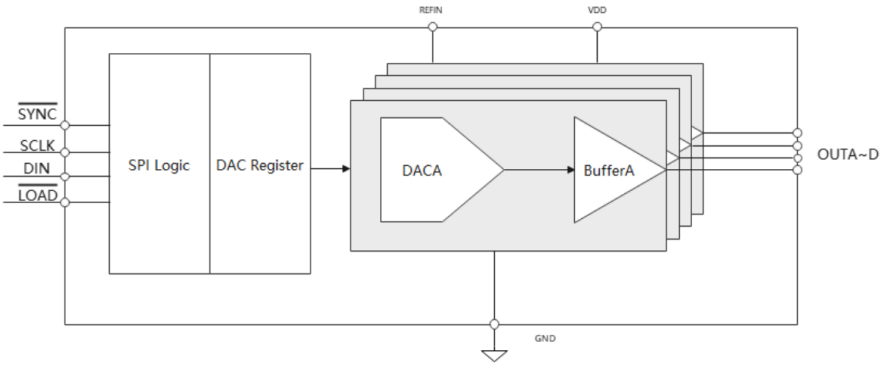
The TPC116S4/TPC112S4 are pin-compatible 16-bit and 12-bit digital-to-analog converters. The products are four-channel, low-power, and buffered voltage-out DACs, which are guaranteed monotonic by design. The devices use a precision external reference applied through the high-resistance input for rail-to-rail operation and low system power consumption.

The TPC116S4/TPC112S4 accept a wide range of 2.7-V to 5.5-V supply voltage. The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V and remains there until a valid write takes place.

The on-chip precision output amplifiers of the TPC116S4/TPC112S4 allow rail-to-rail output swing to be achieved. For remote sensing applications, the inverting input of the output amplifier is available to users. The TPC116S4/TPC112S4 use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The TPC116S4/TPC112S4 are available in the small-sized TSSOP16 package. All packages are specified over the −40°C to +125°C extended industrial temperature range.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2022-12-05	Rev.A.4	Updated the Functional Block Diagram.
2024-12-03	Rev.A.5	Updated to a new datasheet format.

Pin Configuration and Functions

TPC11xS4
TSSOP16
Top View

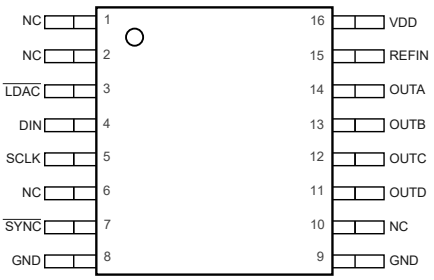


Table 1. Pin Functions

Pin No.	Name	I/O	Description
1	NC	NC	Not connect.
2	NC	NC	Not connect.
3	$\overline{\text{LOAD}}$	DI	• Load DAC. • When the LOAD signal is high, no DAC output updates occur when the input digital data is read into the serial interface. • The DAC outputs are only updated when the LDAC is low.
4	DIN	DI	• Serial data input. • Data is clocked into the 16-/24-bit input shift register on each falling edge of the serial clock input. • Schmitt-Trigger logic input.
5	SCLK	DI	• Serial clock input. • Data can be transferred at rates up to 30 MHz. • Schmitt-Trigger logic input.
6	NC	NC	Not connect.
7	$\overline{\text{SYNC}}$	DI	• Level-triggered control input (active LOW). • This is the frame synchronization signal for the input data. • When $\overline{\text{SYNC}}$ goes low, it enables the input shift register, and the data is transferred in on the falling edges of the following clocks.
8	GND	P	Ground reference point for all circuitry on the part.
9	GND	P	Ground reference point for all circuitry on the part.
10	NC	NC	Not connect.
11	OUTD	AO	DACD output.
12	OUTC	AO	DACC output.
13	OUTB	AO	DACB output.
14	OUTA	AO	DACA output.

Pin No.	Name	I/O	Description
15	REFIN	AI	Reference voltage input.
16	VDD	P	Power supply input.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Supply Voltage, VDD – GND (2)		7	V
	Input Voltage	GND – 0.3	VDD + 0.3	V
	Input Current: +IN, −IN (3)	−20	20	mA
	Output Short-Circuit Duration (4)		Indefinite	
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The supplies must be established simultaneously, with, or before, the application of any input signals.
(3) The inputs are protected by ESD protection diodes to the negative power supply. If the input extends more than 500 mV beyond the negative power supply, the input current should be limited to less than 10 mA.
(4) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. The thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP16	180	35	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 5 V, V_{REF} = 5 V, C_L = 100 pF, R_L = 10 kΩ, T_A = −40℃ to +105°C, unless otherwise noted. Typical values are at T_A = +25℃.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Accuracy (1)						
N	Resolution	TPC112S4	12			Bits
		TPC116S4	16			
INL	Integral Nonlinearity	TPC112S4 (12-bit) (2)	−2	±0.25	2	LSB
		TPC116S4 (16-bit) (2)	−16	±8	16	
DNL	Differential Nonlinearity	TPC112S4 (12-bit) (2)	−1	±0.05	1	LSB
		TPC116S4 (16-bit) (2)	−1	±0.5	1	
OE	Zero Offset Error			6.5	30	mV
	Full-Scale Offset Error		−30	0	30	mV
	Offset-Error Drift			±1		μV/°C
GE	Gain Error		−0.3	±0.13	0.3	%FS
	Gain Temperature Coefficient			±2		ppmFS/°C
Reference Input						
V_{REF}	Reference-Input Voltage Range		0.5		V_{DD}	V
R_{REF}	Reference-Input Impedance			333		kΩ
DAC Output						
	Output Voltage Range		0		V_{REF}	V
	DC Output Impedance			0.1		Ω
C_L	Capacitive Load (3)	Series resistance = 0 Ω			0.1	nF
		Series resistance = 1 kΩ			15	μF
R_L	Resistive Load (3)		5			kΩ
	Short-Circuit Current	V_{DD} = 5.5 V		35		mA
	Power-up Time	From power-down mode		25		μs
Digital Inputs (SCLK, DIN, $\overline{SYNC}$)						
V_{IH}	Input High Voltage	V_{DD} = 5 V	2			V
		V_{DD} = 3.3 V	1.5			V
V_{IL}	Input Low Voltage	V_{DD} = 5 V			0.6	V
		V_{DD} = 3.3 V			0.4	V
I_{IN}	Input Leakage Current	V_{IN} = 0 V or V_{DD}		±5	±10	μA
C_{IN}	Input Capacitance			1		pF
V_{HYS}	Hysteresis Voltage			0.15		V
Dynamic Performance (3)						
SR	Voltage-Output Slew Rate	Positive and negative		1		V/μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BW	Voltage-Output Settling Time	1/4 scale to 3/4 scale, to ≤ 0.5 LSB, 12 bits		14		μs
	Reference −3-dB Bandwidth	Hex code = 800 (TPC112S4), Hex code = 8000 (TPC116S4)		100		kHz
	Digital Feedthrough	Code = 0, all digital inputs from 0 V to V_{DD}, SCLK < 50 MHz		0.5		nV·s
	DAC Glitch Impulse	Major code transition		2		nV·s
	Output Noise	10 kHz		90		nV/√Hz
	Integrated Output Noise	0.1 Hz to 10 Hz		25		μV_{P-P}
Power Requirements						
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Supply Current	V_{DD} = 5 V, no load; all digital inputs at 0 V or V_{DD}, supply current only; excludes reference input current, midscale		0.8	1.5	mA
I_{DD}	Supply Current	V_{DD} = 3.3 V, no load; all digital inputs at 0 V or V_{DD}, supply current only; excludes reference input current, midscale		0.5	1	mA
	Power-down Supply Current	No load, all digital inputs at 0 V or V_{DD}			500	μA

(1) Linearity is tested within 20 mV of GND and V_{DD}.
(2) Gain and offset are tested within 100 mV of GND and V_{DD}.
(3) All timing specifications are measured with $V_{IL} = V_{GND}$, $V_{IH} = V_{DD}$.

Timing Characteristics

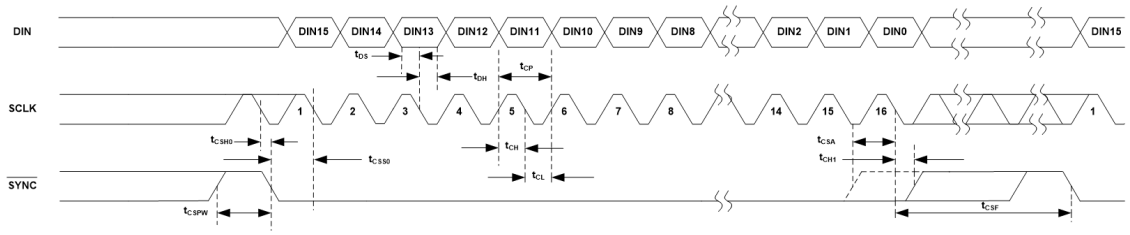


Figure 1. 16-Bit Serial-Interface Timing Diagram (TPC112S4)

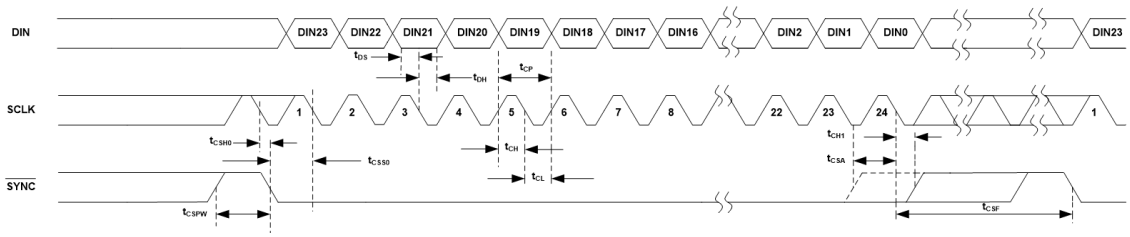


Figure 2. 24-Bit Serial-Interface Timing Diagram (TPC116S4)

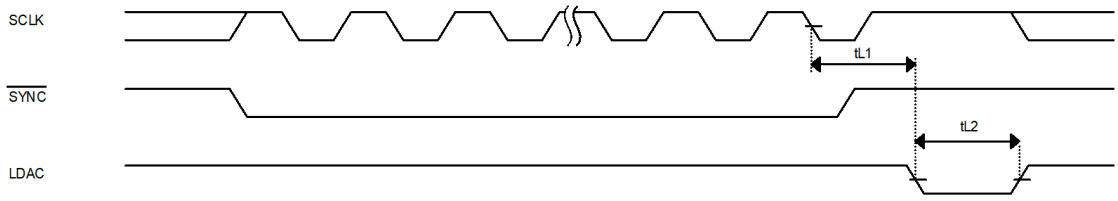


Figure 3. LDAC Timing Diagram

Table 2. Timing Characteristics (Figures 1, 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCLK}	Serial Clock Frequency		0		30	MHz
t_{CH}	SCLK Pulse-Width High		8			ns
t_{CL}	SCLK Pulse-Width Low		8			ns
t_{CSS0}	$\overline{SYNC}$ Fall to SCLK Fall Setup Time		8			ns
t_{CSH0}	$\overline{SYNC}$ Fall to SCLK Fall Hold Time		0			ns
t_{CSH1}	$\overline{SYNC}$ Rise to SCLK Fall Hold Time		0			ns
t_{CSA}	$\overline{SYNC}$ Rise to SCLK Fall				12	ns
t_{CSF}	SCLK Fall to $\overline{SYNC}$ Fall		100			ns
t_{DS}	DIN to SCLK Fall Setup Time		5			ns
t_{DH}	DIN to SCLK Fall Hold Time		4.5			ns
t_{CSPW}	$\overline{SYNC}$ Pulse-Width High		20			ns
t_{CLPW}	$\overline{SYNC}$ Pulse-Width Low		20			ns
t_{CSC}	$\overline{SYNC}$ Rise to $\overline{SYNC}$ Fall		20			ns
t_{L1}	SCLK Falling Edge to $\overline{LDAC}$ Falling Edge for Asynchronous LDAC Update		50			ns
t_{L2}	$\overline{LDAC}$ Pulse Width LOW Time		50			ns

Typical Performance Characteristics

All test conditions: V_S = 5 V, T_A = +25℃, unless otherwise noted.

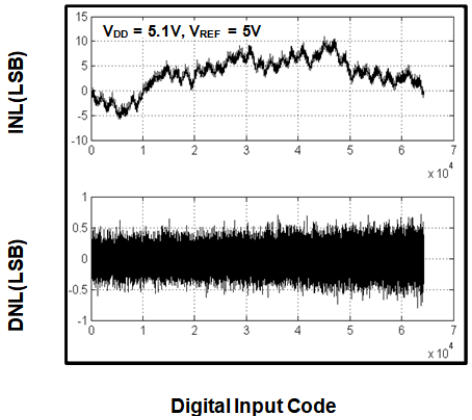


Figure 4. INL and DNL vs. Digital Input Code (+25℃ TPC116S4)

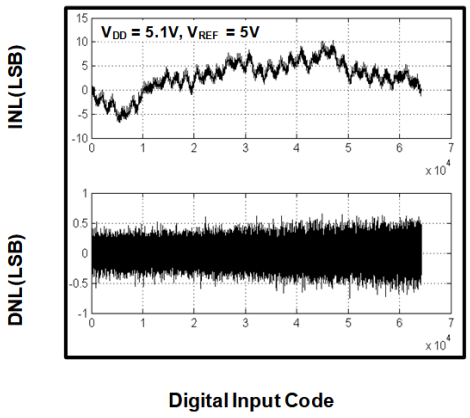


Figure 5. INL and DNL vs. Digital Input Code (−40°C TPC116S4)

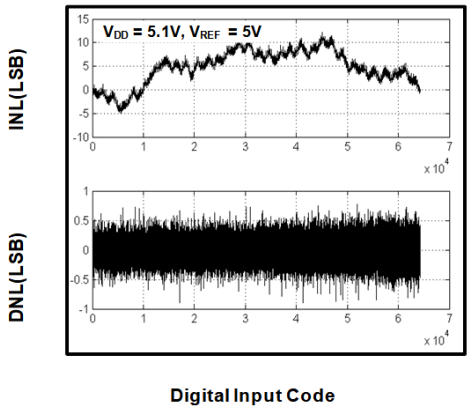


Figure 6. INL and DNL vs. Digital Input Code (+105°C TPC116S4)

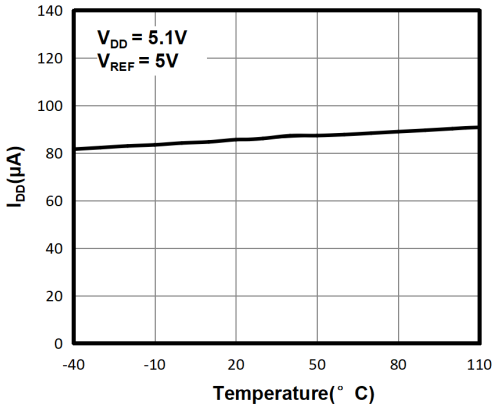


Figure 7. Power-Supply Current vs. Temperature (TPC116S4)

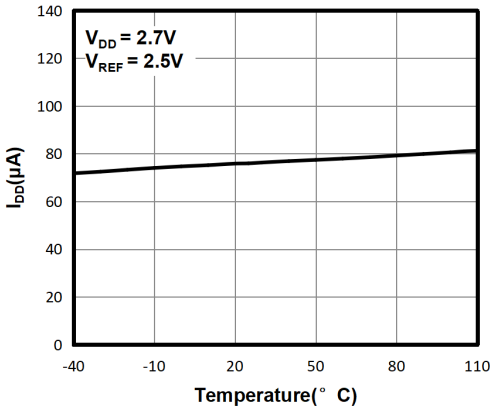


Figure 8. Power-Supply Current vs. Temperature (TPC116S4)

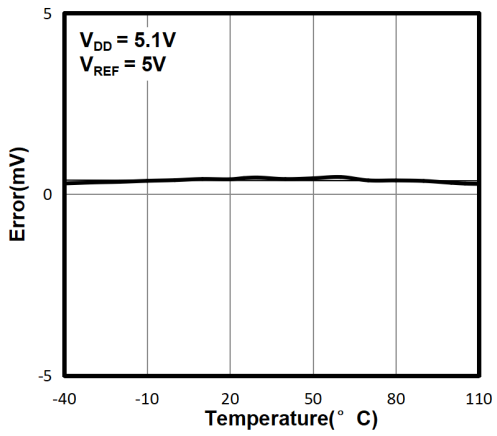


Figure 9. Zero-Scale Error vs. Temperature (TPC116S4)

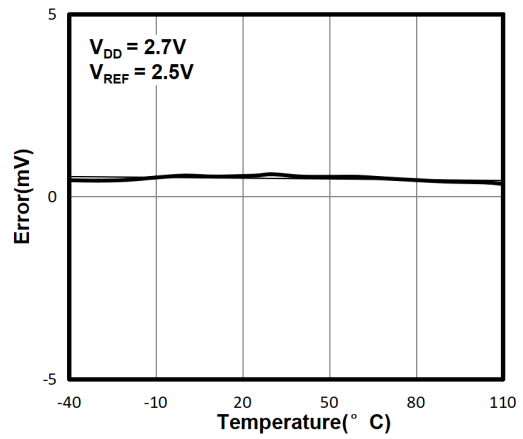


Figure 10. Zero-Scale Error vs. Temperature (TPC116S4)

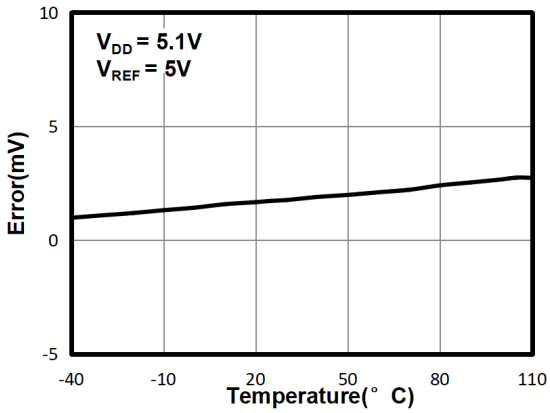


Figure 11. Full-Scale Error vs. Temperature (TPC116S4)

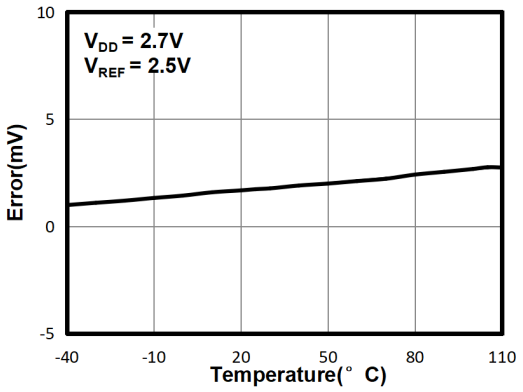


Figure 12. Full-Scale Error vs. Temperature (TPC116S4)

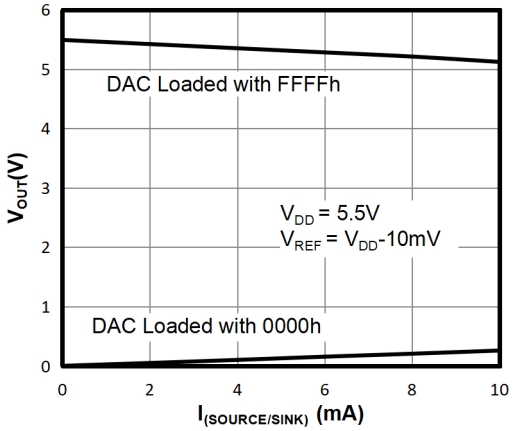


Figure 13. Source and Sink Current Capability (TPC116S4)

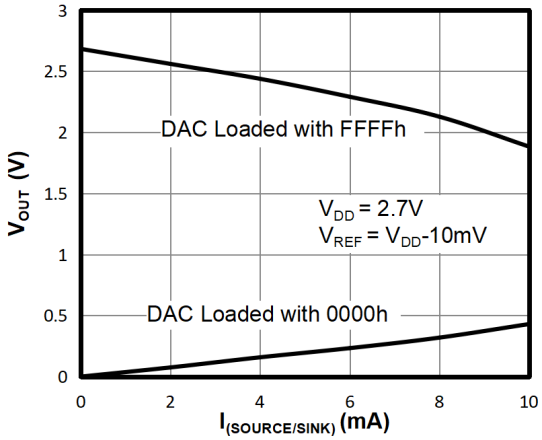


Figure 14. Source and Sink Current Capability (TPC116S4)

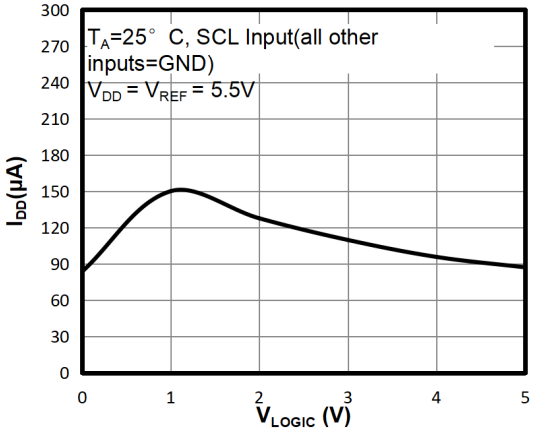


Figure 15. Supply Current vs. Logic Input Voltage (TPC116S4)

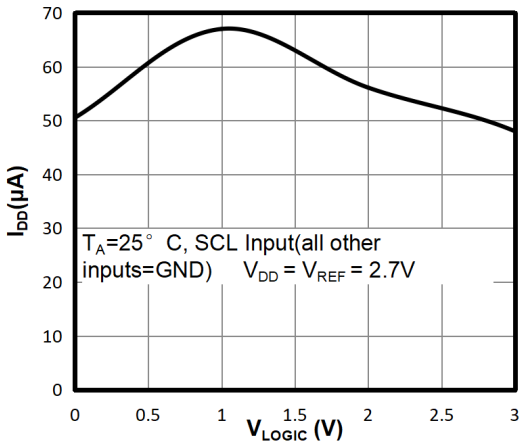


Figure 16. Supply Current vs. Logic Input Voltage (TPC116S4)

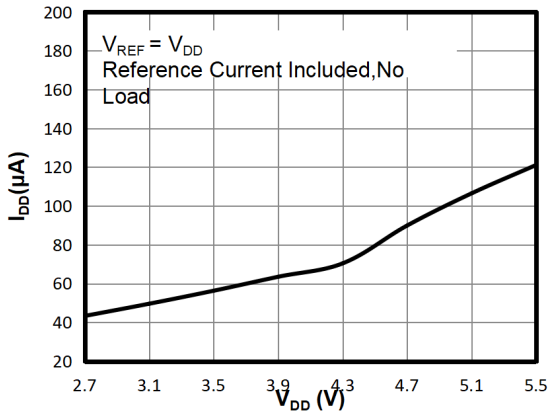
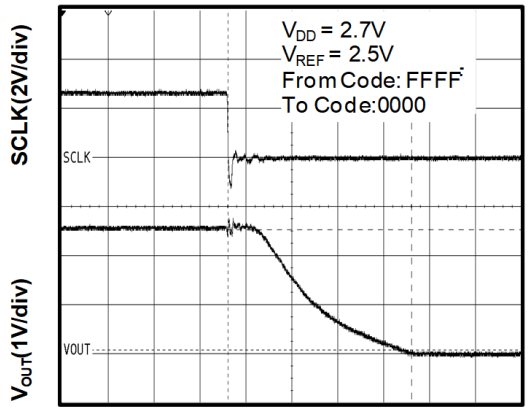
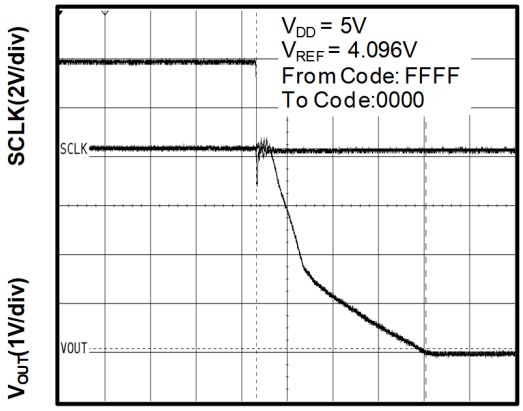


Figure 17. Supply Current vs. Supply Voltage (TPC116S4)



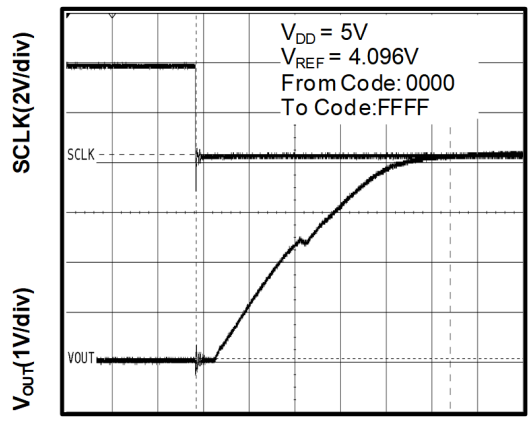
Time (160ns/div)

Figure 18. Full-Scale Settling Time (2.7-V Falling Edge)



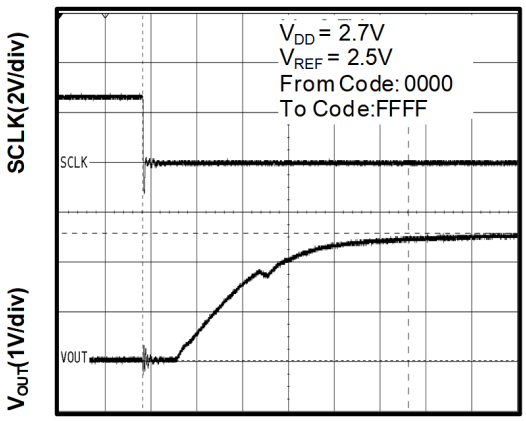
Time (250ns/div)

Figure 19. Full-Scale Settling Time (5-V Falling Edge)



Time (500ns/div)

Figure 20. Full-Scale Settling Time (5-V Rising Edge)



Time (430ns/div)

Figure 21. Full-Scale Settling Time (2.7-V Rising Edge)

Detailed Description

Overview

The TPC116S4 and TPC112S4 are pin-compatible and software-compatible 12-bit and 16-bit DACs. The TPC116S4 and TPC112S4 are 4-channel, low-power, high-reference input resistance, and buffered voltage-output DACs. The TPC116S4 and TPC112S4 minimize the digital noise feedthrough from their inputs to outputs by powering down the SCLK and DIN input buffers after the completion of each data frame. The data frames are 16 bits for the TPC112S4 and 24 bits for the TPC116S4. During power up, the TPC116S4 and TPC112S4 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers which need to be off during power up. The TPC116S4 and TPC112S4 contain a segmented resistor string-type DAC, a serial-in/parallel-out shift register, a DAC register, a power-on-reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first.

Functional Block Diagram

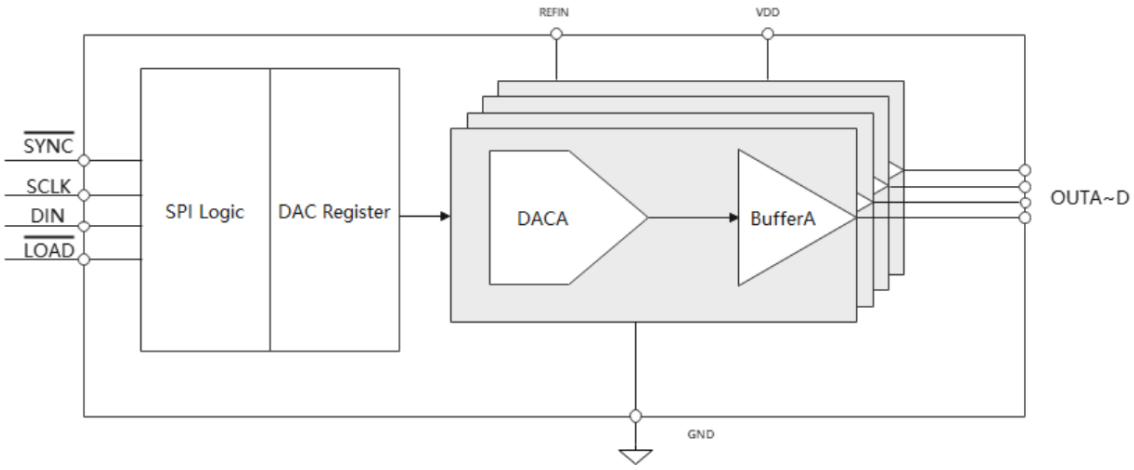


Figure 22. Functional Block Diagram

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

DAC Reference (REF)

The external reference input features a typical input impedance of 333 kΩ and accepts an input voltage from +2 V to VDD. Connect an external voltage supply between REF and GND to apply an external reference.

Serial Interface

The 3-wire serial interface of the TPC116S4/TPC112S4 is compatible with MICROWIRE, SPI, QSPI, and DSP. The interface provides three inputs: SCLK, $\overline{SYNC}$, and DIN. The chip-select input ($\overline{SYNC}$) frames the serial data loading at DIN. Following a chip-select input high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 16 bits for the TPC112S4 and 24 bits for the TPC116S4. The first 3 bits are the control bits followed by 1 power-down bit as well as 12 data bits (MSB first) for the TPC112S4 and 22 data bits (MSB first) for the TPC116S4 as shown in Table 3 and Table 4. The serial input register transfers its contents to the input registers after loading 16/24 bits of data and updates the DAC output immediately after the data is received on the 16-/24-bit falling edge of the clock. To initiate a new data transfer, $\overline{SYNC}$ is driven high and kept for a minimum of 20 ns before the next write sequence. The SCLK can be either high or low between $\overline{SYNC}$ write pulses. Figure 1 and Figure 2 show the timing diagrams for the complete 3-wire serial interface transmission. The DAC code of the TPC116S4 is unipolar binary with V_{OUT} = (code / 65,536) × V_{REF}, while that of the TPC112S4 is unipolar binary with V_{OUT} = (code / 4096) × V_{REF}.

Table 3. Operating Mode Truth Table (TPC112S4)

16-Bit Word					Function
A2	A1	A0	PD	DAC Data Bit	
D15	D14	D13	D12	D11 ~ D0	
1	0	0	0	X	Update DAC A Data
1	0	1	0	X	Update DAC B Data
1	1	0	0	X	Update DAC C Data
1	1	1	0	X	Update DAC D Data 100 k to GND
X	X	X	1	X	Power down

Table 4. Operating Mode Truth Table (TPC116S4)

24-Bit Word									Function
				A2	A1	A0	PD	DAC Data Bit	
D23	D22	D21	D20	D19	D18	D17	D16	D15 ~ D0	
X	X	X	X	1	0	0	0	X	Update DAC A Data

X	X	X	X	1	0	1	0	X	Update DAC B Data
X	X	X	X	1	1	0	0	X	Update DAC C Data
X	X	X	X	1	1	1	0	X	Update DAC D Data
X	X	X	X	X	X	X	1	X	Power down

Typical Application

Figure 23 shows the typical application schematic.

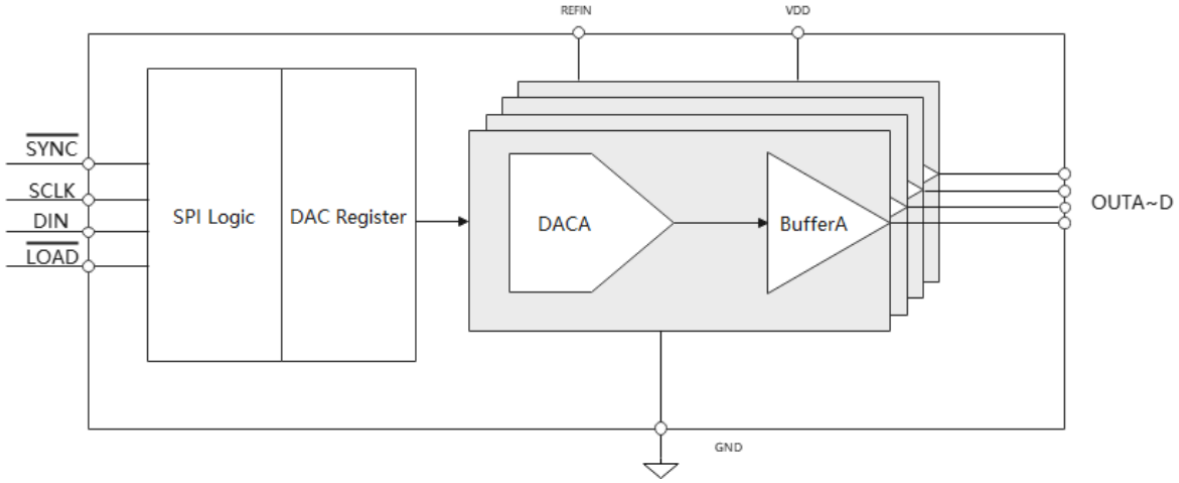
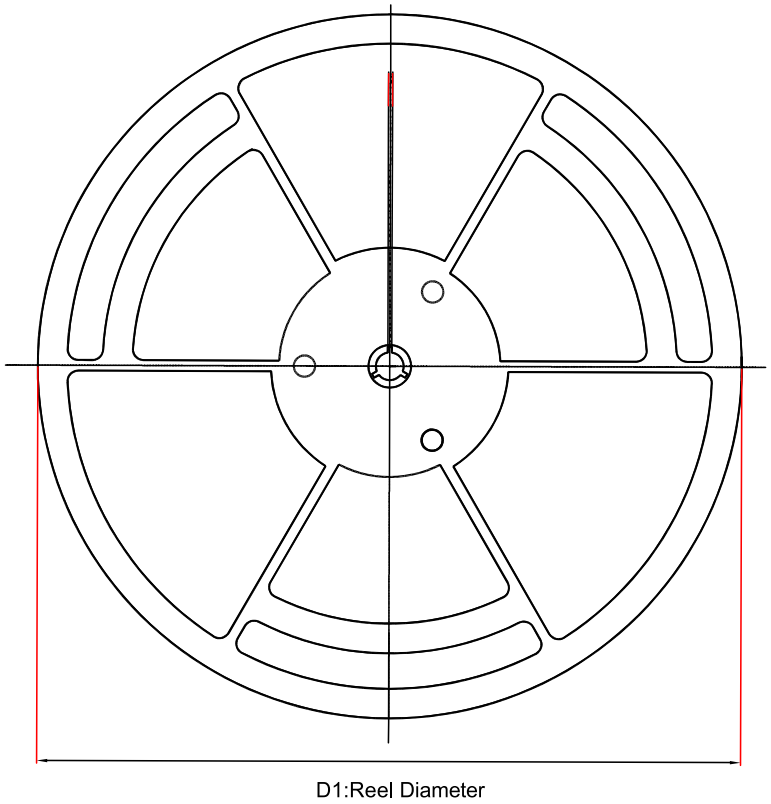
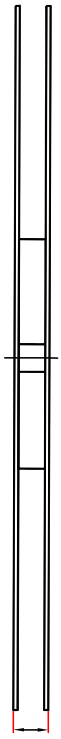
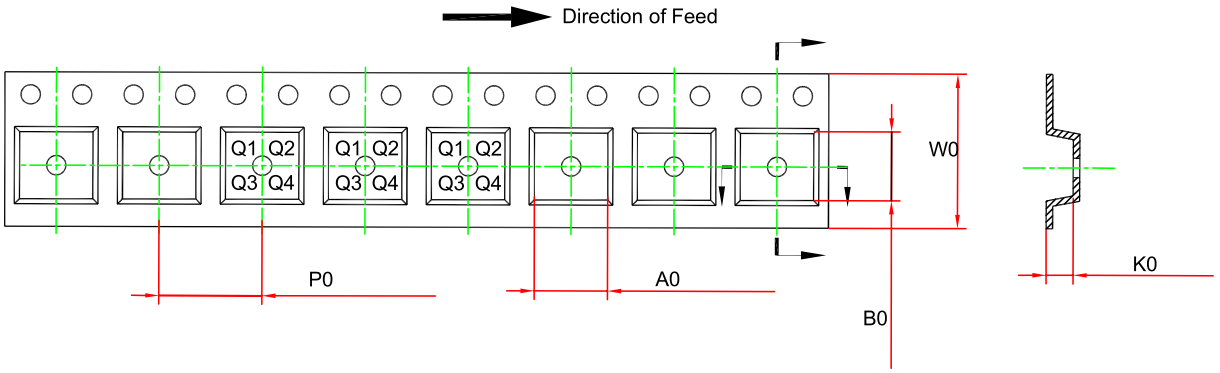


Figure 23. Typical Application Circuit

Tape and Reel Information





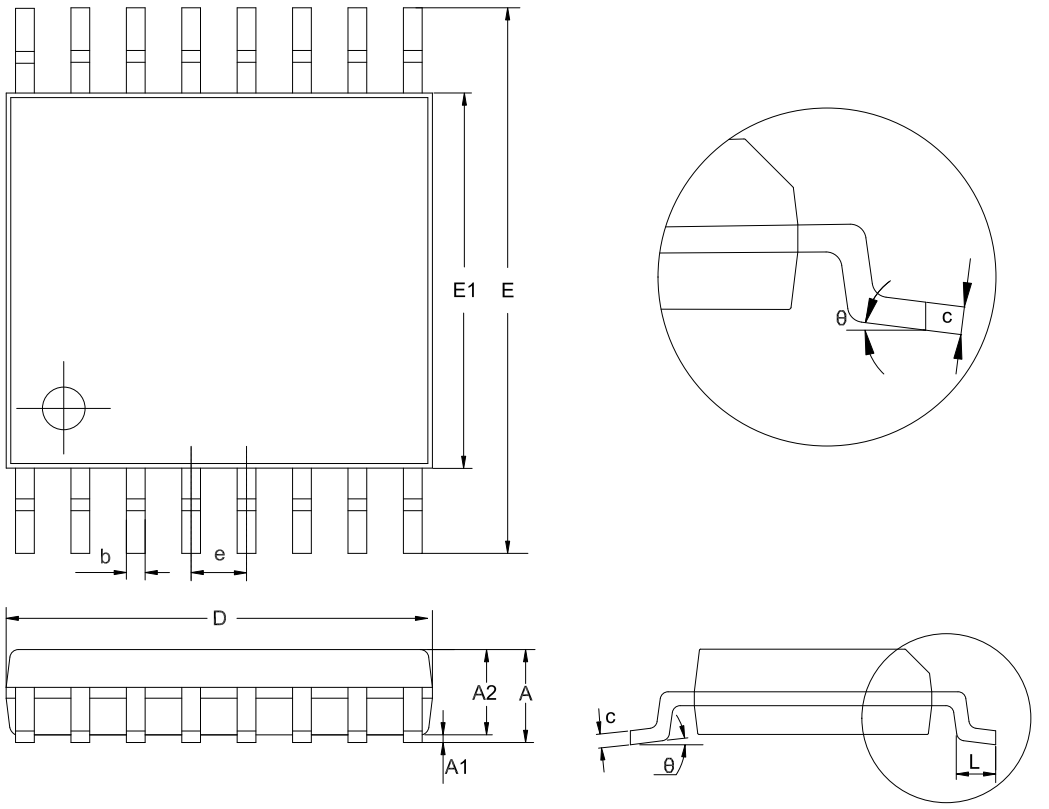


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC112S4-TR	TSSOP16	330	17.6	6.8	5.4	1.3	8	12	Q1
TPC116S4-TR	TSSOP16	330	17.6	6.8	5.4	1.3	8	12	Q1

Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC112S4-TR	−40 to 125°C	TSSOP16	112S4	1	Tape and Reel, 3000	Green
TPC116S4-TR	−40 to 125°C	TSSOP16	116S4	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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