

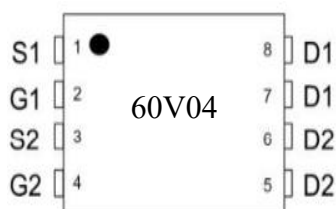
**Features**

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

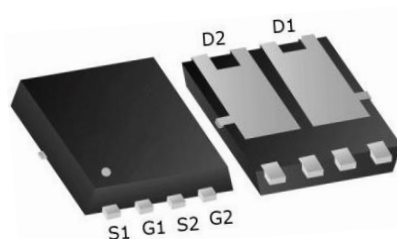
 B_{vds} **40V** **R_{dson}** **6.8m Ω** **I_D** **60A****Application**

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

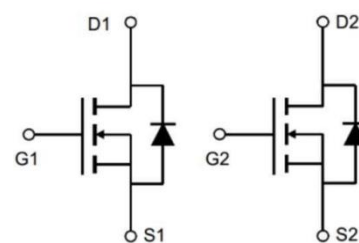
RoHS

Package

Marking and pin assignment



PDFN5x6-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
60V04	S60V04F	PDFN5x6-8L	5000

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C=25^{\circ}\text{C}$	I_D	60	A
	$T_C=100^{\circ}\text{C}$		30	A
Pulsed Drain Current ²		I_{DM}	100	A
Single Pulsed Avalanche Energy ³		E_{AS}	28	mJ
Avalanche Current		I_{AS}	180	A
Total Power Dissipation		P_D	29	W
Operating Junction Temperature Range		T_J	$-55 \sim 150$	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	$-55 \sim 150$	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance,Junction-to-Case ¹	$R_{\theta JC}$	--	3.2	$^{\circ}\text{C/W}$
Thermal Resistance,Junction-to-Ambient ¹	$R_{\theta JA}$	--	60	$^{\circ}\text{C/W}$

Ordering Information

Ordering Number	Package	Pin Assignment						Packing
Halogen Free		G1	G2	D1	D2	S1	S2	
HLS60V04F	PDFN5x6-8L	2	4	7,8	5,6	1	3	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32\text{V}, V_{GS}=0\text{V}$	-	-	1	μA
Gate to Body Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	1.6	2.5	V
Static Drain-Source On-Resistance ³	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=12\text{A}$	-	6.8	8.5	m Ω
		$V_{GS}=4.5\text{V}, I_D=10\text{A}$	-	10	15	
Input Capacitance	C_{iss}	$V_{DS}=15\text{V}, V_{GS}=0\text{V},$ $f=1\text{MHz}$	-	690	-	pF
Output Capacitance	C_{oss}		-	193	-	
Reverse Transfer Capacitance	C_{rss}		-	38	-	
Total Gate Charge	Q_g	$V_{DS}=20\text{V}, V_{GS}=4.5\text{V},$ $I_D=12\text{A}$	-	5.8	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	1.2	-	
Turn-on Delay Time	$T_{d(on)}$	$V_{GS}=10\text{V}, V_{DD}=15\text{V},$ $R_G=3.3\Omega, I_D=1\text{A}$	-	14.3	-	nS
Turn-on Rise Time	t_r		-	5.6	-	
Turn-Off Delay Time	$T_{d(off)}$		-	20	-	
Turn-Off Fall Time	T_f		-	11	-	
Body Diode Reverse Recovery Charge	Q_{rr}		-	12	-	
Maximum Continuous Drain to Source Diode Forward Current ^{1,5}	I_S	$V_G=V_{DD}=0\text{V}, \text{Force Current}$	-	-	60	A
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0\text{V}, I_S=1\text{A}$	-	-	1	V

Notes:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=31\text{A}$.
- 4.The power dissipation is limited by 150°C junction temperature.
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Performance Characteristics

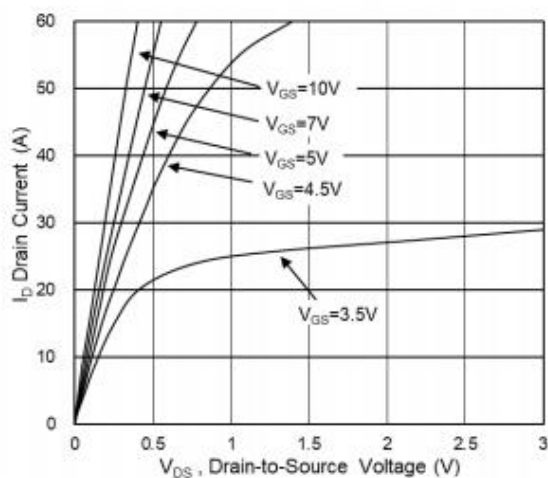


Fig.1 Typical Output Characteristics

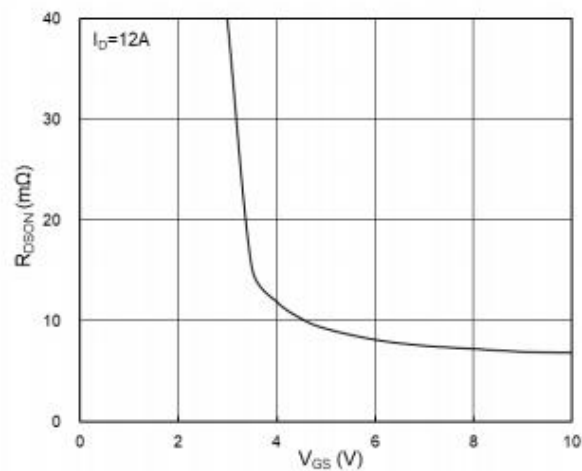


Fig.2 On-Resistance vs G-S Voltage

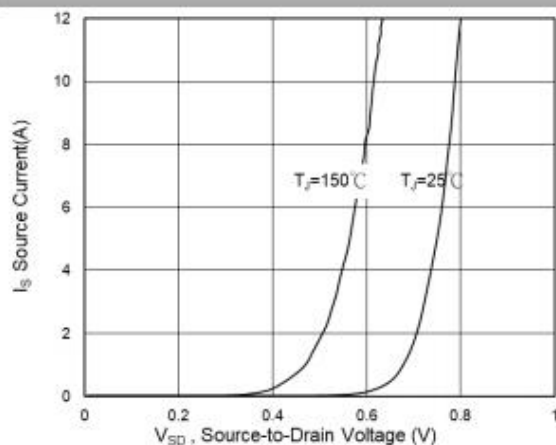


Fig.3 Source Drain Forward Characteristics

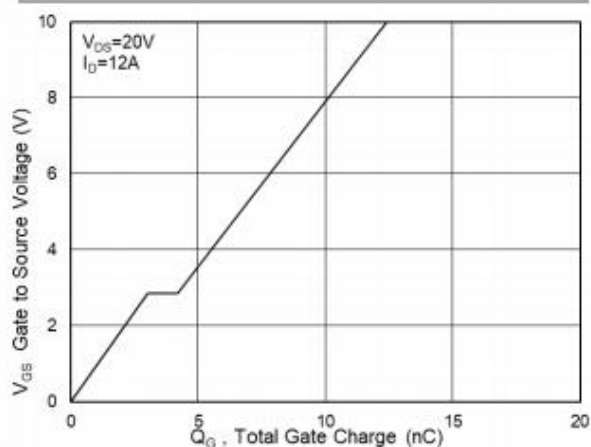


Fig.4 Gate-Charge Characteristics

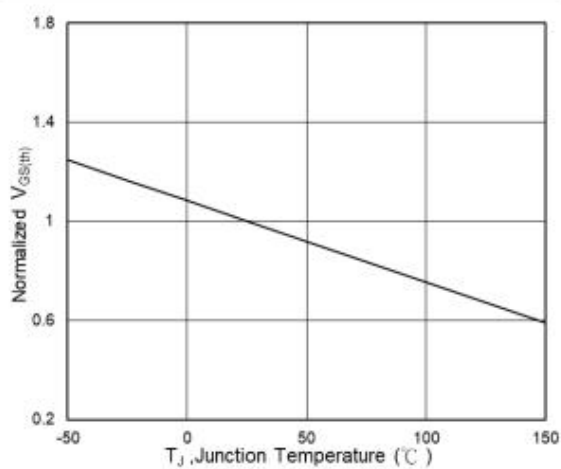


Fig.5 Normalized $V_{GS(th)}$ vs T_J

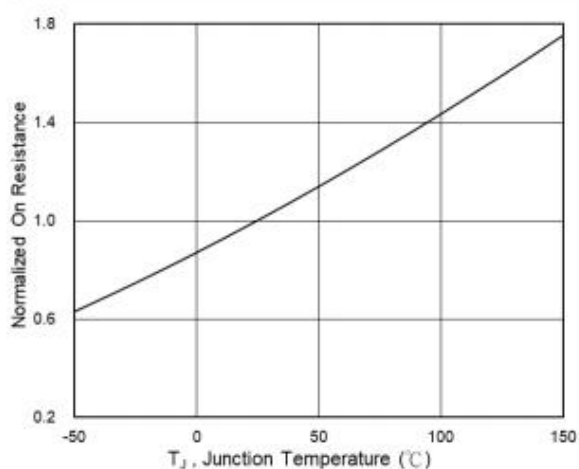


Fig.6 Normalized $R_{DS(on)}$ vs T_J

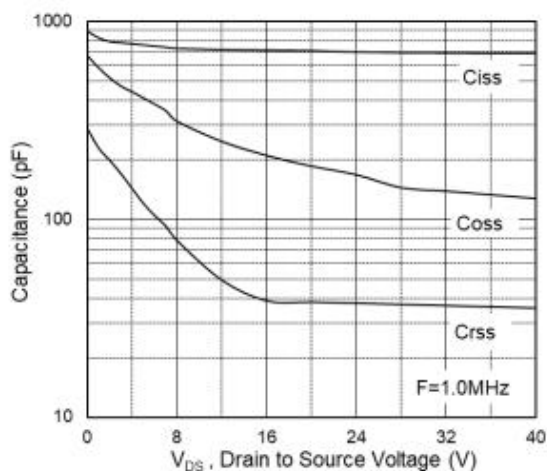


Fig.7 Capacitance

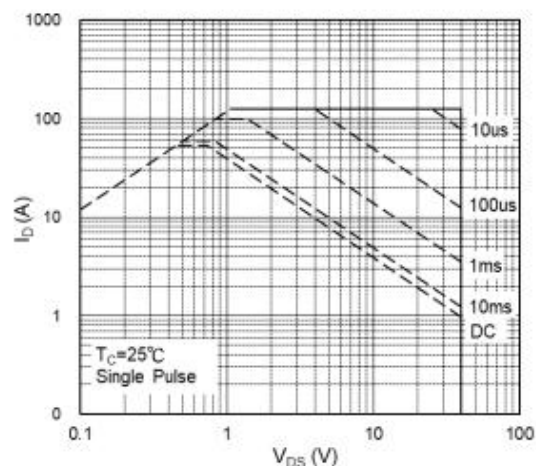


Fig.8 Safe Operating Area

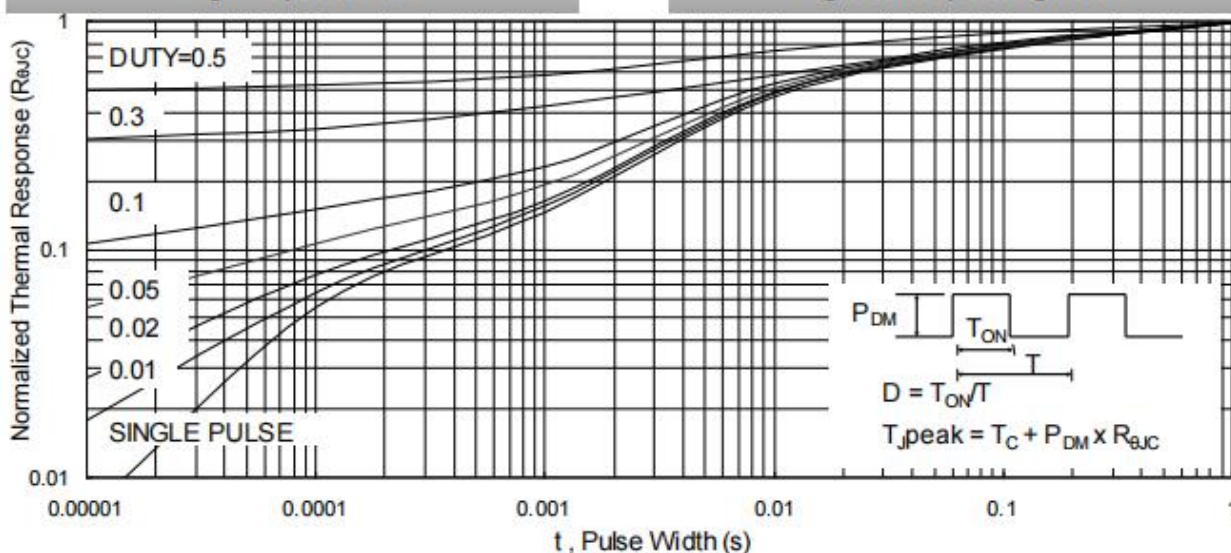


Fig.9 Normalized Maximum Transient Thermal Impedance

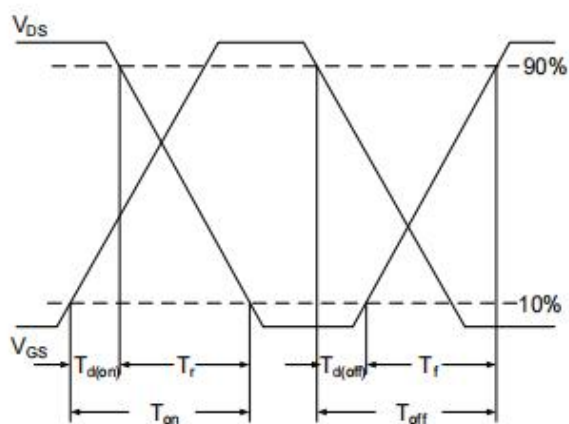


Fig.10 Switching Time Waveform

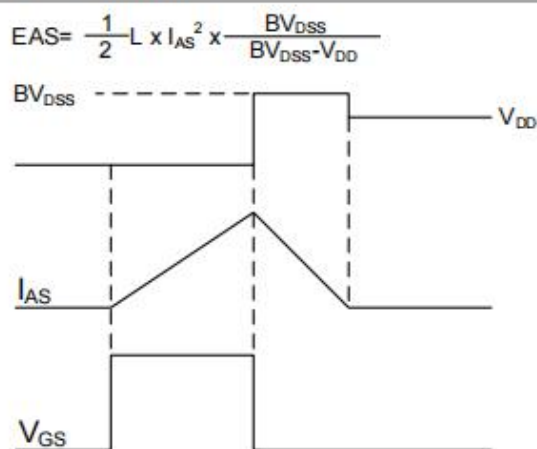
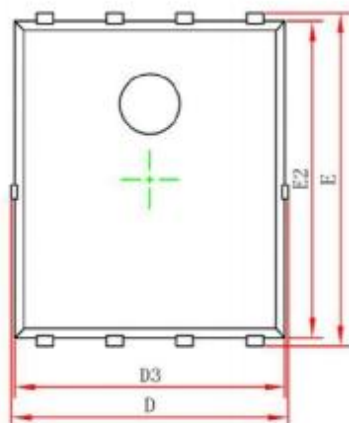
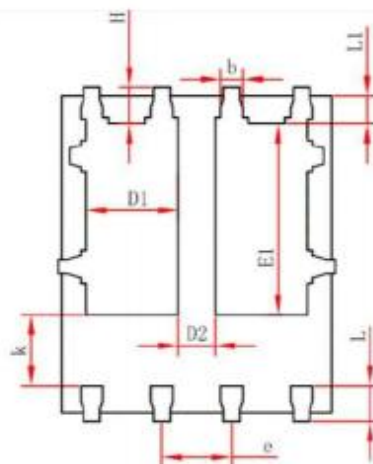
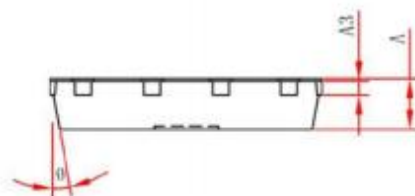


Fig.11 Unclamped Inductive Waveform



Package Dimensions PDFN5x6-8L

Top ViewBottom ViewSide View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°



Important Notice and Disclaimer

HL Microelectronics reserves the right to make changes to this document and its products and specifications at any time without notice.

Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

HL Microelectronics makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, not does HL Microelectronics assume any liability for application assistance or customer product design.

HL Microelectronics does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

No license is granted by implication or otherwise under any intellectual property rights of HL Microelectronics.

HL Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of HL Microelectronics.