

SCT4036DEHR-VB Datasheet

N-Channel 650V (D-S) SiC Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	650	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 18$ V	0.05
Q_g (nC)	90	

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



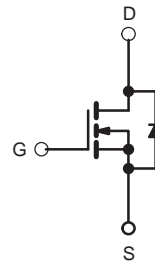
APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- DC/DC converter

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Top View



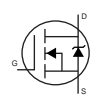
N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	650	V	
Gate-Source Voltage	V_{GS}	-10 / +22		
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 18 V	$T_C = 25$ °C	40	A
		$T_C = 100$ °C	32	
Pulsed Drain Current ^a	I_{DM}	120		
Linear Derating Factor		2.1	W/°C	
Single Pulse Avalanche Energy ^b	E_{AS}	225	mJ	
Maximum Power Dissipation	P_D	187	W	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C	
Drain-Source Voltage Slope	dV/dt	50	V/ns	
Reverse Diode dV/dt ^d				15
Soldering Recommendations (Peak Temperature) ^c	for 10 s	260	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 100$ V, starting $T_J = 25$ °C, $L = 0.5$ mH, $R_g = 25$ Ω , $I_{AS} = 30$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 10\text{ mA}$		2	-	5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = +22\text{ V}$		-	-	100	nA
		$V_{GS} = -10\text{ V}$		-	-	100	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$		-	10	-	μA
		$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}$	$I_D = 20\text{ A}$	-	0.05	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 0\text{ V}, I_D = 30\text{ A}$		-	12	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 600\text{ V},$ $f = 1\text{ MHz}$		-	2000	-	pF
Output Capacitance	C_{oss}			-	175	-	
Reverse Transfer Capacitance	C_{rss}			-	9	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		-	156	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	268	-	
Total Gate Charge	Q_g	$V_{GS} = -5/18\text{ V}$	$I_D = 20\text{ A}, V_{DS} = 400\text{ V}$	-	70	-	nC
Gate-Source Charge	Q_{gs}			-	20	-	
Gate-Drain Charge	Q_{gd}			-	23	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 20\text{ A},$ $V_{GS} = -5/18\text{ V}, R_g = 2\text{ }\Omega$		-	12	15	ns
Rise Time	t_r			-	10	13	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	t_f			-	10	-	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{ open drain}$		-	2.2	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	40	A
Pulsed Diode Forward Current	I_{SM}			-	-	120	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 20\text{ A}, V_{GS} = 0$		-	-	4.1	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 20\text{ A},$ $di/dt = 1000\text{ A}/\mu\text{s}, V_R = 400\text{ V}$		-	20	-	ns
Reverse Recovery Charge	Q_{rr}			-	60	-	μC
Reverse Recovery Current	I_{RRM}			-	10	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 60 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 60 % V_{DSS} .

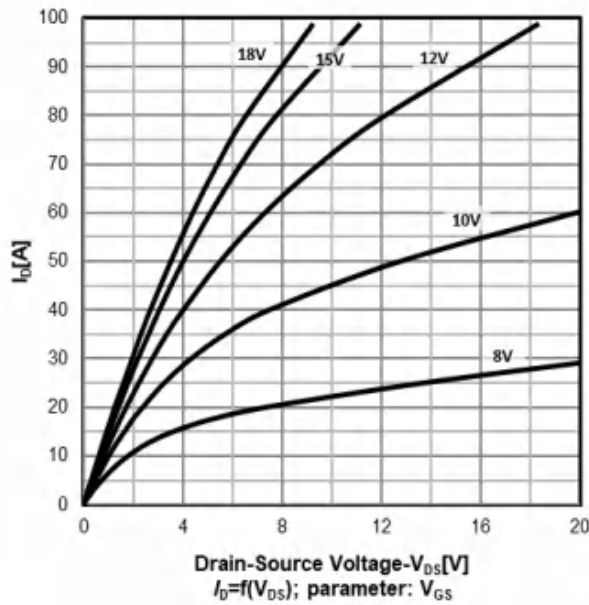
Safe operating area Tc=25 °C
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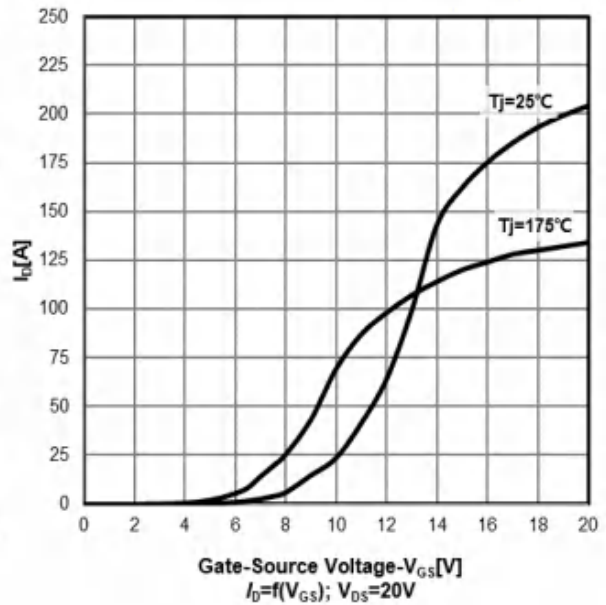
On-Region characteristics Tj=25 °C



On-Region characteristics Tj=175 °C



Transfer characteristics



Drain current vs temperature



Power dissipation



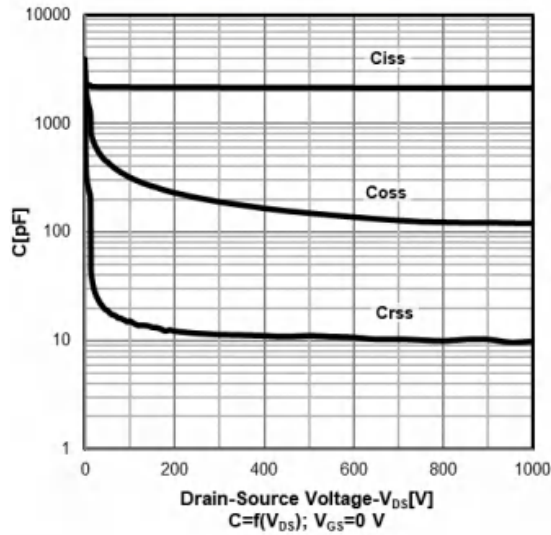
Threshold voltage vs temperature



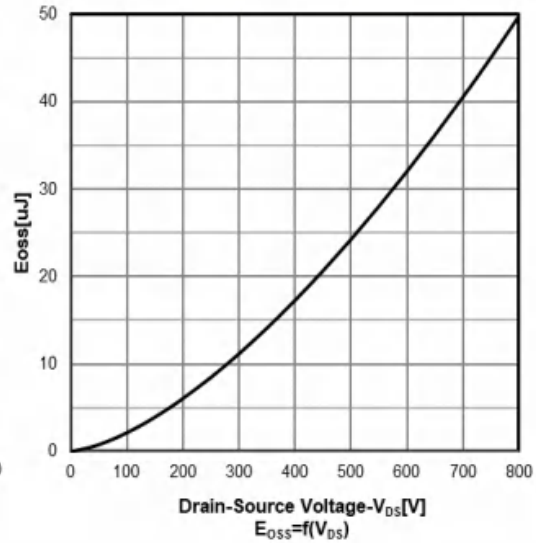
Normalized On-resistance vs temperature



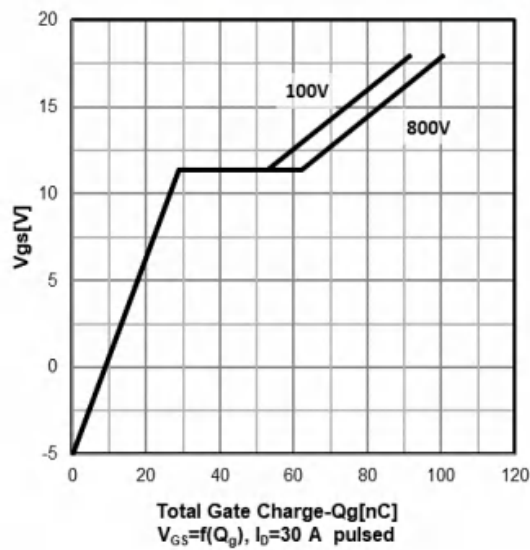
Typ. capacitances



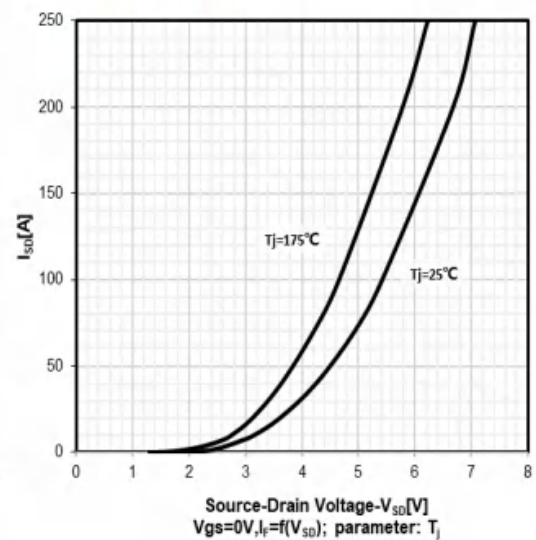
C_{oss} stored energy



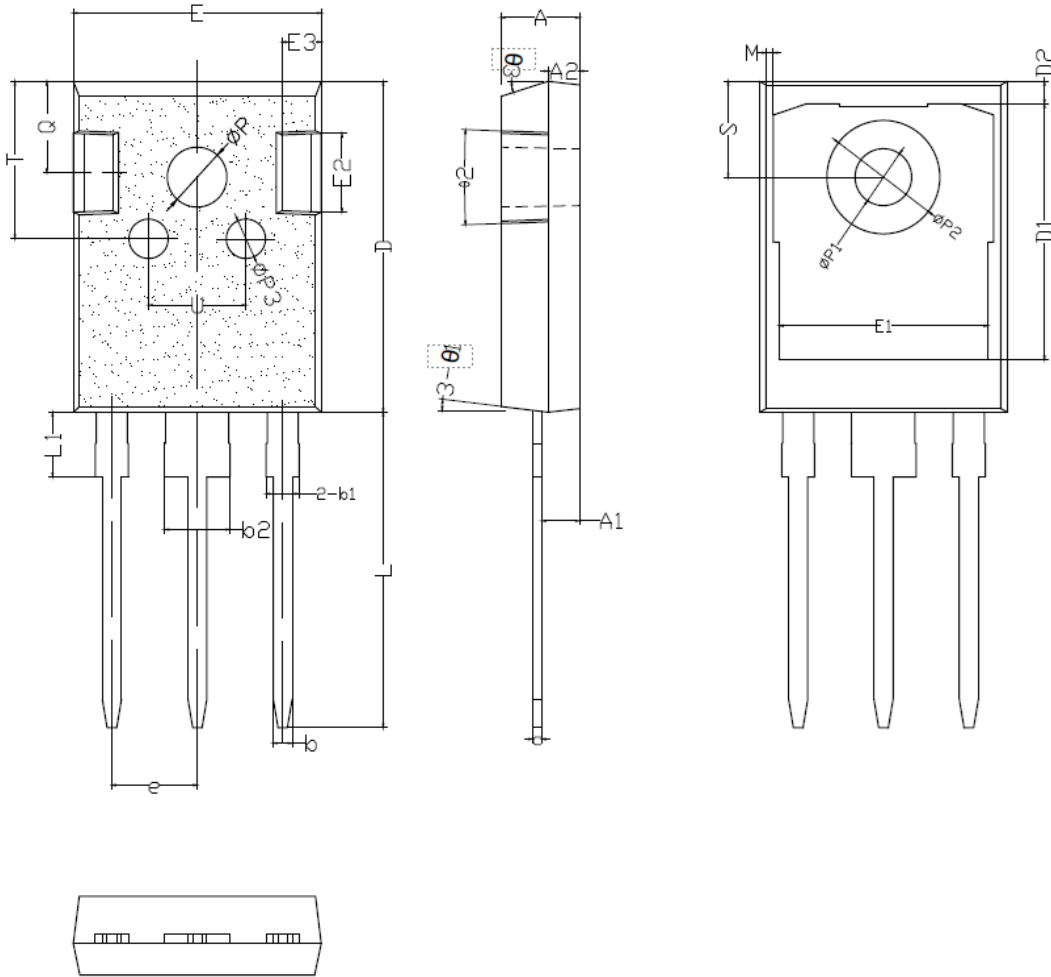
Typ. gate charge characteristics



Diode forward voltage characteristics
 $T_j=25^\circ C/175^\circ C$



TO-247 PACKAGE OUTLINE DIMENSIONS



SYMBOL	mm		
	MIN	NOM	MAX
*A	4.90	5.00	5.10
*A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
*b	1.15	1.20	1.25
*b1	1.95	2.10	2.25
*b2	2.95	3.10	3.25
*c	0.55	0.60	0.65
*D	20.90	21.00	21.10
D1	16.35	16.55	16.75
D2	1.05	1.20	1.35

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