

AOK60B65M3-VB Datasheet

650V Trench and Fieldstop IGBT

PRODUCT SUMMARY		
V_{CE} (V)	650	
I_C (A)	120 (TC=25°C)	60 (TC=100°C)
$V_{CE(sat)}$ (V)	1.7	
I_{CM} (A)	180	

FEATURES

- Very Low V_{CEsat}
- Low turn-off losses
- High speed switching
- Maximum junction temperature 175°C
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



RoHS
COMPLIANT
HALOGEN
FREE

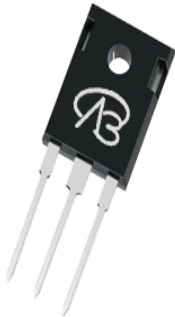
APPLICATIONS

- Telecommunications
 - Server and telecom power supplies
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Consumer and computing
 - ATX power supplies
- Industrial
 - Welding
 - Battery chargers
- Renewable energy
 - Solar (PV inverters)
- Switch mode power supplies (SMPS)

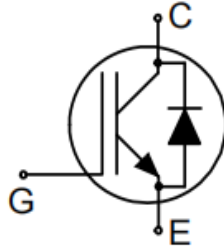
Package pin definition

- Pin1 G - Gate
- Pin2 C & backside - Collector
- Pin3 E - Emitter

TO-247



Top View



ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Collector-Emitter Voltage			V _{CE}	650	V
Gate-Emitter Voltage			V _{GE}	±30	
Continuous Collector Current (T _J = 150 °C)	V _{GE} at 15 V	T _C = 25 °C	I _C	120	A
		T _C = 100 °C		60	
Pulsed Collector Current ^a			I _{CM}	180	
Diode Forward Current ^b			I _F	60	A
Maximum Power Dissipation		T _C = 25 °C	P _D	450	W
		T _C = 100 °C		200	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Short Circuit Withstand Time ^{TC=150°C}	VGE= 15V, VCE≤ 400V		tsc	3	μs
Short Circuit Withstand Time ^{TC=100°C}	VGE= 15V, VCE≤ 330V			5	
Soldering Recommendations (Peak Temperature) ^c	for 10 s			260	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- Current limited by maximum junction temperature.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case	R_{thJC}	-	0.5	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Collector-Emitter Breakdown Voltage	BV_{CE}	$V_{GE} = 0\text{ V}$, $I_C = 250\text{ }\mu\text{A}$ $V_{GE} = 0\text{ V}$, $I_C = 1\text{ mA}$	650 650	- -	- -	V
Gate-Source Threshold Voltage (N)	$V_{GE(th)}$	$V_{CE} = V_{GE}$, $I_D = 250\text{ }\mu\text{A}$	4	5	6	V
Zero Gate Voltage Collector Current	I_{CES}	$V_{CE} = 650\text{ V}$, $V_{GE} = 0\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$	-	1	20	μA
		$V_{CE} = 650\text{ V}$, $V_{GE} = 0\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$	-	1000	-	μA
Gate-Emitter Leakage Current	I_{GES}	$V_{CE} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	100	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$V_{GE} = 15\text{ V}$ $I_C = 60\text{ A}$	-	1.8	2.1	V
Forward Transconductance	g_{fs}	$V_{CE} = 20\text{ V}$, $I_C = 60\text{ A}$	-	40	-	S
Dynamic						
Input Capacitance	C_{ies}	$V_{GE} = 0\text{ V}$, $V_{CE} = 25\text{ V}$, $f = 500\text{ KHz}$	-	6210	-	pF
Output Capacitance	C_{oes}		-	228	-	
Reverse Transfer Capacitance	C_{res}		-	60	-	
Turn-on Energy	E_{on}	$V_{CE} = 400\text{ V}$, $V_{GE} = 0/15\text{ V}$, $I_C = 60\text{ A}$, $R_g = 10\Omega$	-	0.76	-	nJ
Turn-off Energy	E_{off}		-	0.26	-	
Total Gate Charge	Q_g	$V_{GE} = 15\text{ V}$ $I_C = 60\text{ A}$, $V_{CE} = 400\text{ V}$	-	165	-	nC
Gate-Emitter Charge	Q_{ge}		-	18	-	
Gate to Collector Charge	Q_{gc}		-	23	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{CE} = 400\text{ V}$, $V_{GE} = 0/15\text{ V}$, $I_C = 60\text{ A}$, $R_g = 10\Omega$	-	72	-	ns
Rise Time	t_r		-	42	-	
Turn-Off Delay Time	$t_{d(off)}$		-	170	-	
Fall Time	t_f		-	26	-	
Internal emitter inductance measured 5 mm	L_E		-	13	-	nH
Diode Characteristics						
Diode Forward Current	I_F	IGBT symbol showing the integral reverse junction diode	-	-	60	A
Pulsed Diode Forward Current	I_{FM}		-	-	180	
Diode Forward Voltage	V_F	$I_F = 60\text{ A}$	-	1.50	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 60\text{ A}$, $di_F/dt = 200\text{ A}/\mu\text{s}$, $V_R = 400\text{ V}$	-	60	-	ns
Reverse Recovery Charge	Q_{rr}		-	0.3	-	μC
Reverse Recovery Current	I_{RRM}		-	11	-	A

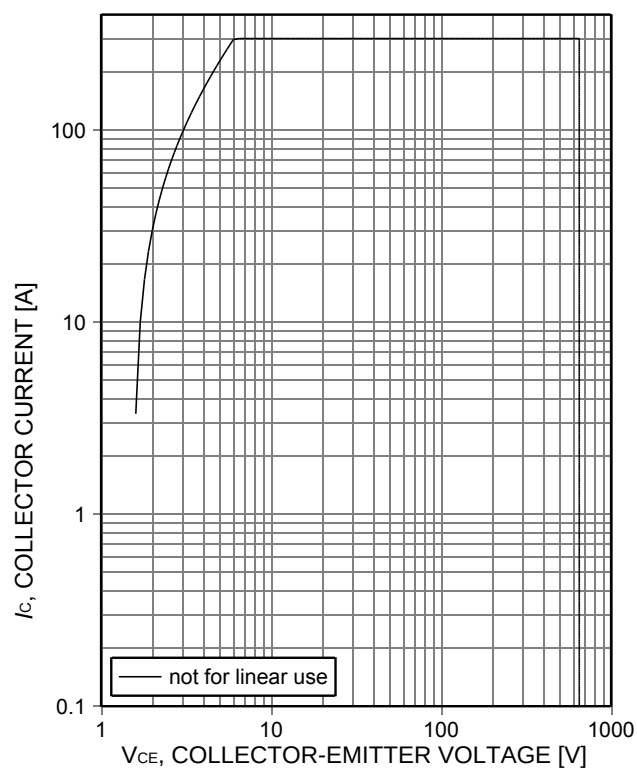


Figure 1. Forward bias safe operating area

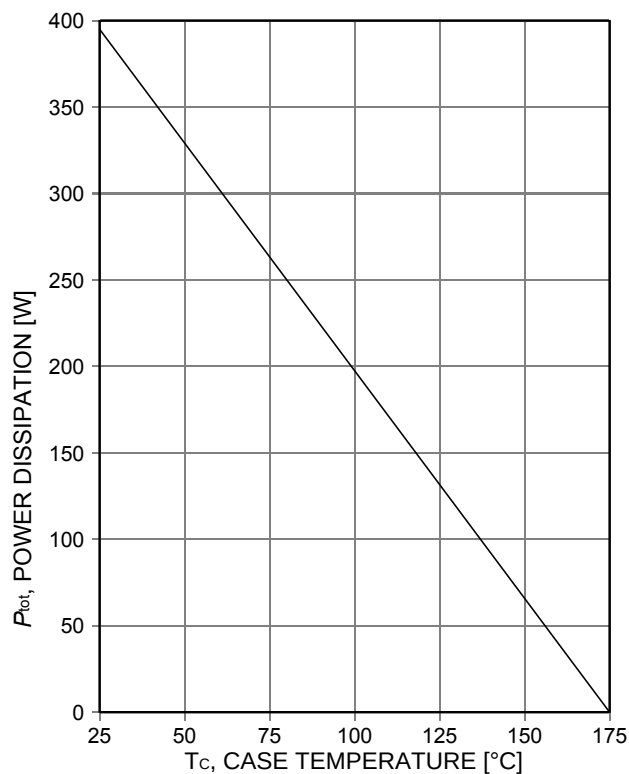


Figure 2. Power dissipation as a function of case

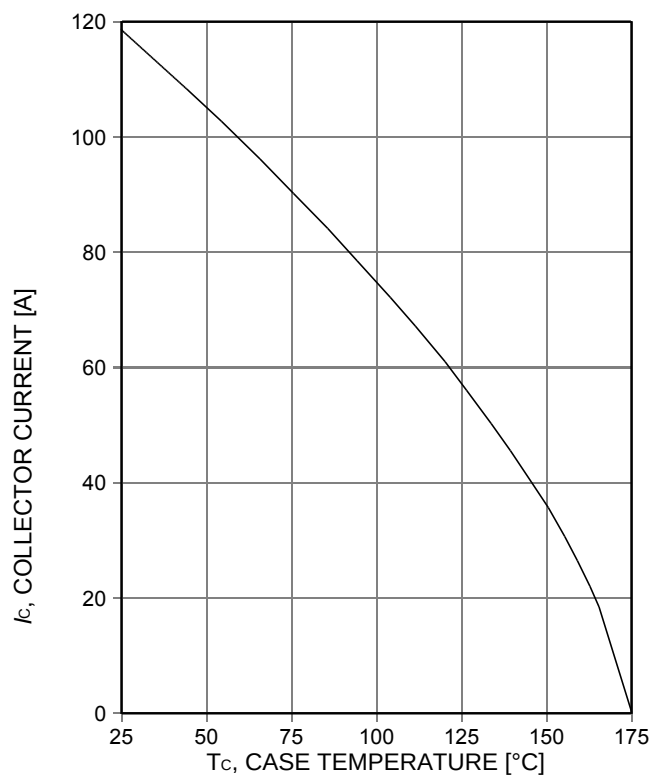


Figure 3. Collector current as a function of case temperature

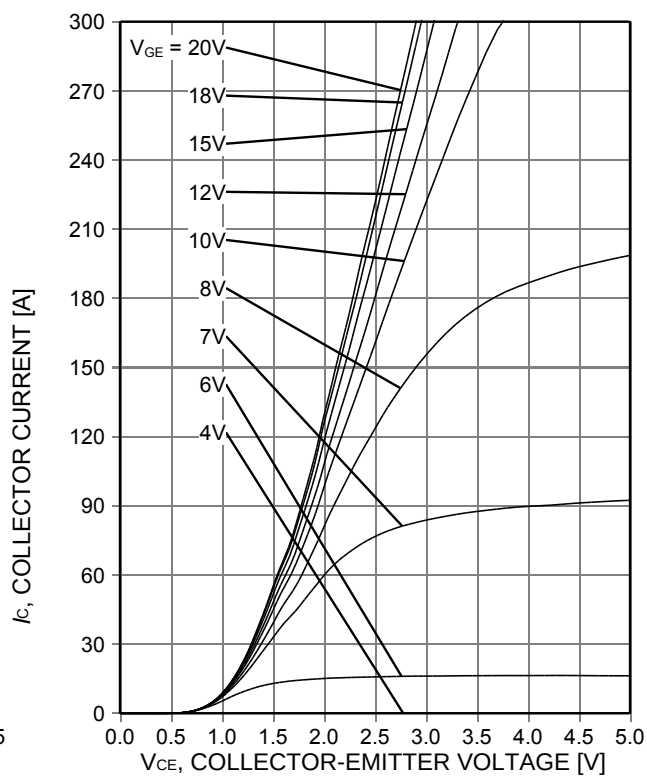


Figure 4. Typical output characteristic

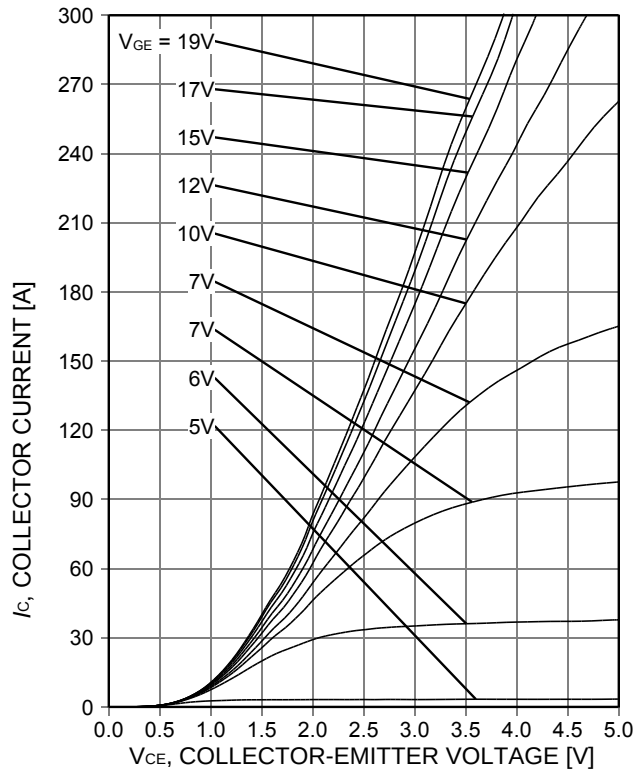


Figure 5. Typical output characteristic

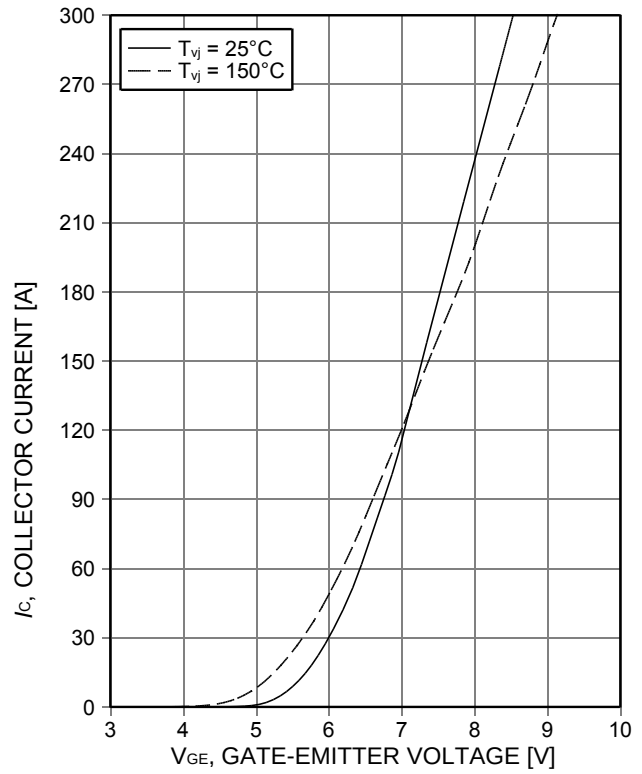


Figure 6. Typical transfer characteristic

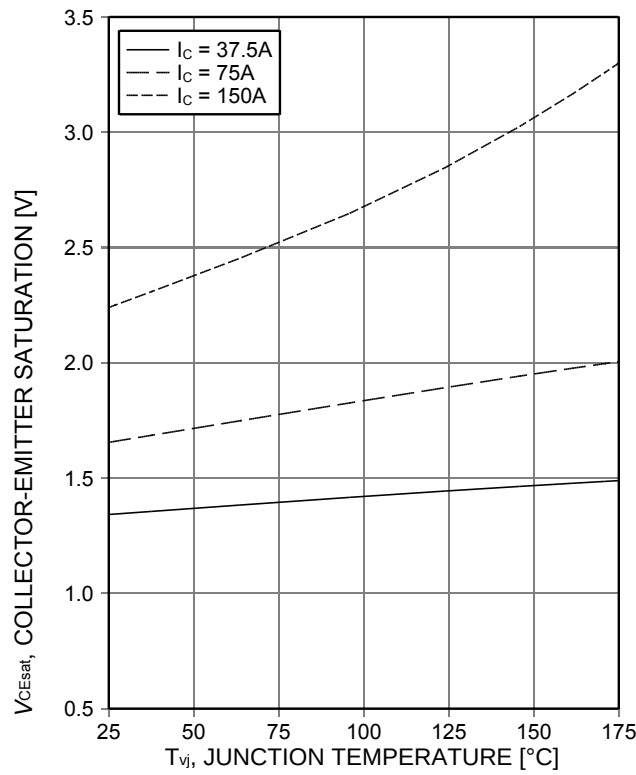


Figure 7. Typical collector-emitter saturation voltage as a function of junction temperature

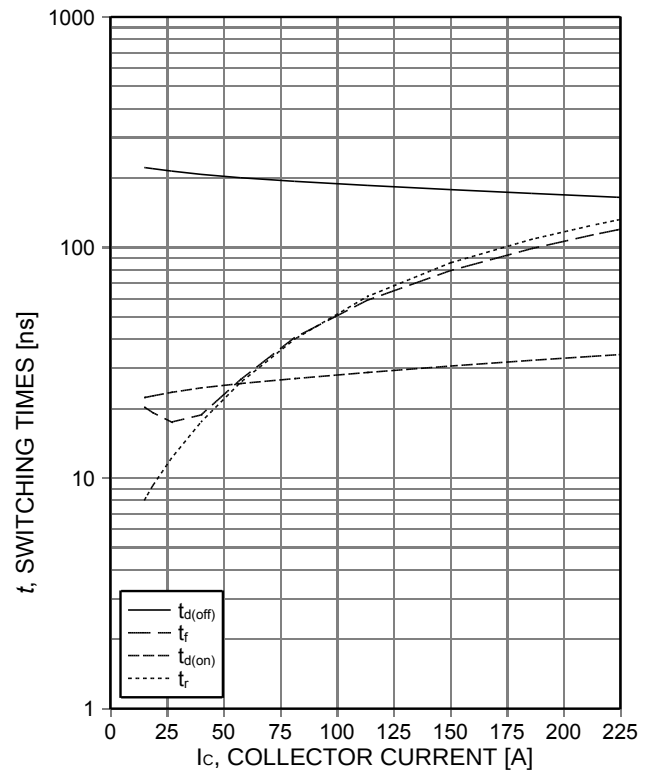


Figure 8. Typical switching times as a function of collector current

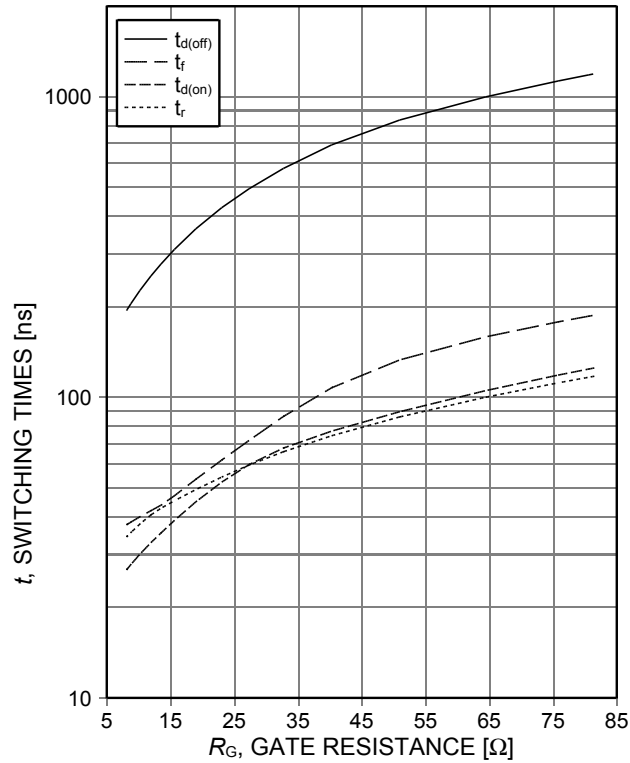


Figure 9. Typical switching times as a function of gate resistance

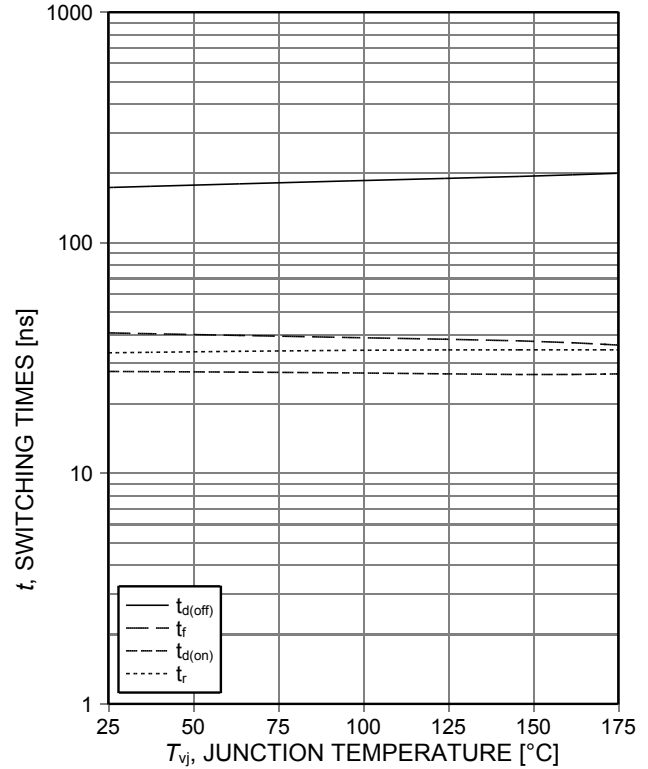


Figure 10. Typical switching times as a function of junction temperature

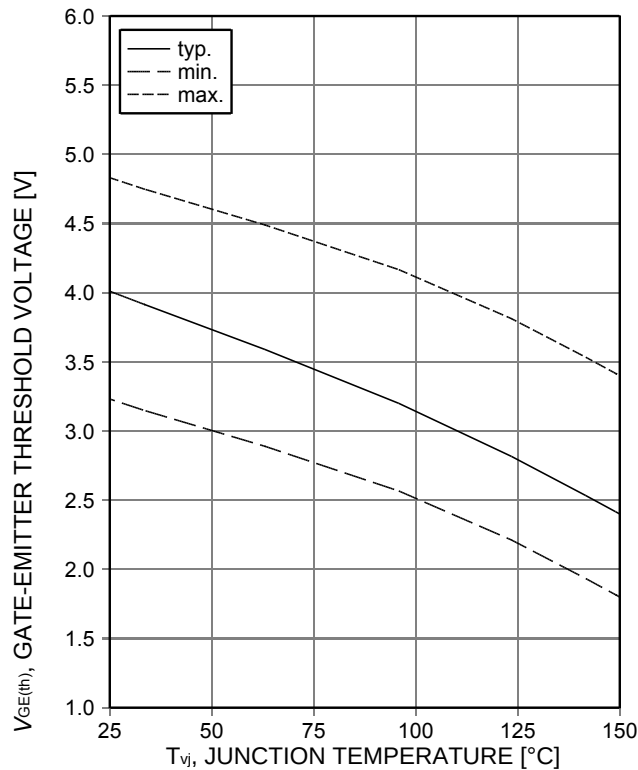


Figure 11. Gate-emitter threshold voltage as a function of junction temperature

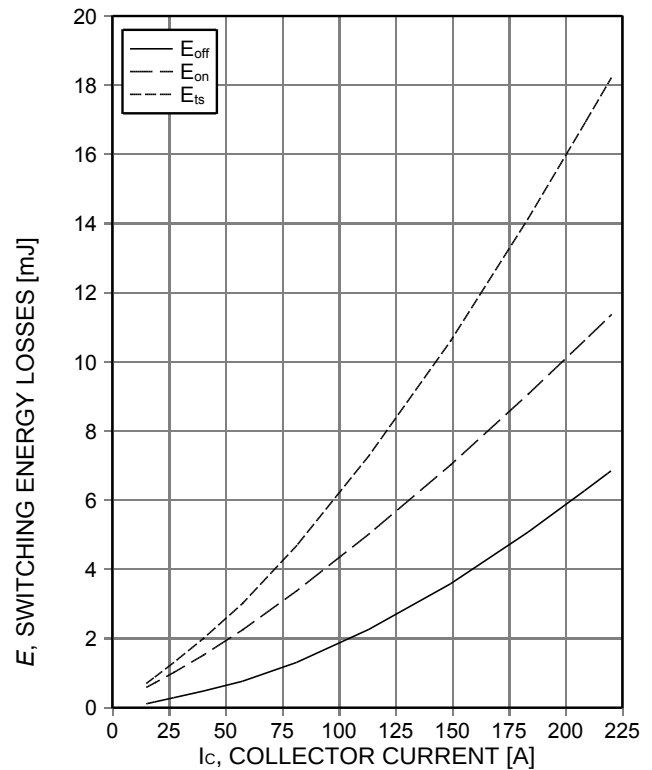


Figure 12. Typical switching energy losses as a function of collector current

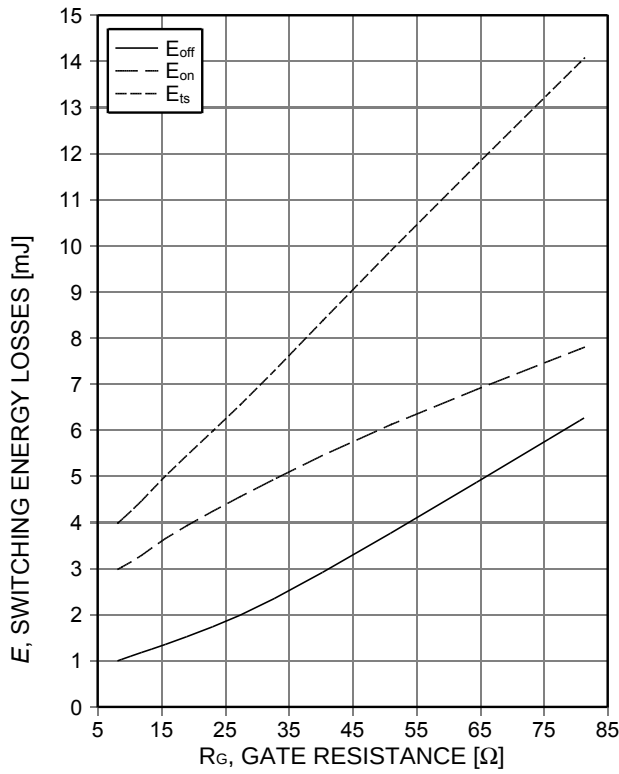


Figure 13. Typical switching energy losses as a function of gate resistance

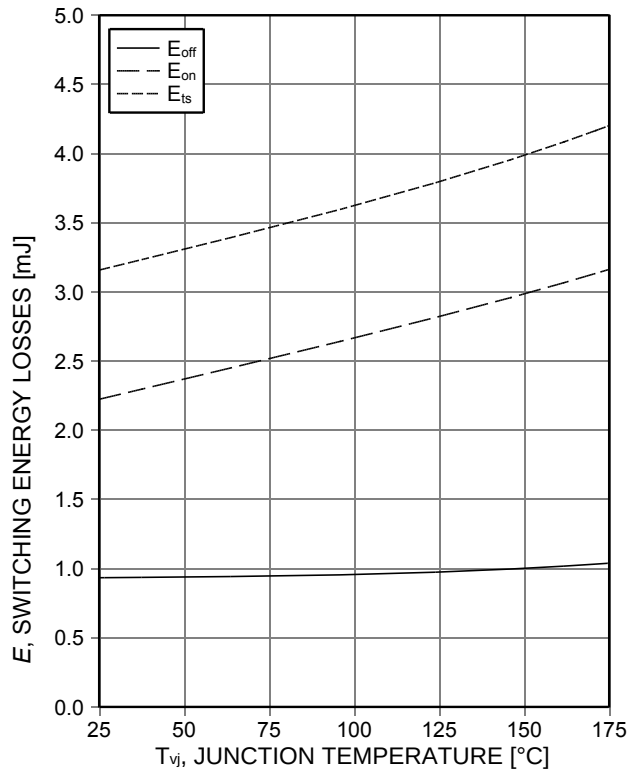


Figure 14. Typical switching energy losses as a function of junction temperature

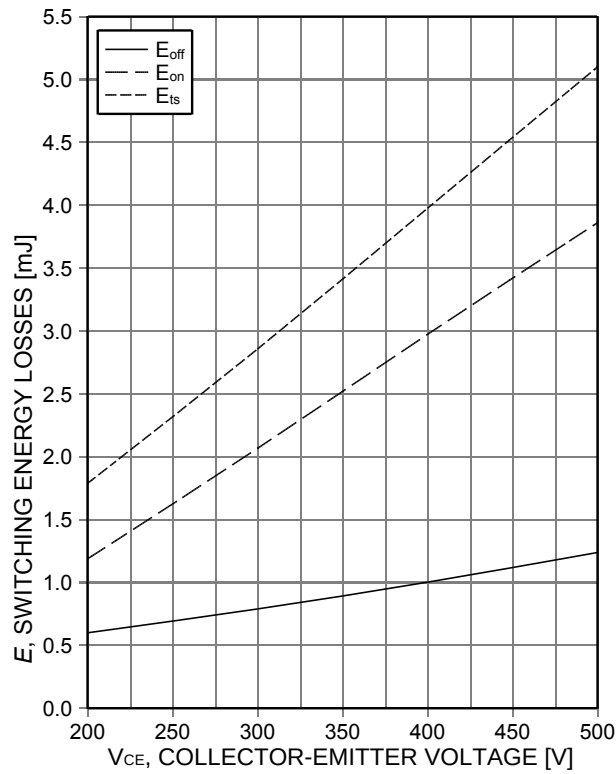


Figure 15. Typical switching energy losses as a function of collector emitter voltage

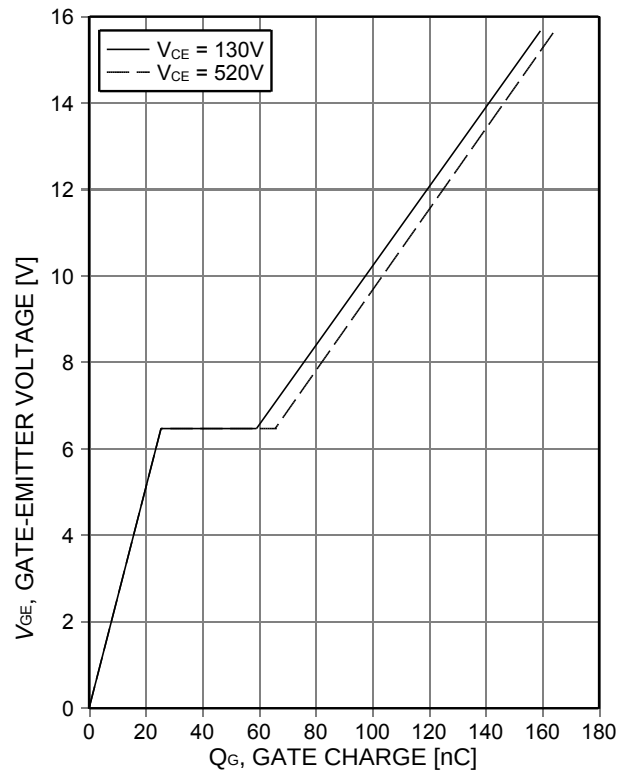
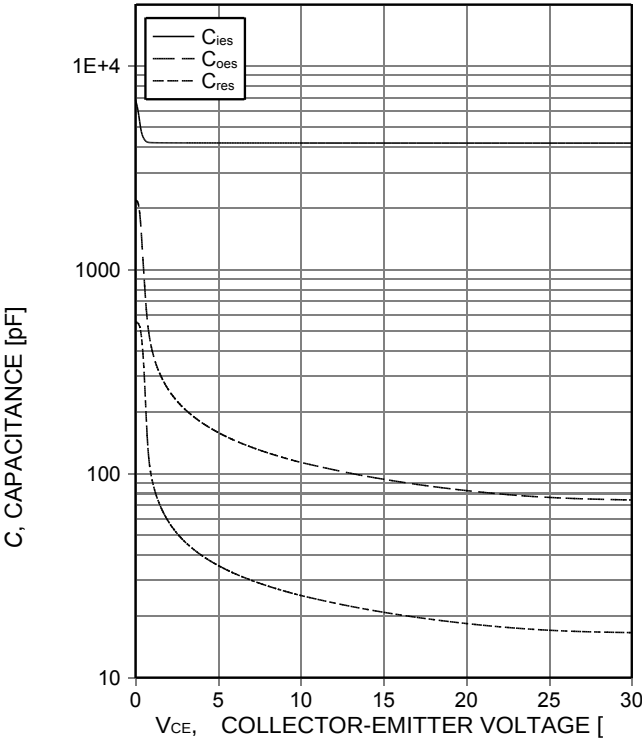


Figure 16. Typical gate charge



V]Figure 17. Typical capacitance as a function of collector-emitter voltage

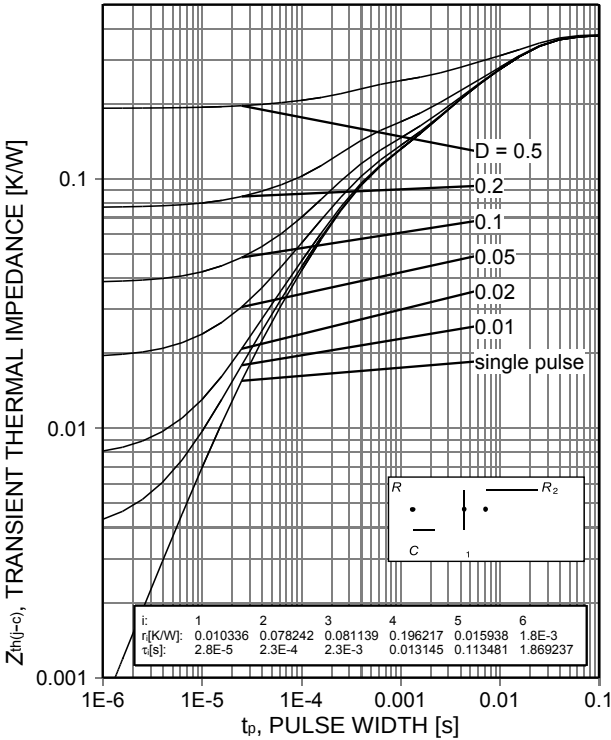


Figure 18. IGBT transient thermal impedance

Technical drawing of a microchip package showing top, side, and front views with dimensions. The top view shows a square package with a central circular feature of diameter $\varnothing p$ and a width of E . The side view shows the package height D and the distance from the base to the top of the package $D1$. The front view shows the package width A and the distance from the base to the top of the package $A2$. The package is mounted on a substrate with three leads labeled 1, 2, and 3. The distance from the base to the top of the package is L . The distance from the base to the top of the package is $L1$. The distance from the base to the top of the package is $b2$ and $b4$. The distance from the base to the top of the package is c and b .

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