Smart High-Side Power Switch
RM77200DQ Datasheet

1.Basic Features

- Very low standby current
- Electrostatic discharge (ESD) protection
- Green Product (RoHS compliant)
- Quad channel device
- 3.3V and 5V compatible logic inputs
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state

2.Description

The RM77200DQ is a 200mΩ quad channel Smart High-Side Power Switch, embedded in a DFN8*6-24 package, providing protective functions and diagnosis. The power transistor is built by an N-channel MOSFET with charge pump. It is specially designed to drive lamps up to R10W 24V or R5W 12V, as well as LEDs in the harsh automotive environment.

3.Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 12V and 24V trucks and transportation systems

4.Product Summary

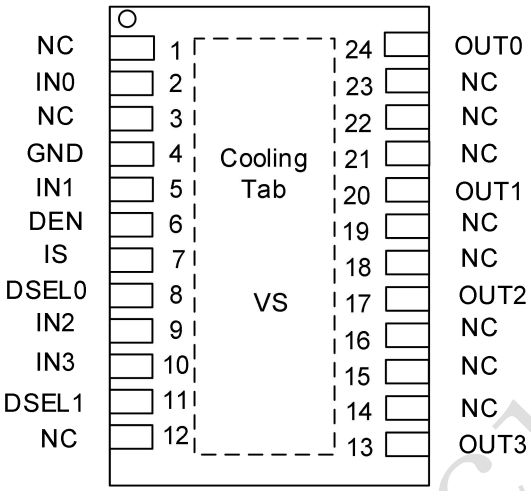
Overvoltage protection	$V_{S(AZ)}$	70	V
Operating voltage range	$V_{S(OP)}$	5...48	V
ON state resistance per channel	$R_{DS(ON)}$	140	mΩ
Nominal load current (one channel active)	$I_{L(NOM)1}$	1.5	A
Nominal load current (all channels active)	$I_{L(NOM)2}$	1	A
Load current limitation	$I_{L(SC)}$	5	A
Typical current sense ratio	k_{ILIS}	295	

5.Ordering Code

Part number	Package Type	Marking	Materials	Package			Package Qty
RM77200DQ	DFN8*6-24L	RM77200DQ	Halogen free	Tape&reel	10 reels/box	30k/box	3000/reel

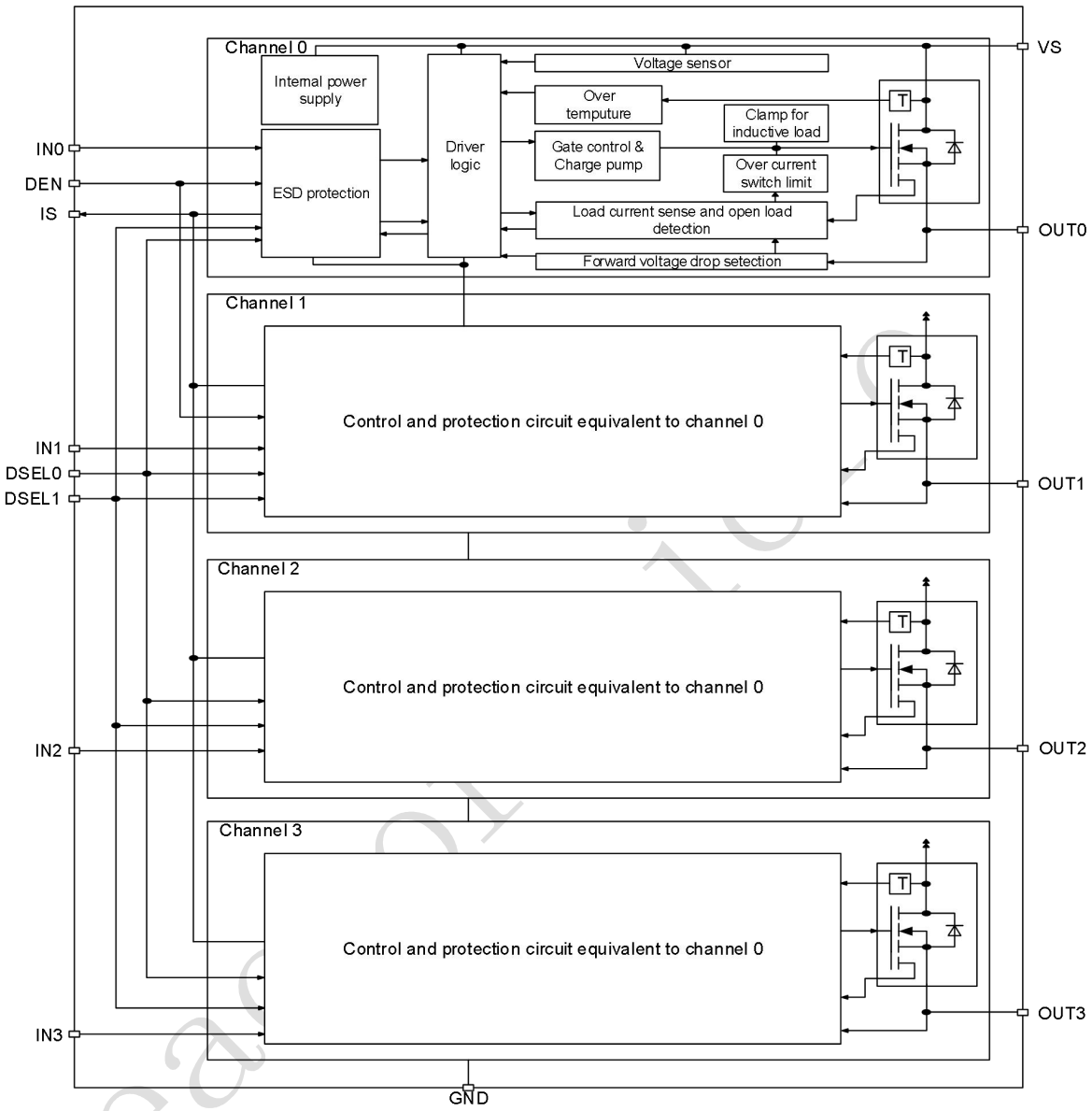
Table of Contents

6.Pin Configuration



Pin	Symbol	Function
1,3,12,14,15,16, 18,19,21,22,23	NC	Not Connected; No internal connection to the chip
2	IN0	INput channel 0; Input signal for channel 0 activation
4	GND	GrouND; Ground connection
5	IN1	INput channel 1; Input signal for channel 1 activation
6	DEN	Diagnostic ENable; Digital signal to enable/disable the diagnosis of the device
7	IS	Sense; Sense current of the selected channel
8	DSEL0	Diagnostic SELection; Digital signal to select the channel to be diagnosed
9	IN2	INput channel 2; Input signal for channel 2 activation
10	IN3	INput channel 3; Input signal for channel 3 activation
11	DSEL1	Diagnostic SELection; Digital signal to select the channel to be diagnosed
13	OUT3	OUTput 3; Protected high side power output channel 3
17	OUT2	OUTput 2; Protected high side power output channel 2
20	OUT1	OUTput 1; Protected high side power output channel 1
24	OUT0	OUTput 0; Protected high side power output channel 0
Cooling tab	VS	Voltage Supply; Battery voltage

7.Block Diagram



8.Absolute Maximum Ratings[1)]

T_J=-40°C to +150°C; (unless otherwise specified)

Parameter	Symbol	Values	Unit	
Supply voltage	V_S	-0.3 to 48	V	
Reverse polarity voltage	$-V_{S(REV)}$	0 to 28	V	t<2min T_A=25℃ R_L≥47Ω Z_{GND}=Diode+27Ω
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0 to 36	V	R_{Supply}=10mΩ L_{Supply}=5uH R_{ECU}=20mΩ R_{Cable}=16mΩ/m L_{Cable}=1uH/m, L=0or5m
Load dump protection	$V_{S(LD)}$	65	V	R_I=2Ω R_L=47Ω
Voltage at INPUT pins	V_{IN}	-0.3 to 6	V	
Current through INPUT pins	I_{IN}	-2 to 2	mA	
Voltage at DEN pin	V_{DEN}	-0.3 to 6	V	
Current through DEN pin	I_{DEN}	-2 to 2	mA	
Voltage at DSEL pin	V_{DSEL}	-0.3 to 6	V	
Current through DSEL pin	I_{DSEL}	-2 to 2	mA	
Voltage at IS pin	V_{IS}	-0.3 to V_S	V	
Current through IS pin	I_{IS}	-20 to 20	mA	
Current through ground pin	I_{GND}	-20 to 20	mA	
Power dissipation(DC), T_A=85°C	P_{TOT}	1.48	W	T_A=85℃ T_J<150℃
Junction to board Both channels active[2)]	R_{thJB}	33.6	K/W	
Maximum energy dissipation Single pulse (one channel)	E_{AS}	20	mJ	$I_{L(0)}$=1A $T_{J(0)}$=150℃ V_S=28V
Junction temperature	T_J	-40 to 150	℃	
Ambient temperature	T_A	-40 to 125	℃	
Storage temperature	T_{STG}	-55 to 150	℃	

Notes:

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditiosn for extended periods may affect device reliability.
2. Specified R_{thJB} value is according to JEDEC JESD51-2, -5, -7 at natural convection on FR4 2s2p board with 1 W power dissipation equally dissipated for both channel at T_A =105°C ; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 um Cu, 2 x 35 um Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer.

9.Electrical Characteristics

T_J=- 40°C to 150°C, V_S=28V; (unless otherwise specified)

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ	Max	
$R_{DS(ON)}$	ON-state resistance per channel	I_L=1A, V_{IN}=4.5V, T_J=25℃	-	140	200	mΩ
		I_L=1A, V_{IN}=4.5V, T_J=150℃		190	300	
$I_{L(NOM)}$	Nominal load current	T_A=85℃, T_J<150℃, (one channel)	-	1.5	-	A
		T_A=85℃, T_J<150℃, (four parallel channels)	-	1	-	A
$I_{OUT(GND)}$	Output leakage current while GND disconnected	GND disconnected	-	0.01	-	mA
t_{on}	Turn-ON time	R_L=47Ω, V_S=28V, V_{IN} Turn-ON time to 90% V_{OUT}	20	65	150	us
t_{off}	Turn-OFF time	R_L=47Ω, V_S=28V, V_{IN} Turn-OFF time to 10% V_{OUT}	10	60	150	us
Δt_{SW}	Turn-ON / OFF matching t_{ON}-t_{OFF}		-50	-	50	us
t_{on_delay}	Turn-ON delay time	R_L=47Ω, V_S=28V, V_{IN} Turn-ON time to 10% V_{OUT}	-	60	120	us
t_{off_delay}	Turn-OFF delay time	R_L=47Ω, V_S=28V, V_{IN} Turn-OFF time to 90% V_{OUT}	-	35	70	us
dV/dt_{ON}	Turn-ON Slew rate	R_L=47Ω, V_S=28V, From 30% to 70% V_{OUT}	0.3	1	1.7	V/us
dV/dt_{OFF}	Turn-OFF Slew rate	R_L=47Ω, V_S=28V, From 70% to 30% V_{OUT}	0.3	1	2.3	V/us
$V_{S(OP)}$	Operating voltage	V_{IN}=4.5V, R_L=47Ω	5	-	48	V
$V_{S(UV)}$	Undervoltage shutdown	V_{IN}=4.5V, V_{DEN}=0V, R_L=47Ω, From V_{DS}<1V to I_{OUT}=0A	3.2	3.7	4.5	V
$V_{S(OP)\_MIN}$	Minimum functional supply voltage	V_{IN}=4.5V, R_L=47Ω, From I_{OUT}=0A to V_{DS}<0.5V;	3.8	4.5	5	V
$V_{S(UV)\_HYS}$	Undervoltage shutdown hysteresis			0.85		V
$I_{S(OFF)}$	Standby current for whole device with load (ambient)	V_S=36V, V_{OUT}=0V, V_{IN} floating, V_{DEN} floating, T_J≤85°C	-	0.1	0.5	uA
$V_{DS(AZ)}$	Drain to source clamping voltage	$V_{DS(AZ)}$=[V_S-V_{OUT}], I_{DS}=5mA	65	70	75	V
$V_{S(AZ)}$	Overvoltage protection	I_{SOV}=5mA	65	70	75	V
$I_{L(off)}$	Output leakage current per channel	V_{IN} floating, V_{OUT}=0, T_J=25°C	-	0.1	0.5	uA
		V_{IN} floating, V_{OUT}=0, T_J=150°C	-	1	5	
I_{GND_1}	Operating current (One channel active)	V_{IN}=V_{DEN}=5.5V, V_S=36V	-	1	3	mA

I_{GND_4}	Operating current (All channels active)	V_{IN}=V_{DEN}=5.5V, V_S=36V	-	2.5	7	mA
$I_{L(SC)}$	Load current limitation		4	5.5	10	A
K_{ILIS1}	Current sense ratio	I_L=0.05A, V_{IN}=V_{DEN}=4.5V	-40%	260	+40%	
K_{ILIS2}	Current sense ratio	I_L=0.2A, V_{IN}=V_{DEN}=4.5V	-15%	285	+15%	
K_{ILIS3}	Current sense ratio	I_L=0.5A, V_{IN}=V_{DEN}=4.5V	-11%	290	+11%	
K_{ILIS4}	Current sense ratio	I_L=1A, V_{IN}=V_{DEN}=4.5V	-9%	295	+9%	
$V_{IN(H)}$	High level input voltage threshold		1.5	-	2.3	V
$V_{IN(L)}$	Low level input voltage threshold		1	-	2	V
$V_{IN(HYS)}$	Input voltage hysteresis		0	0.35	-	V
$I_{IN(H)}$	High level input voltage threshold	V_{IN}=5.5V	2	20	40	uA
$I_{IN(L)}$	Low level input voltage threshold	V_{IN}=0.8V	1	4	25	uA
$V_{DEN(H)}$	High level input voltage threshold		1.5	-	2.3	V
$V_{DEN(L)}$	Low level input voltage threshold		1	-	2	V
$V_{DEN(HYS)}$	Input voltage hysteresis		0	0.35	-	V
$I_{DEN(H)}$	High level input current	V_{DEN}=5.5V	2	12	25	uA
$I_{DEN(L)}$	Low level input current	V_{DEN}=0.8V	1	4	25	uA
$V_{DSEL(H)}$	High level input voltage threshold		1.5	-	2.3	V
$V_{DSEL(L)}$	Low level input voltage threshold		1	-	2	V
$V_{DSEL(HYS)}$	Input voltage hysteresis		0	0.35	-	V
$I_{DSEL(H)}$	High level input current	V_{DSEL}=5.5V	2	12	25	uA
$I_{DSEL(L)}$	Low level input current	V_{DSEL}=0.8V	1	4	25	uA
$V_{DS(NL)}$	Output voltage drop limitation at small load currents	I_L=25mA	-	10	22	mV
V_S-$V_{OL(OFF)}$	Open load detection threshold in OFF state	V_{IN}=0V, V_{DEN}=4.5V	3	-	5	V
$I_{L(OL)}$	Open load detection threshold in ON state	V_{IN}=V_{DEN}=4.5V, $I_{IS(OL)}$=33uA	2	-	15	mA
$I_{IS\_(DIS)}$	IS pin leakage current when sense is disabled	V_{IN}=4.5V, V_{DEN}=0V, I_L=1A	-	0.02	1	uA
$I_{IS(FAULT)}$	Sense signal maximum current in fault condition	V_{IS}=V_{IN}=V_{DSEL}=0V, V_{OUT}=V_S>10V, V_{DEN}=4.5V	3	4	8	mA
$I_{IS(OLOFF)}$	SENSE Open Load in OFF Current		1	1.6	2	mA
$V_{IS(AZ)}$	Sense pin maximum voltage VS to IS	I_{IS}=5mA	65	70	75	V
$T_{J(SC)}$	Thermal shutdown temperature		150	-	-	℃
$\Delta T_{J(SC)}$	Thermal shutdown hysteresis		-	20	-	K
$t_{sIS(ON)}$	Current sense settling time to k_{ILIS} function stable after positive input slope on both INput and DEN	V_{DEN}=V_{IN}=0V to 4.5V, V_S=28V, R_{IS}=1kΩ, C_{SENSE}<100pF, I_L=0.5A	-	120	200	us
$t_{sIS(ON\_DEN)}$	Current sense settling time with load current stable and transition of the DEN	V_{DEN}=0V to 4.5V, V_S=28V, R_{IS}=1kΩ, C_{SENSE}<100pF, I_L=0.5A	-	20	40	us

$t_{sIS(LC)}$	Current sense settling time to I_{IS} stable after positive input slope on current load	V_{DEN}=4.5V, R_{IS}=1kΩ, C_{SENSE}<100pF, I_L=0.2A to I_L=0.5A	-	8	15	us
$t_{sIS(FAULT\_OL\_OFF)}$	Current sense settling time to I_{IS} stable for open load detection in OFF state	V_{DEN}=0V to 4.5V, R_{IS}=1kΩ, C_{SENSE}<100pF, V_{OUT}=V_S=28V	-	110	180	us
$t_{sIS(FAULT\_OL\_ON\_OFF)}$	Current sense settling time to I_{IS} stable for open load detection in ON-OFF transition	V_{IN}=4.5V to 0V, V_{DEN}=4.5V, R_{IS}=1kΩ, C_{SENSE}<100pF, V_{OUT}=V_S=28V	-	130	180	us
$t_{sIS(FAULT)}$	Current sense settling time to I_{IS} stable for overload detection	V_{IN}=V_{DEN}=0V to 4.5V, R_{IS}=1kΩ, C_{SENSE}<100pF, V_{DS}=5V	-	-	200	us
$t_{sIS(OFF)}$	Diagnostic disable time DEN transition to I_{IS}<50% I_L/k_{ILIS}	V_{DEN}=4.5V to 0V, V_{IN}=4.5V, V_S=28V, R_{IS}=1kΩ, C_{SENSE}<100pF, I_L=0.5A	-	3	20	us
$t_{sIS(ChC)}$	Current sense settling time from one channel to another	V_{IN0}=V_{IN1}=4.5V, V_{DEN}=4.5V, V_{DSEL}=0V to 4.5V, R_{IS}=1kΩ, C_{SENSE}<100pF, $I_{L(OUT0)}$=0.5A, $I_{L(OUT1)}$=0.2A		20	40	us
$V_{DS(REV)}$	Drain source diode voltage during reverse polarity	I_L=-1A	200	850	1050	mV

10.Timing diagrams

Figure 1: Switching a Resistive Load Timing

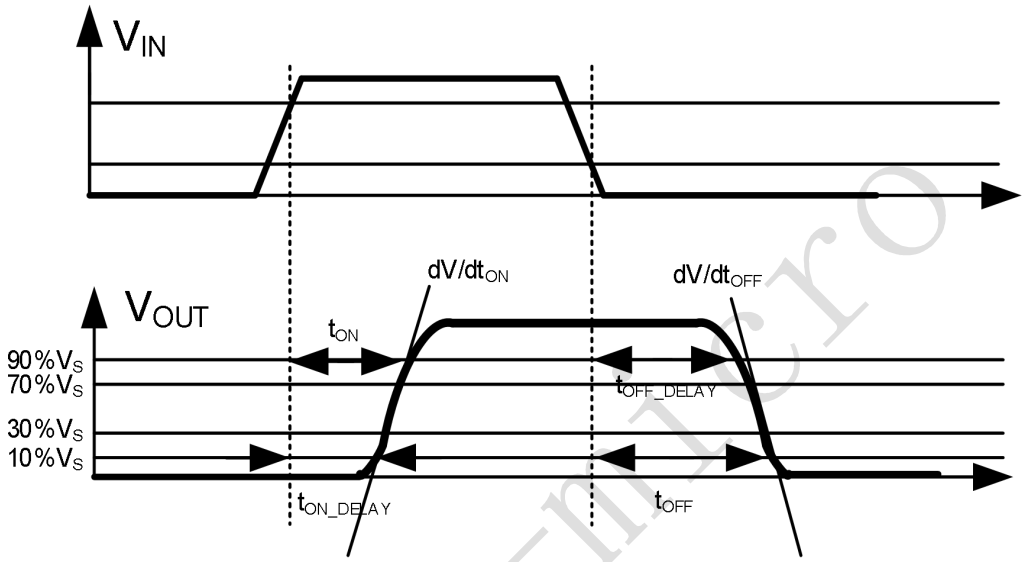


Figure shows the typical timing when switching a resistive load

Figure 2: Switching an Inductive Load Timing

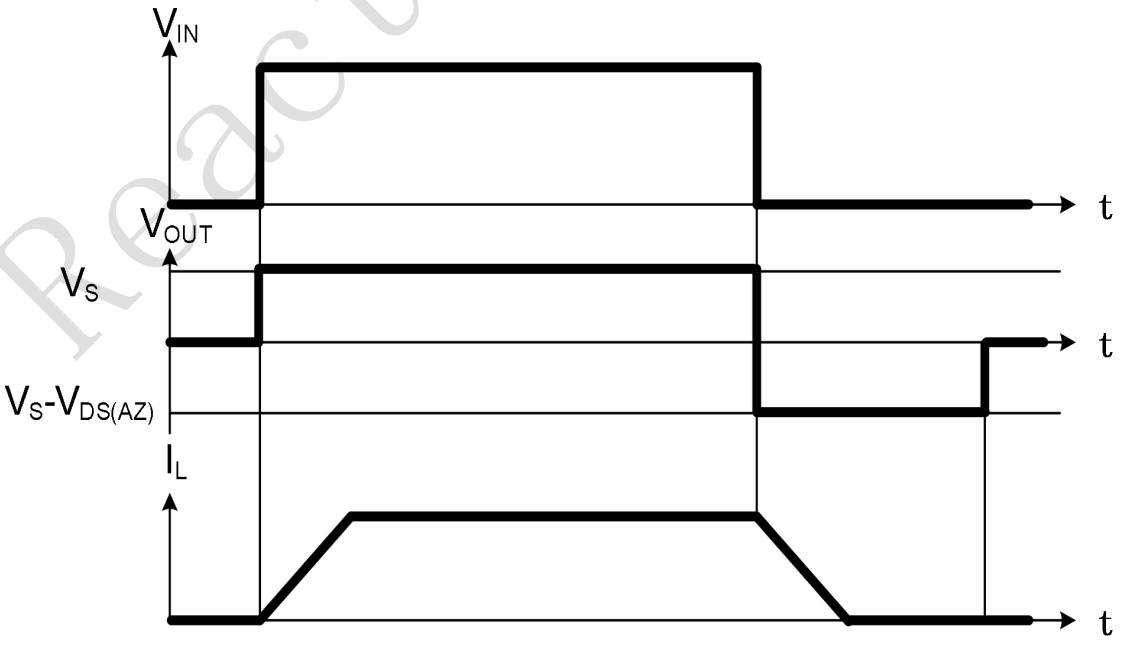


Figure 3: SENSE Settling / Disabling Timing

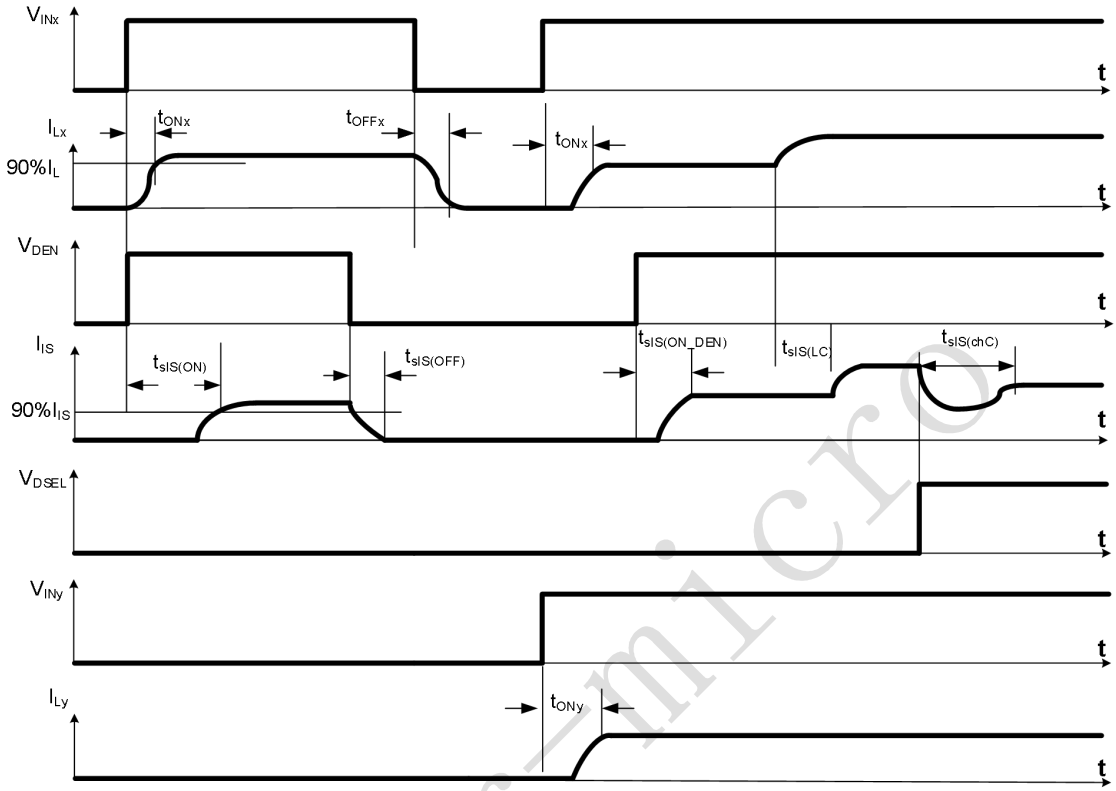


Figure 4: SENSE Signal in Open Load Timing

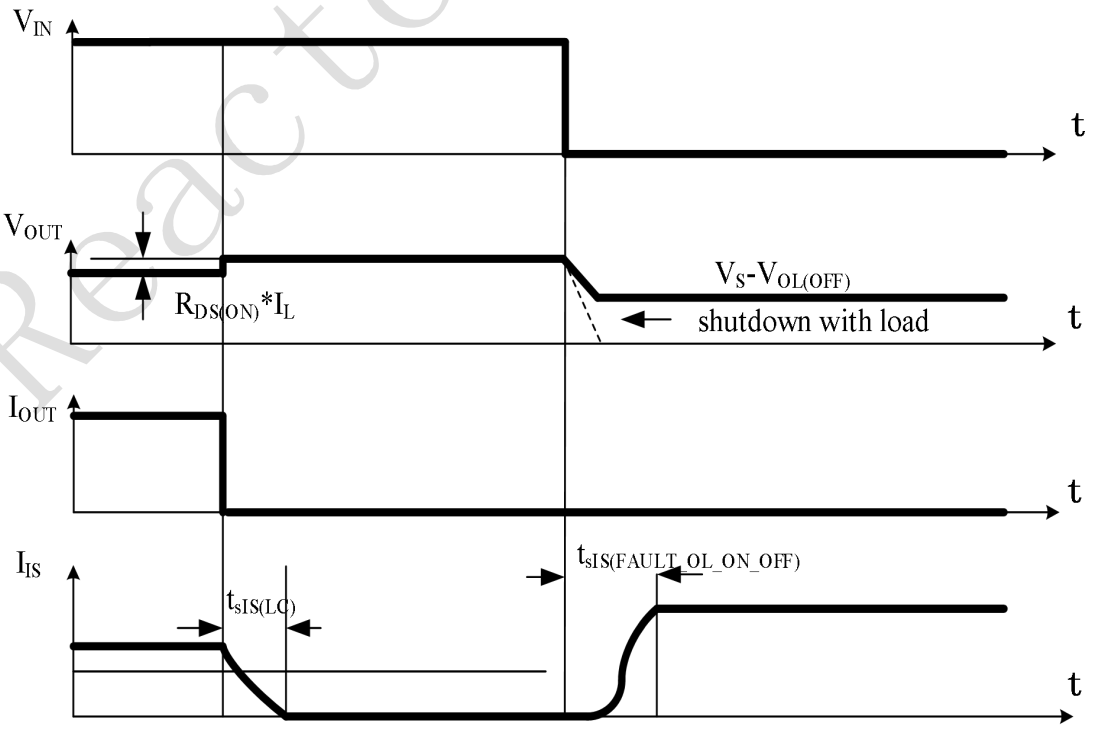


Figure 5: Undervoltage Behavior

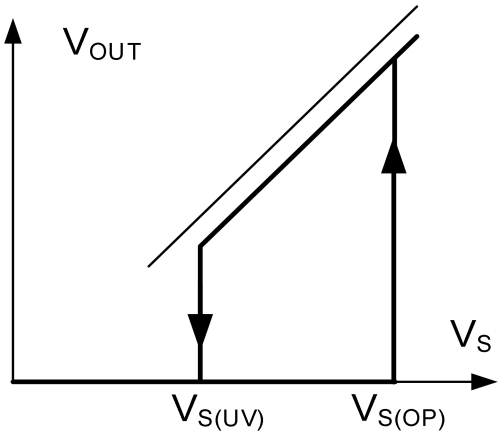
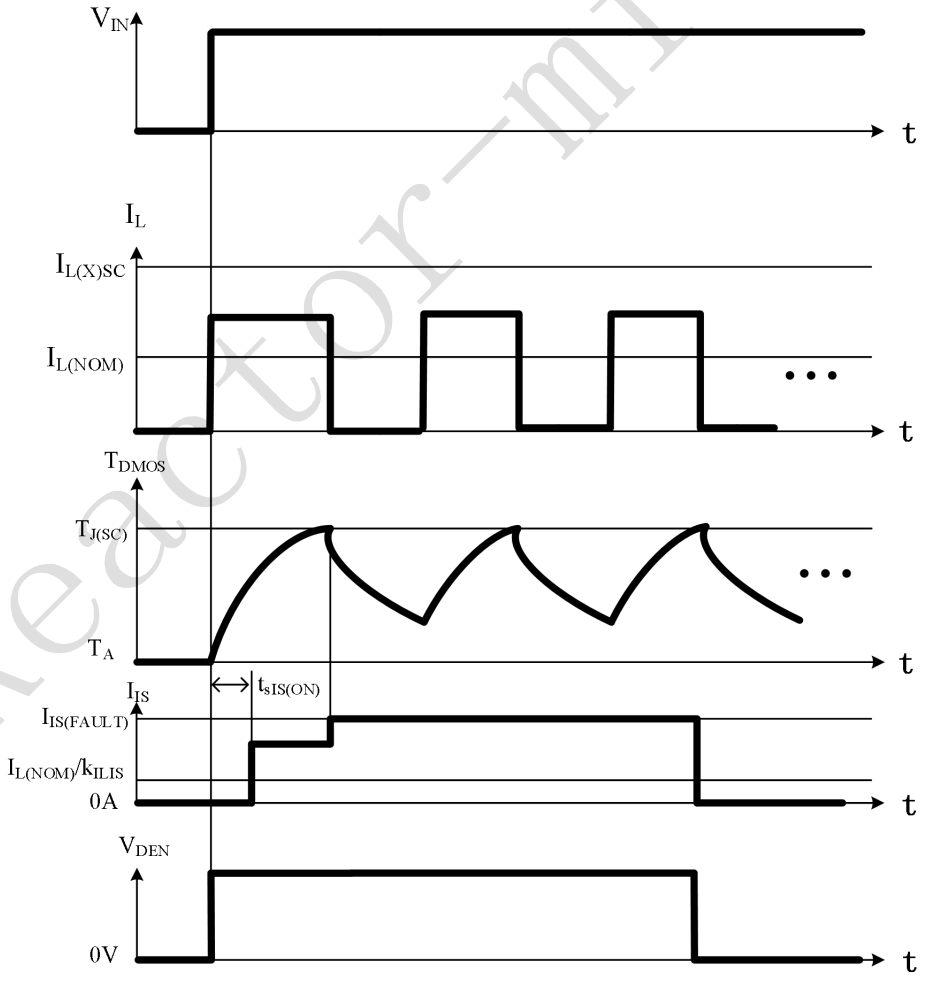


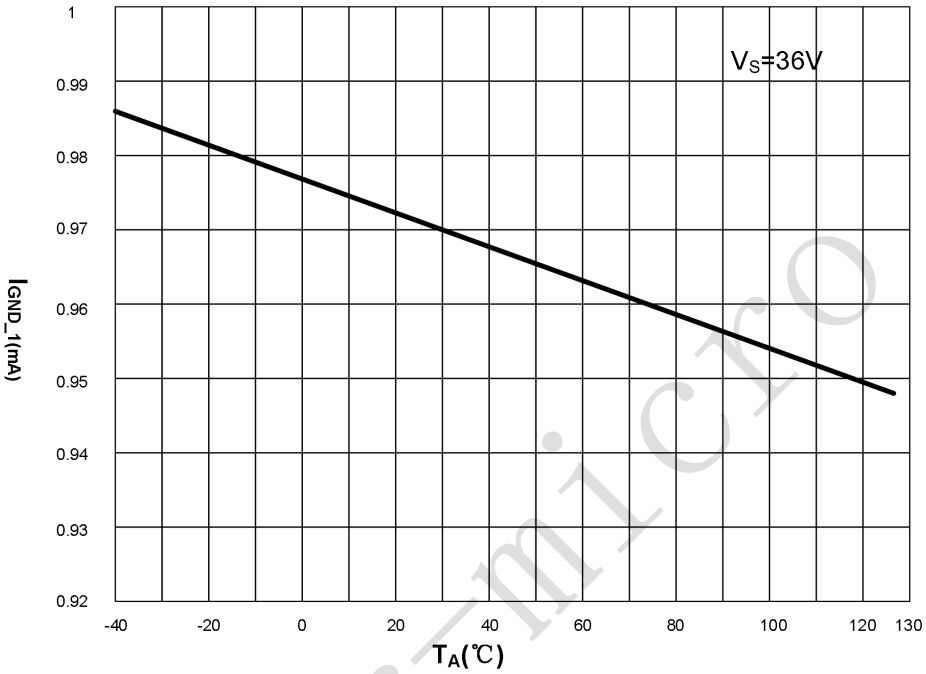
Figure 6: Overload Protection and Overtemperature Protection



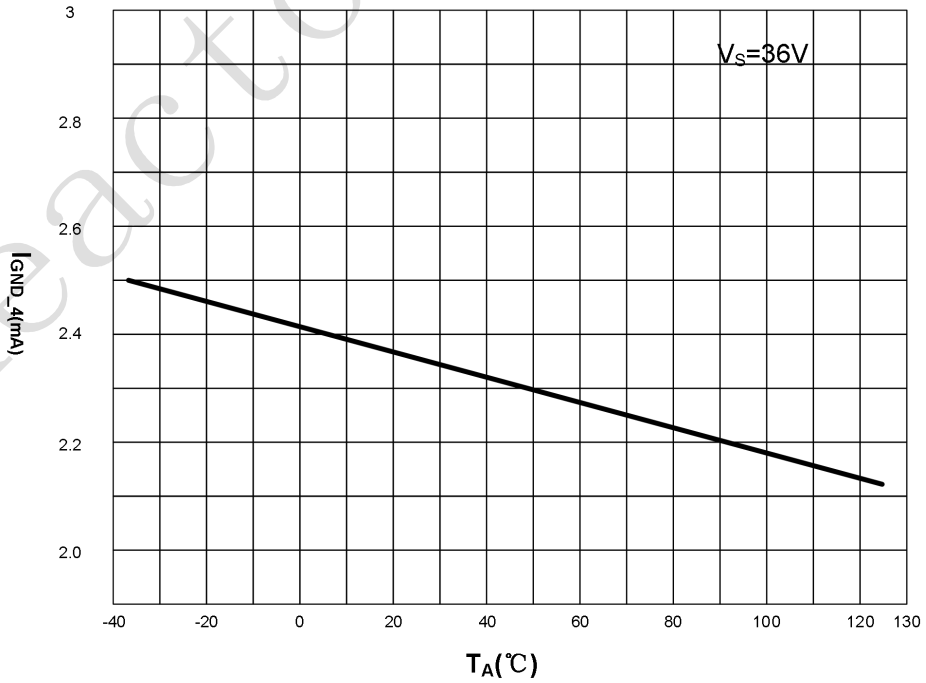
Retry strategy is implemented such that when the DMOS temperature has cooled down enough, the switch is switched ON again.

11.General Product Characteristics

Operating current

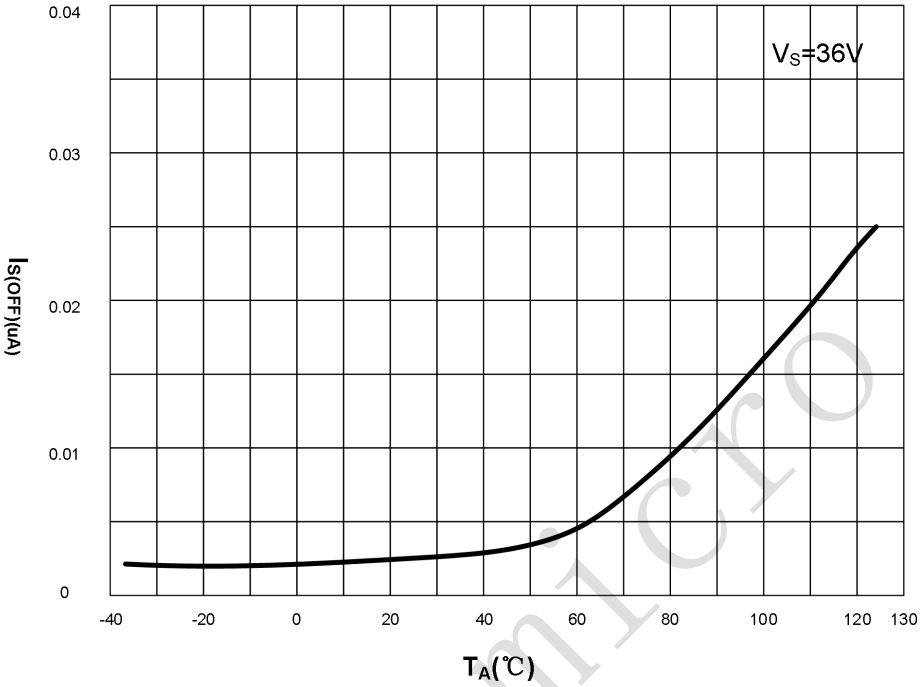


One Channel Active I_{GND_1}= f(T_A)

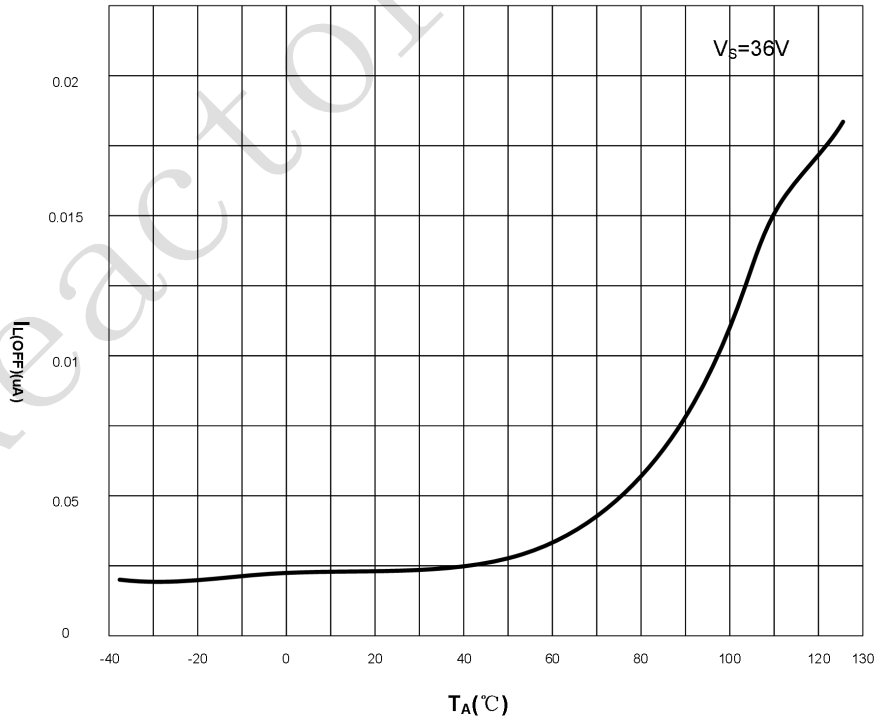


All Channels Active I_{GND_4}= f(T_A)

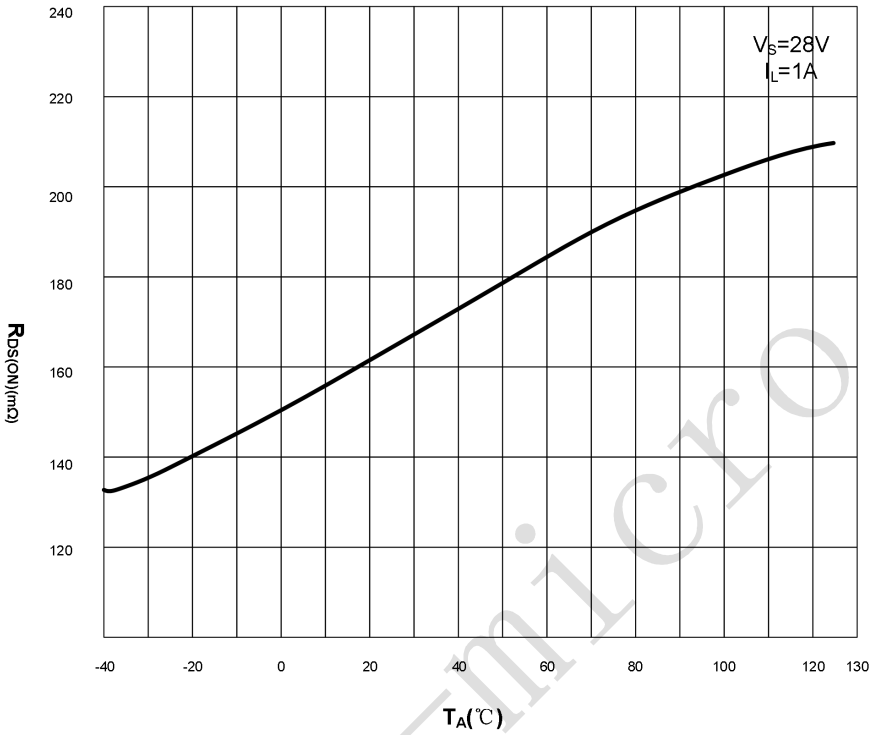
Standby Current for Whole Device with Load



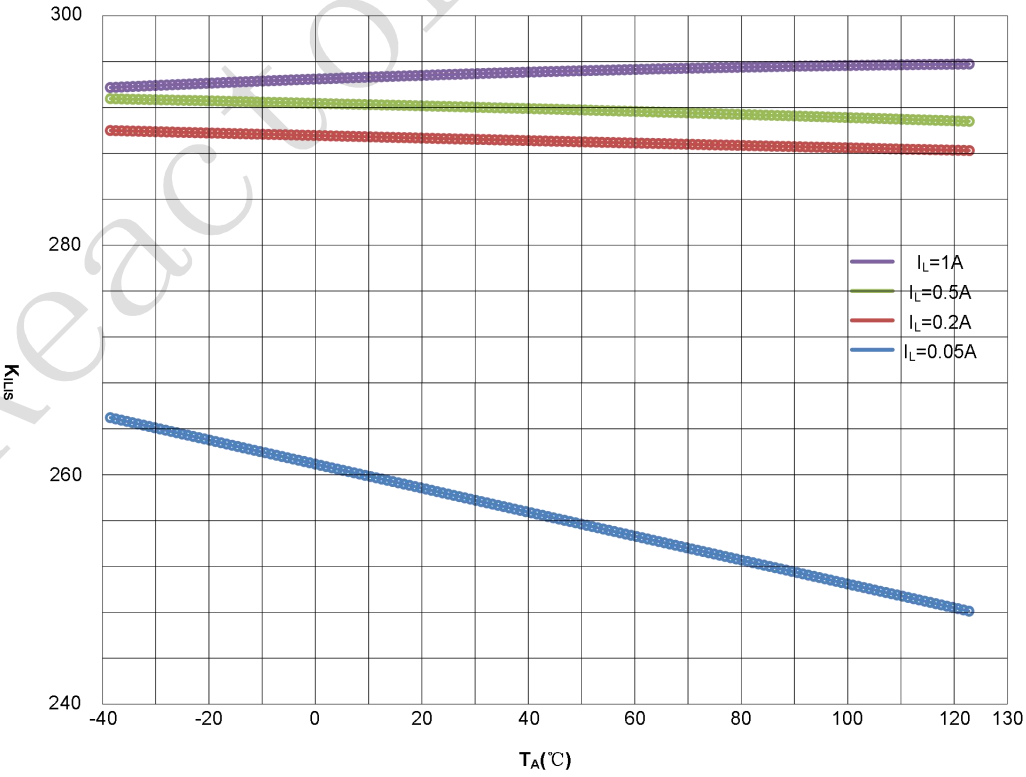
Output leakage current per channel



Typical ON-State Resistance



Current Sense



11.Truth Table

Operation Mode	Input level Channel x	DEN	Output Level	Diagnostic Output
Normal operation	L H	H	Z ~V_S	Z $I_{IS}=I_L/K_{ILIS}$
Short circuit to GND	L H	H	~GND ~GND	Z $I_{IS(FAULT)}$
Overtemperature	L H	H	Z Z	Z $I_{IS(FAULT)}$
Short circuit to VS	L H	H	V_S V_S	$I_{IS(FAULT)}$ $I_{IS}<I_L/K_{ILIS}$
Open Load	L L H	H	$<V_{OL(OFF)}$ [1] $>V_{OL(OFF)}$ [1] ~V_S [2]	Z $I_{IS(FAULT)}$ $I_{IS}<I_{IS(OL)}$
Inverse current	L H	H	~V_{INV} ~V_{INV}	$I_{IS(FAULT)}$ $I_{IS}<I_{IS(OL)}$ [3]
Current limitation	H	H	$<V_S$	$I_{IS(FAULT)}$
Underload	H	H	~V_S [4]	$I_{IS(OL)}<I_{IS}<I_L/K_{ILIS}$
Don't care	Don't care	L	Don't care	Z

L="Low" Level, H="High" Level

1) Stable with additional pull-up resistor.
2) The output current has to be smaller than $I_{L(OL)}$.
3) After maximum t_{INV}.
4) The output current has to be higher than $I_{L(OL)}$.

12.Functions

12.1 Voltage and Current Definition

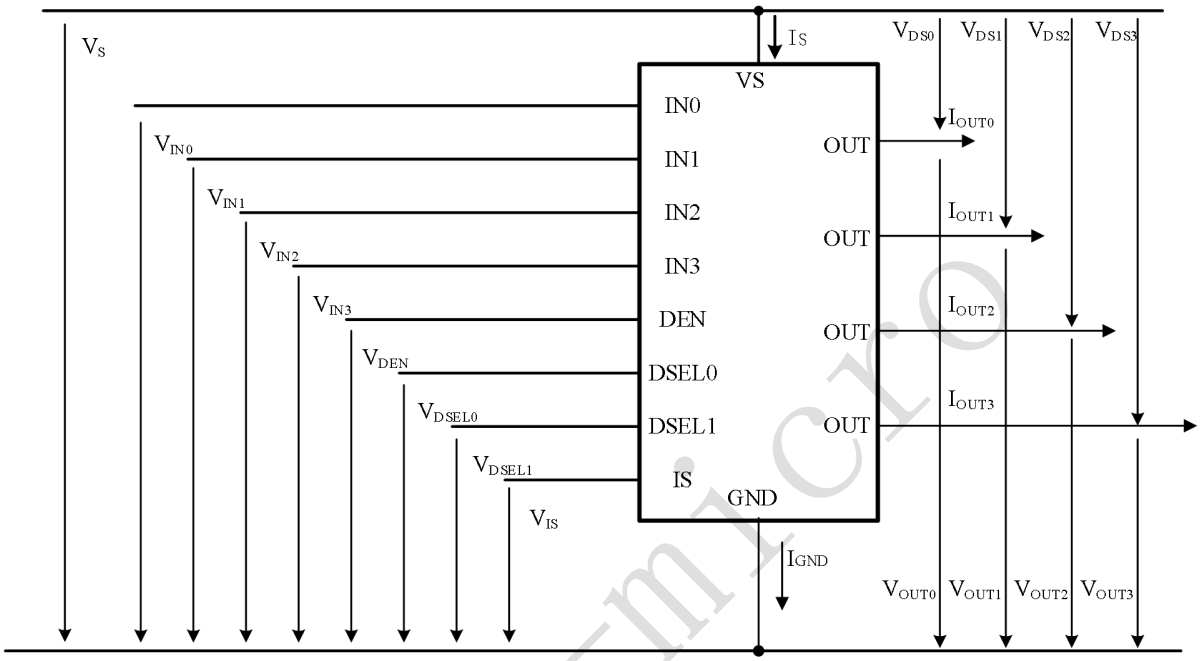
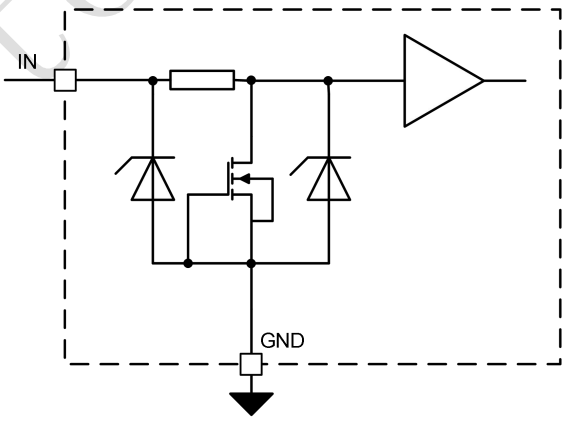


Figure shows all terms used in this data sheet, with associated convention for positive values.

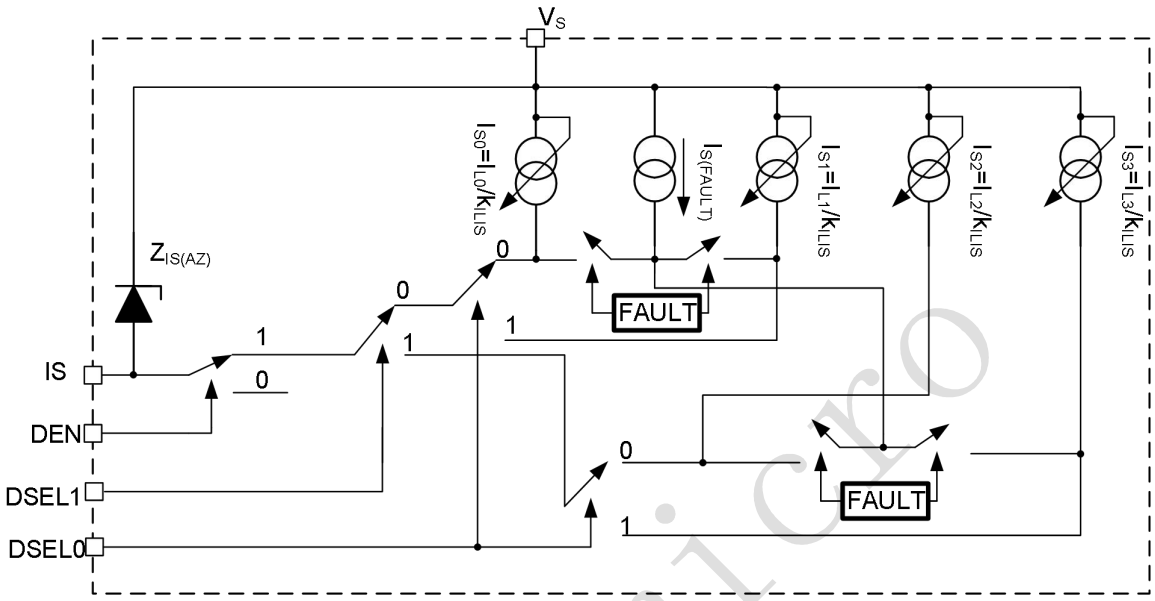
12.2 Input circuit (ESD protection)



The input circuitry is compatible with 3.3 and 5V microcontrollers. The concept of the input pin is to react to voltage thresholds. An implemented Schmitt trigger avoids any undefined state if the voltage on the input pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state.The input circuitry is compatible with PWM applications. Figure shows the electrical equivalent input circuitry. In case the pin is not needed, it must be left opened, or must be connected to device ground (and not module ground) via a 10kΩ input resistor.

The DEN and DSEL0, 1 pins enable and disable the diagnostic functionality of the device. The pins have the same structure as the INput pins.

12.3 Diagnostic Functions

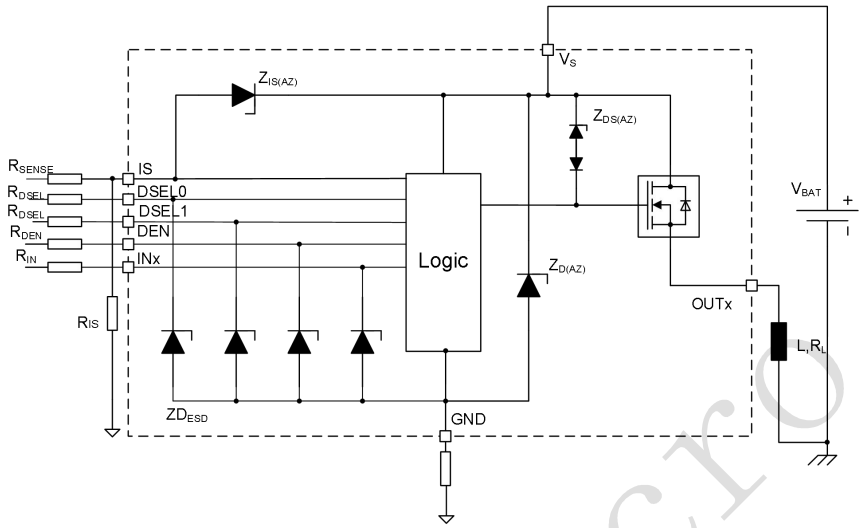


The RM77200DQ provides a sense signal called I_{IS} at pin IS. As long as no "hard" failure mode occurs (short circuit to GND / current limitation / overtemperature / excessive dynamic temperature increase or open load at OFF) a proportional signal to the load current (ratio $k_{ILIS}=I_L / I_{IS}$) is provided. The complete IS pin and diagnostic mechanism is described in Figure. The accuracy of the sense current depends on temperature and load current. The sense pin multiplexes the currents $I_{IS(0)}$, $I_{IS(1)}$, $I_{IS(2)}$ and $I_{IS(3)}$ via the pins DSEL0 and DSEL1. Thanks to this multiplexing, the matching between $k_{ILISCHANNEL0}$, $k_{ILISCHANNEL1}$, $k_{ILISCHANNEL2}$ and $k_{ILISCHANNEL3}$ is optimized. Due to the ESD protection, in connection to V_S, it is not recommended to share the IS pin with other devices if these devices are using another battery feed. The consequence is that the unsupplied device would be fed via the IS pin of the supplied device.

Diagnostic Truth Table

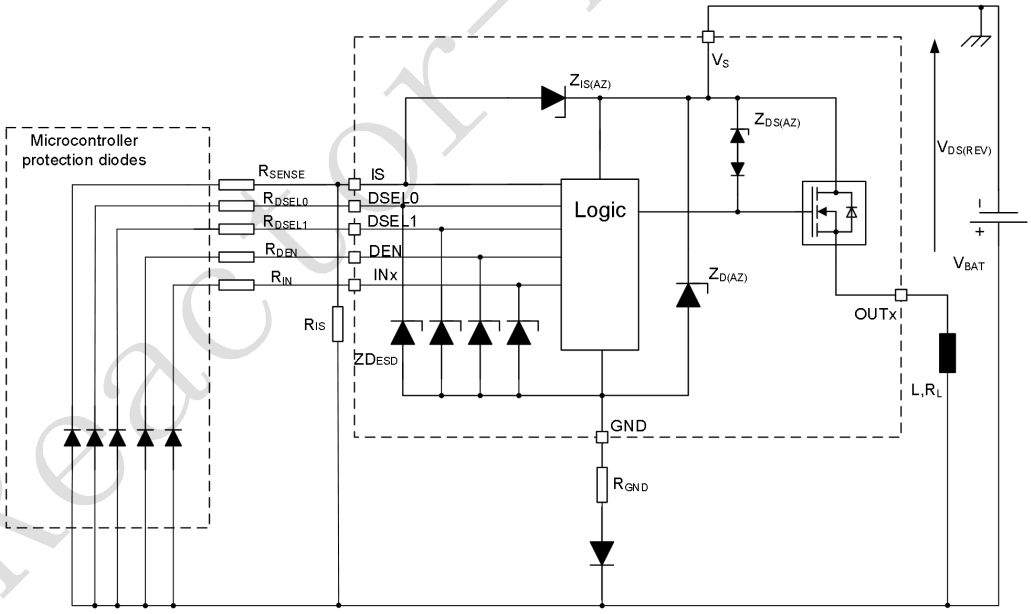
DEN	DSEL1	DSEL0	IS			
0	don't care	don't care	Z	Z	Z	Z
1	0	0	$I_{IS(0)}$	0	0	0
1	0	1	0	$I_{IS(1)}$	0	0
1	1	0	0	0	$I_{IS(2)}$	0
1	1	1	0	0	0	$I_{IS(3)}$

12.4 Overvoltage Protection



There is an integrated clamp mechanism for overvoltage protection ($Z_{D(AZ)}$). To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor.

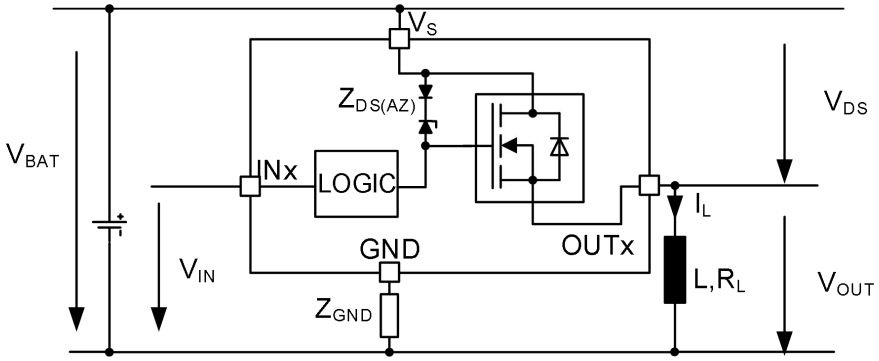
12.5 Reverse Polarity Protection



In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Figure shows a typical application. R_{GND} resistor is used to limit the current in the Zener protection of the device. Resistors R_{DSEL}, R_{DEN}, and R_{IN} are used to limit the current in the logic of the device and in the ESD protection stage. R_{SENSE} is used to limit the current in the sense transistor which behaves as a diode. The recommended value for R_{DEN}=R_{DSEL}=R_{IN}=R_{SENSE}=10kΩ. It is recommended to use a resistor in series to a diode in the ground path.

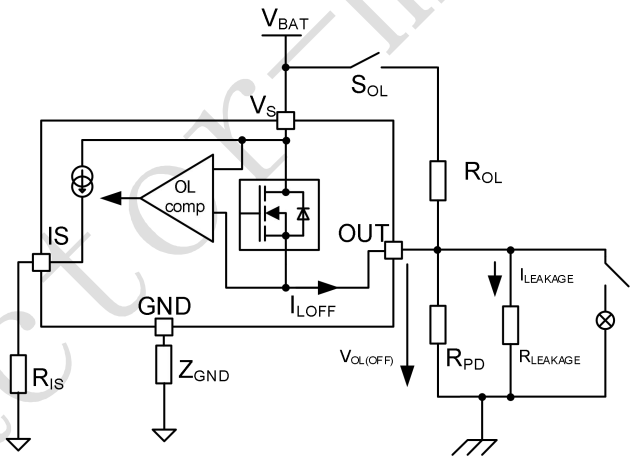
During reverse polarity, no protection functions are available.

12.6 Output Clamping



When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{DS(AZ)}$ implemented that limits negative output voltage to a certain level (V_S-$V_{DS(AZ)}$). Nevertheless, the maximum allowed load inductance is limited.

12.7 Open Load Detection in OFF Electrical Equivalent Circuit



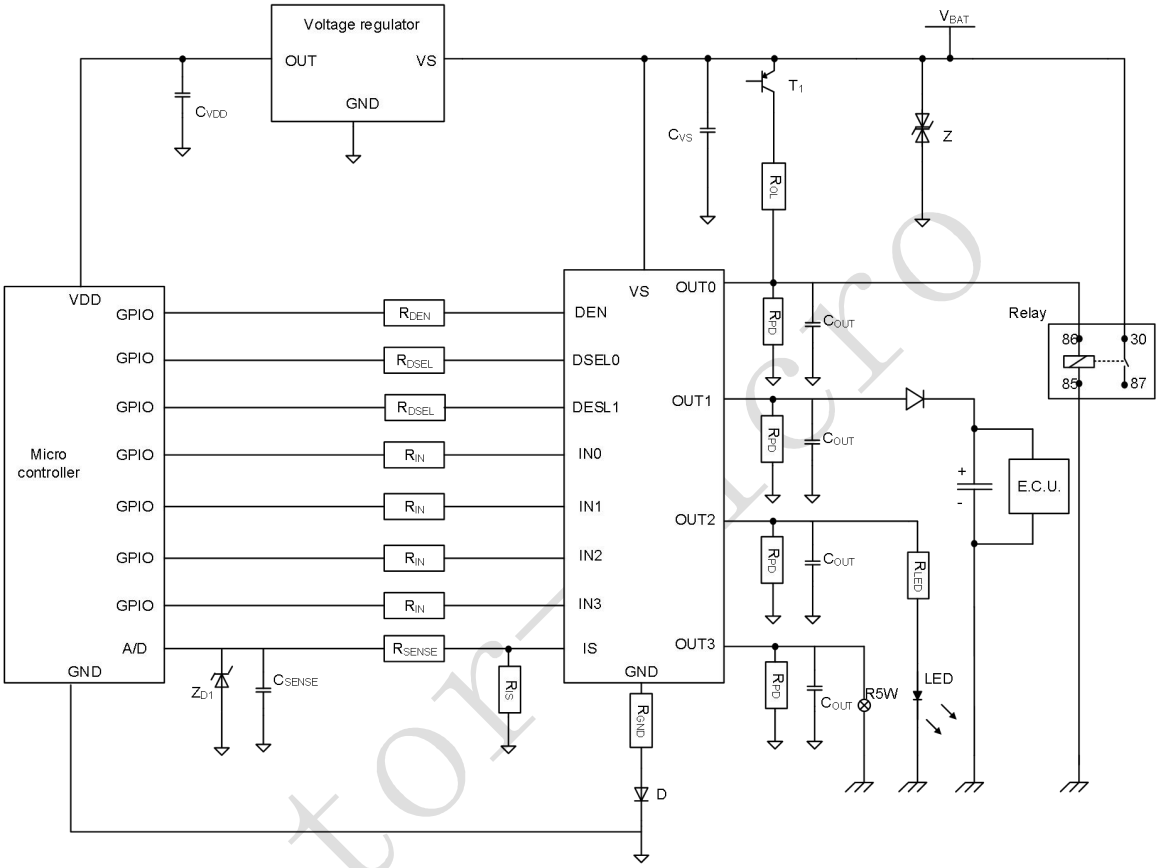
For open load diagnosis in OFF-state, an external output pull-up resistor (R_{OL}) is recommended. For the calculation of pull-up resistor value, the leakage currents and the open load threshold voltage $V_{OL(OFF)}$ have to be taken into account. Figure gives a sketch of the situation. $I_{leakage}$ defines the leakage current in the complete system, including $I_{L(OFF)}$ and external leakages, e.g, due to humidity, corrosion, etc... in the application.

To reduce the stand-by current of the system, an open load resistor switch S_{OL} is recommended. If the channel x is OFF, the output is no longer pulled down by the load and V_{OUT} voltage rises to nearly V_S. This is recognized by the device as an open load. The voltage threshold is given by $V_{OL(OFF)}$. In that case, the SENSE signal is switched to the $I_{IS(FAULT)}$.

An additional R_{PD} resistor can be used to pull V_{OUT} to 0V. Otherwise, the OUT pin is floating. This resistor can be used as well for short circuit to battery detection.

13.Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality,condition or quality of the device.



Note: This is a very simplified example of an application circuit.The function must be verified in the real application.

Bill of Material

Reference	Value	Reference	Value
R_{IN}	10KΩ	T_1	Dual NPN/PNP
R_{DEN}	10KΩ	C_{OUT}	10nF
R_{DSEL}	10KΩ	R_{LED}	680Ω
R_{SENSE}	2KΩ	Z	58V Zener diode
R_{IS} [1)2)]	1KΩ	C_{VS}	100nF
R_{GND}	47Ω	Z_{D1}	6.2V Zener diode
R_{PD}	47KΩ	C_{SENSE}	10nF
R_{OL}	1.5KΩ	D	BAS21

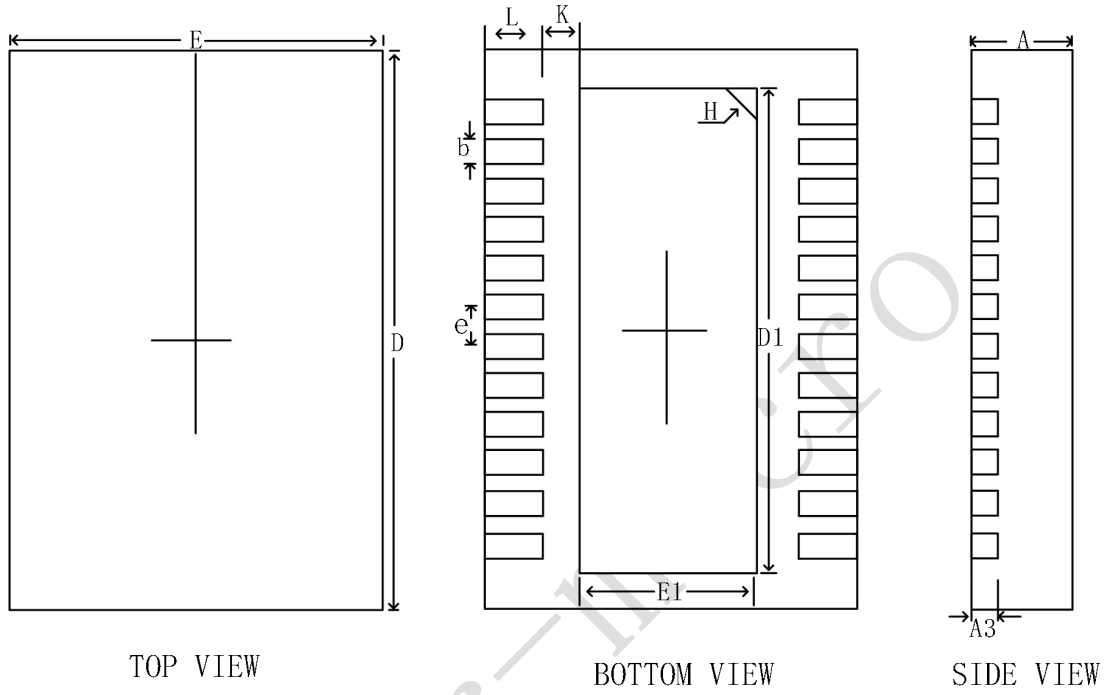
Notes：

1) R_{IS} shall be a 1% tolerance resistor;

2) If reverse polarity protection is not implemented,select R_{IS} in 1206 package.

14.Package

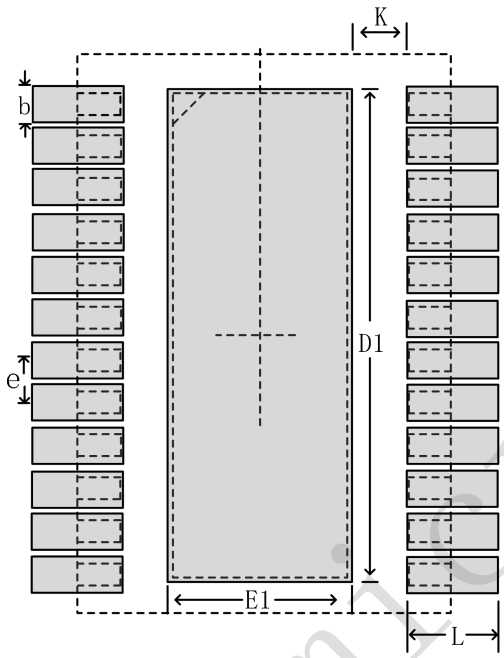
DFN8*6-24L



Unit :mm

Symbol	MIN	NOM	MAX
E	5.90	6.00	6.10
D	8.00	8.50	9.00
E1	2.55	2.65	2.75
D1	6.30	6.40	6.50
K	0.94	1.04	1.14
b	0.15	0.25	0.35
e	-	0.65	-
A	0.90	1.00	1.10
A3	0.154	0.254	0.354
L	0.54	0.64	0.74

15.Recommended Soldering Footprint



Unit : mm

Symbol	NOM	Symbol	NOM
E1	2.8	b	0.25
D1	6..5	e	0.65
K	0.96	L	1

16.Revision History

Version*	Change Description	Date
REV.A	Initial Version	2024/09/06
REV.B	Revised certain parameters in the Electrical Characteristics table.	2024/12/03
REV.C	1) Added certain parameter in the Absolute Maximum Ratings 2) Revised and Added certain parameter in the Electrical Characteristics table. 3) Revised the Package dimensions of section 14.	2025/06/30
NOTE*:Datasheets with alphabetic version numbers (e.g., REV.A, REV.B, REV.C) are designated for the sample phase,whereas those with numeric version numbers (e.g., V1.0, V1.1, V1.2) are intended for the mass production phase.		