

CD4051

CMOS Single 8-Channel Analog Multiplexer or Demultiplexer With Logic-Level Conversion

1. General Description

1.1 Description

The CD4051 series analog multiplexers and demultiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals.

1.2 Features

- Wide range of digital and analog signal levels:
Digital: 3V to 18V
Analog: $\leq 18V_{P-P}$
- Low ON resistance, 80 Ω (Typ) over 15V $_{P-P}$

signal input range for $V_{DD}-V_{EE} = 18V$

- High OFF resistance, channel leakage of $\pm 100pA$ (Typ) at $V_{DD}-V_{EE} = 18V$
- Binary address decoding on chip
- 100% tested for quiescent current at 18V
- 5V, 10V, and 15V parametric ratings
- Break-before-make switching eliminates channel overlap

1.3 Device Information

PART NUMBER	PACKAGE
CD4051	DIP
	SOP
	TSSOP

2. Pin Description and Functional Diagram

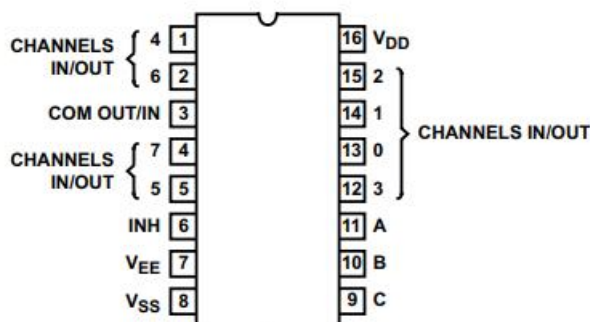


Figure 2.1: Top View

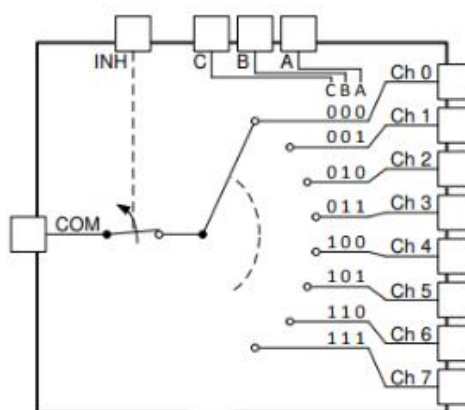
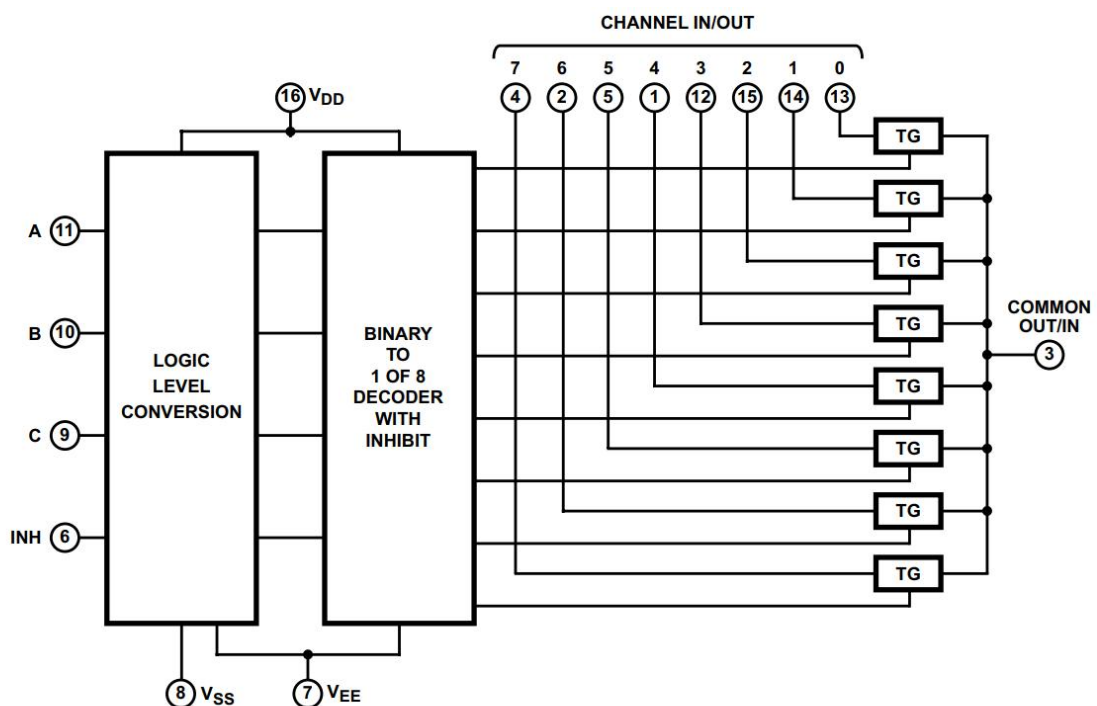


Figure 2.2: Functional Diagram

PIN No.	NAME	I/O	FUNCTION
1	CH 4 IN/OUT	I/O	Channel 4 In/Out
2	CH 6 IN/OUT	I/O	Channel 6 In/Out
3	COM OUT/IN	I/O	Common Out/In
4	CH 5 IN/OUT	I/O	Channel 5 In/Out
5	CH 7 IN/OUT	I/O	Channel 7 In/Out
6	INH	I	Disables All Channels
7	VEE		Negative Power Input
8	VSS		Ground
9	C	I	Channel Select C
10	B	I	Channel Select B
11	A	I	Channel Select B
12	CH 3 IN/OUT	I/O	Channel 3 In/Out
13	CH 0 IN/OUT	I/O	Channel 0 In/Out
14	CH 1 IN/OUT	I/O	Channel 1 In/Out
15	CH 2 IN/OUT	I/O	Channel 2 In/Out
16	VDD		Positive Power Input

3. System Diagram

3.1 Logic Diagram



All inputs are protected by standard CMOS protection network.

Figure 3.1: CD4051 Logic Diagram



3.2 Truth Table

Input State				On Channel(s)
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None

X = don't care, 1≡High State, 0≡Low State

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V_{DD}	DC Supply Voltage Range (Voltage Referenced to VSS Terminals)	-0.5	20	V
V_I	Input Voltage Range, All Inputs	0.5	$V_{DD}+0.5$	V
T_J	Junction Temperature		125	°C
T_{OP}	Operating Temperature	-40	85	°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under normal operating conditions.

4.2 Electrical Characteristics

($T_a=25^{\circ}\text{C}$, $V_{SUPPLY}=\pm 5\text{ V}$, and $R_L=100\ \Omega$, unless otherwise specified)

Symbol	Parameter	Test Condition				MIN	TYP	MAX	Unit
		VIS	VEE	VSS	VDD				
I_{DD}	Supply Current	--	0	0	5	--	0	1	μA
		--	0	0	10	--	0	1	μA
		--	0	0	18	--	0	2	μA
r_{ON}	Drain to Source ON Resistance ($0\leq V_{IS}\leq V_{DD}$)	--	0	0	5	--	200	500	Ω
		--	0	0	10	--	100	300	Ω
		--	0	0	15	--	80	240	Ω
Δr_{ON}	Change in ON Resistance (Between Any Two Channels)	--	0	0	5	--	10	--	Ω
		--	0	0	10	--	10	--	Ω
		--	0	0	15	--	10	--	Ω

Symbol	Parameter	Test Condition				MIN	TYP	MAX	Unit
		VIS	VEE	VSS	VDD				
I_{OFF}	OFF Channel Leakage Current (Any Channel OFF or ALL Channels OFF)	--	0	0	18	--	0	± 2	μA
I_{ON}	ON Channel Leakage Current (Any Channel ON or ALL Channels ON)	5 or 0	-5	0	10.5	--	--	± 2	μA
		5	0	0	18	--	--	± 2	μA
V_{IL}	Low Level Input Voltage	--	--	--	5	--	--	0.8	V
		--	--	--	10	--	--	0.8	V
		--	--	--	15	--	--	0.8	V
V_{IH}	High Level Input Voltage	--	--	--	5	3.5	--	--	V
		--	--	--	10	7	--	--	V
		--	--	--	15	11	--	--	V
I_{IN}	Input Leakage Current	$V_{IN}=0, 18$			18	--	0	± 2	μA

5. Parameter Measurement Information

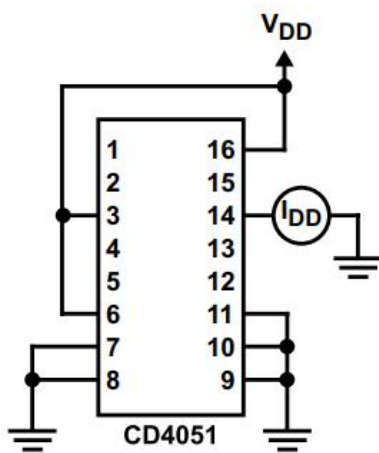


Figure 5.1: OFF Channel Leakage Current – Any Channel OFF

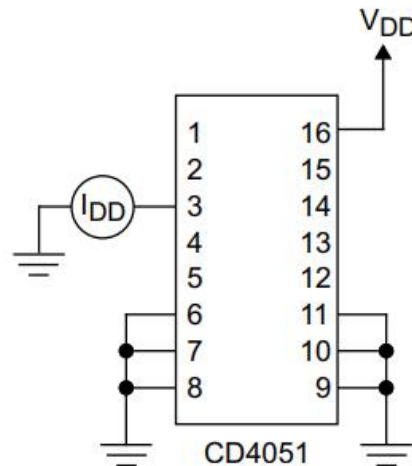


Figure 5.2: ON Channel Leakage Current – Any Channel ON

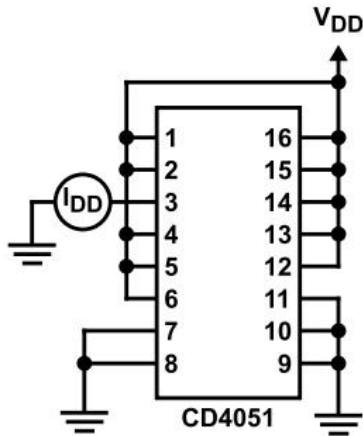


Figure 5.3: OFF Channel Leakage Current

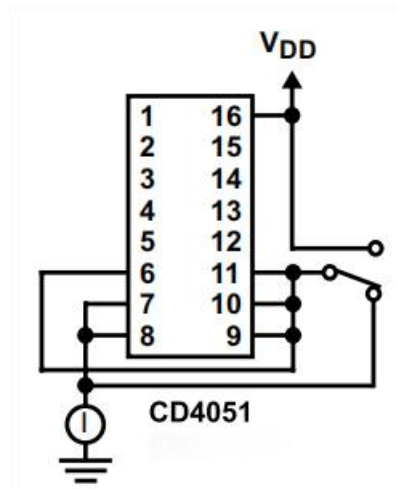


Figure 5.4: Quiescent Device Current

– All Channels OFF

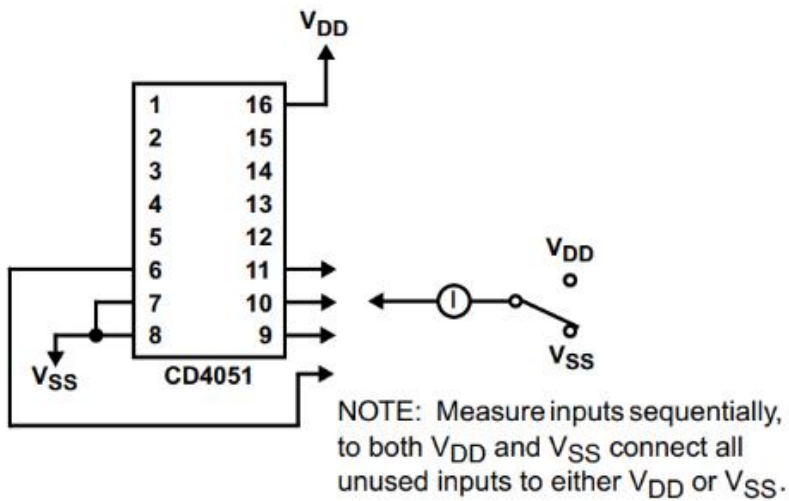


Figure 5.5: Input Current



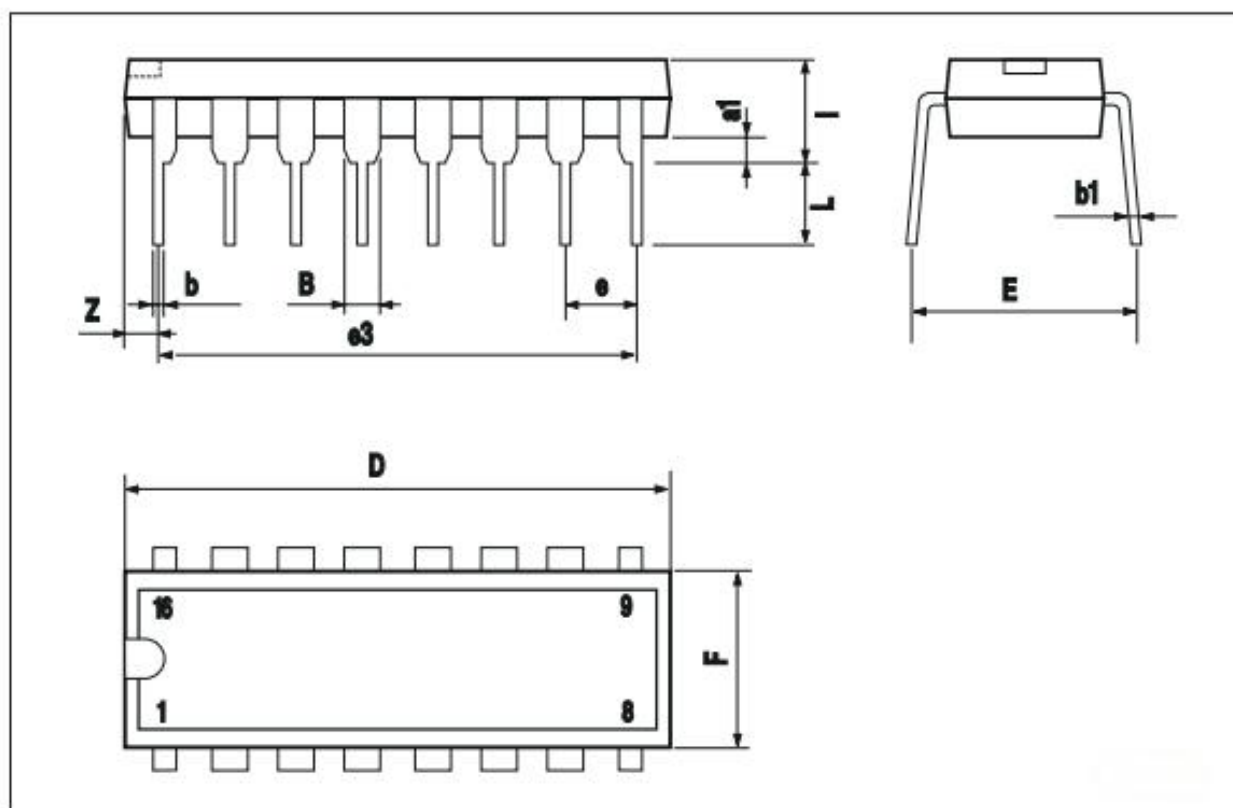
6. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
CD4051ND16ATBE	DIP	16	Tube	25
CD4051NS16ARDQ	SOP	16	Tape & Reel	4000
CD4051TS16ARDQ	TSSOP	16	Tape & Reel	4000

7. Package Information

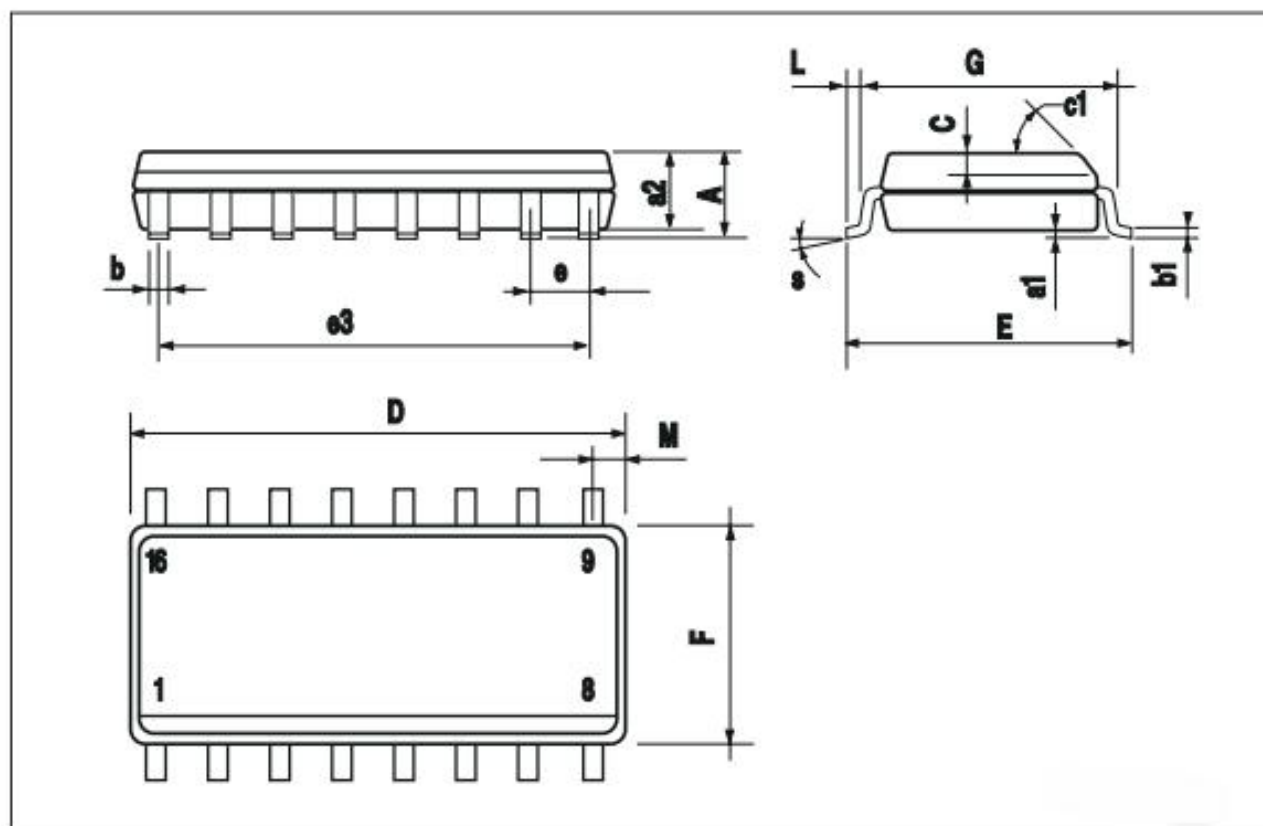
7.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



7.2 SOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



7.3 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

