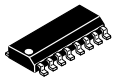
CAN Transceiver, ISO 11992

NCV7390



SOIC−16
CASE 751B−05

Description

The NCV7390 transceiver provides a point−to−point connection for serial data interchange between towing and towed vehicle or other similar automotive applications.

The transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus.

The device provides differential transmit capability but allow switching in error conditions to a single−wire transmitter and/or receiver.

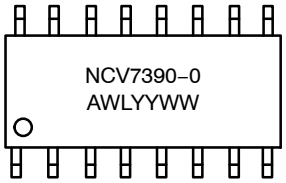
Features

- Designed for Systems According to the International Standard ISO 11992−1
- Suited Both for 12 V and 24 V Battery Systems Applications
- Error Detection Circuit and Capability of Single Wire Operation
- Sleep Mode with Low Current Consumption and Bus wake−up Function
- V_{CC} Pin Allowing Interfacing with 3 V to 5 V Microcontrollers
- Low Electromagnetic Emission (EME) and High Electromagnetic Susceptibility
- Ground Shift Robustness
- Under all Supply Conditions the Chip Behaves Predictably
- Thermal Protection
- AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Automotive, Interface Between Truck and Trailer

MARKING DIAGRAM



A	= Assembly Site
WL	= Wafer Lot Number
YY	= Year of Production
WW	= Work Week Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

TYPICAL APPLICATIONS

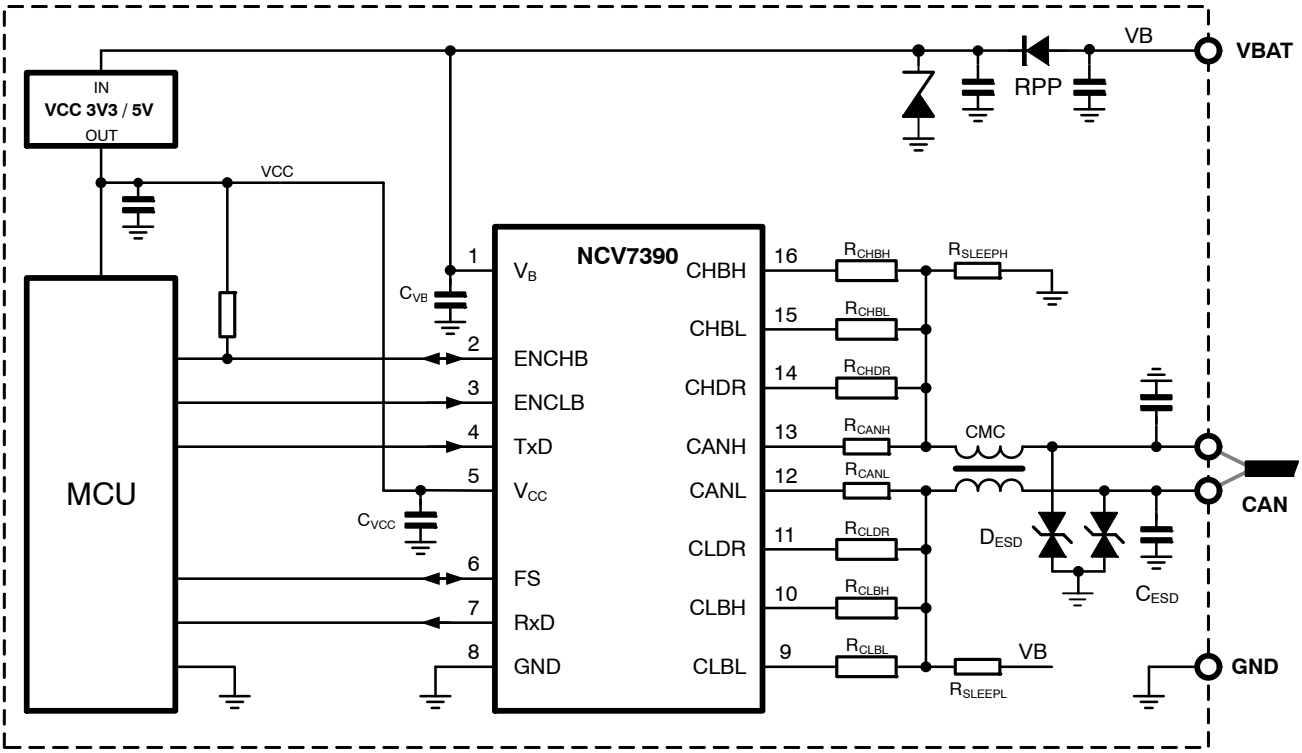


Figure 1. Typical Application Diagram

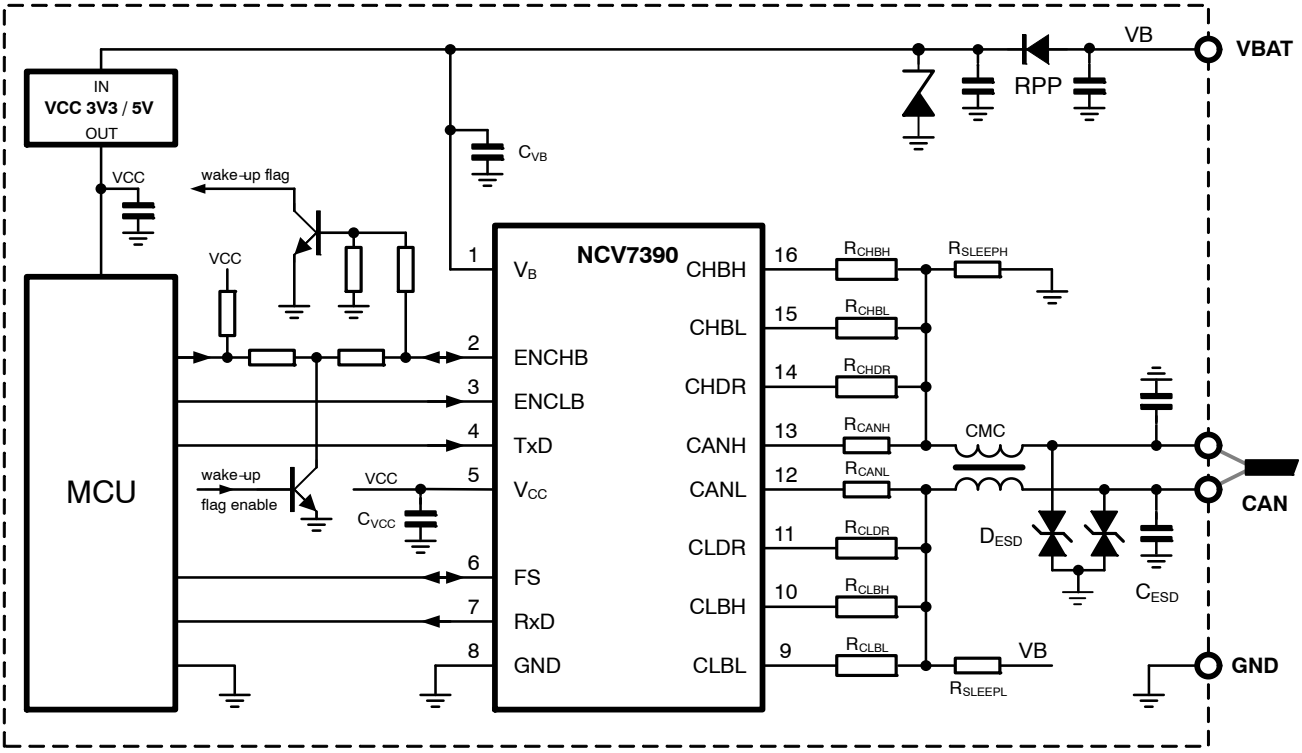


Figure 2. Typical Application Diagram with Sleep / Wake−up Mode

RECOMMENDED EXTERNAL COMPONENTS FOR THE APPLICATION DIAGRAM

Component	Function	Value	Unit	Note
RPP	Diode, Reverse polarity protection			e.g. Vishay RS2JHE3_A/I
C_{VB}	Decoupling capacitor on V_B supply pin, ceramic	100	nF	
C_{VCC}	Decoupling capacitor on V_{CC} supply pin, ceramic	100	nF	Type 0603 or less
D_{ESD}	CAN bus protection element			e.g.: – SZMMBZ33VALT1G – varistor, TDK, B72500E5250L060
C_{ESD}	ESD protection capacitor	220	pF	100 V
CMC	Common mode choke	51	μH	e.g. TDK ACT45B−510−2P−TL003
R_{CANH}	CANH protection resistor	1	kΩ	≤ 1%, ≥ 0.25 W
R_{CANL}	CANL protection resistor	1	kΩ	≤ 1%, ≥ 0.25 W
R_{SLEEPH}	Sleep mode resistor (optional)	22	kΩ	≤ 1%, ≥ 0.25 W
R_{SLEEPL}	Sleep mode resistor (optional)	22	kΩ	≤ 1%, ≥ 0.25 W
24 V SYSTEM				
R_{CHBH}	Resistor, recessive level bias high, CANH	1.62	kΩ	≤ 1%, ≥ 1 W
R_{CHBL}	Resistor, recessive level bias low, CANH	887	Ω	≤ 1%, ≥ 1 W
R_{CHDR}	Resistor, dominant level, CANH	274	Ω	≤ 1%, ≥ 1 W
R_{CLBH}	Resistor, recessive level bias high, CANL	887	Ω	≤ 1%, ≥ 1 W
R_{CLBL}	Resistor, recessive level bias low, CANL	1.91	kΩ	≤ 1%, ≥ 1 W
R_{CLDR}	Resistor, dominant level, CANL	280	Ω	≤ 1%, ≥ 1 W
12 V SYSTEM				
R_{CHBH}	Resistor, recessive level bias high, CANH	1.62	kΩ	≤ 1%, ≥ 1 W
R_{CHBL}	Resistor, recessive level bias low, CANH	887	Ω	≤ 1%, ≥ 1 W
R_{CHDR}	Resistor, dominant level, CANH	221	Ω	≤ 1%, ≥ 1 W
R_{CLBH}	Resistor, recessive level bias high, CANL	887	Ω	≤ 1%, ≥ 1 W
R_{CLBL}	Resistor, recessive level bias low, CANL	2.21	kΩ	≤ 1%, ≥ 1 W
R_{CLDR}	Resistor, dominant level, CANL	274	Ω	≤ 1%, ≥ 1 W

BLOCK DIAGRAM

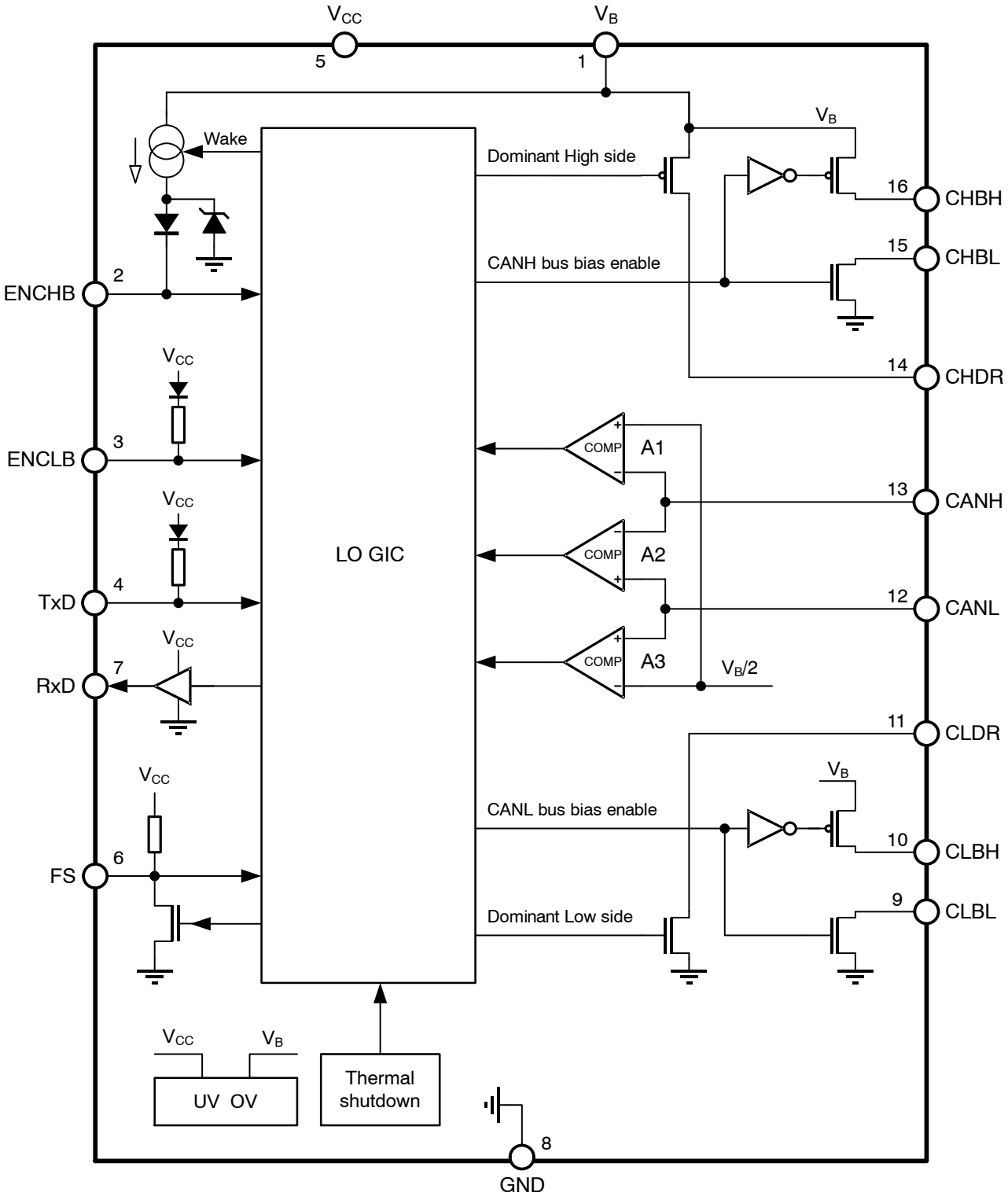


Figure 3. NCV7390 Block Diagram

PIN CONNECTIONS

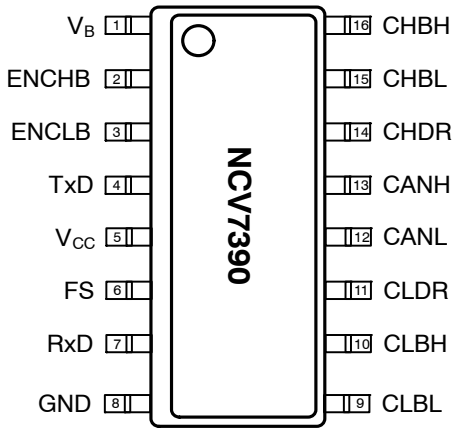


Figure 4. Pin Connections – SOIC−16
(Top View)

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	V_B	Battery supply connection
2	ENCHB	CANH Enable input (active low) / wake−up output
3	ENCLB	CANL Enable input (active low)
4	TxD	Transmit data input
5	V_{CC}	Logic supply voltage
6	FS	Fault state input/output
7	RxD	Receive data output
8	GND	Ground
9	CLBL	CANL Bias voltage Low
10	CLBH	CANL Bias voltage High
11	CLDR	CANL Driver
12	CANL	CANL receiver input
13	CANH	CANH receiver input
14	CHDR	CANH Driver
15	CHBL	CANH Bias voltage Low
16	CHBH	CANH Bias voltage High

MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_B	Supply Voltage, pin V_B	(Note 1)	−0.3	+65	V
V_{CC}	Supply Voltage, pin V_{CC}	(Note 1)	−0.3	+6.0	V
V_{CAN}	DC Voltage at Pins CANH, CANL, CLBL, CLBH, CLDR, CHDR, CHBL, CHBH	$0 < V_{CC} < 5.5$ V	−0.3	V_B + 0.3	V
V_{DIG_IN}	DC Voltage at Pin ENCHB		−0.3	+65	V
V_{DIG_IN}	DC Voltage at Pin TxD, ENCLB		−0.3	+6.0	V
V_{DIG_OUT}	DC Voltage at Pin RxD		−0.3	V_{CC} + 0.3	V

MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DIG_OUT}	DC Voltage at Pin FS		−0.3	+6	V
I_{OP1A}	Peak Output Current CHBH, CLBL (Bus Short)	Duration of 2 ms	–	41	mA
I_{OP2A}	Peak Output Current CHBL, CLBH (Bus Short)	Duration of 2 ms	–	77	mA
I_{OP3A}	Peak Output Current CHDR, CLDR (Bus Short)	Duration of 2 ms	–	228	mA
I_{OP1}	Peak Output Current CHBH, CLBL	Duration of 1 sec	–	28	mA
I_{OP2}	Peak Output Current CHBL, CLBH	Duration of 1 sec	–	54	mA
I_{OP3}	Peak Output Current CHDR, CLDR	Duration of 1 sec	–	82	mA
V_{ESD_IEC}	Electrostatic Discharge Voltage at CAN Bus Pins and V_B Pin, Test Circuit as shown in Figure 10 System HBM, Direct Contact	(Note 2)	−16	+16	kV
V_{ESD_HBM}	Electrostatic Discharge Voltage at all Pins; Component HBM	(Note 3)	−2	+2	kV
V_{ESD_CDM}	Electrostatic Discharge Voltage at all Pins; Component CDM	(Note 4)	−250	+250	V
V_{TRAN}	Voltage Transients, CAN Bus Pins Test Pulses According to ISO7637−2, Class C Test Circuit as shown in Figure 10	test pulses 1	−200	–	V
		test pulses 2a	–	+300	
		test pulses 3a	−200	–	
		test pulses 3b	–	+200	
	Voltage Transients, pin V_B, According to ISO7637−2, Class C Maximum voltage seen on IC V_B Pin clamped by external element. Test Circuit as shown in Figure 10	Test pulse 5 Load dump	–	65	
Latch−up	Static Latch−up at all Pins	(Note 5)	–	150	mA
T_J	Maximum Junction temperature		−40	+150	°C
T_A	Maximum Ambient temperature		−40	+125	°C
T_{STG}	Storage Temperature		−55	+150	°C
MSL	Moisture Sensitivity Level		2		–
T_{SLD}	Peak Soldering Temperature (Note 6)		–	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. System human body model electrostatic discharge (ESD) pulses in accordance with IEC 61000−4−2. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND. External components according to the table: Recommended External Components for the Application Diagram.
3. Standardized human body model electrostatic discharge (ESD) pulses in accordance with EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
4. Standardized charged device model ESD pulses when tested according to AEC−Q100−011.
5. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78.
6. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC 16 small − 150 mil (Note 7) Thermal Resistance Junction−to−Air (Note 8) Thermal Resistance Junction−to−Air (Note 9)	 $R_{\theta JA\_1}$ $R_{\theta JA\_2}$	 170 96	K/W

7. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
8. Test board according to EIA/JEDEC Standard JESD51−3 (1S0P PCB), signal layer with 10% trace coverage.
9. Test board according to EIA/JEDEC Standard JESD51−7 (2S2P PCB), signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V to 5.5 V; V_B = 7.0 V to 32 V; for typical values T_A = 25°C, for min/max values T_J = −40°C to +150°C, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 8). Positive currents flow into the respective pin)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} SUPPLY INPUT (Pin V_{CC})						
V_{CC}	Supply Voltage (input condition)		3.0	–	5.5	V
I_{CC}	Supply Current, all modes	$V_{TxD} = V_{ENCLB} = V_{ENCHB} = V_{CC}$ FS High	–	–	10	μA
		$V_{TxD} = V_{ENCLB} = V_{ENCHB}$ = 0 V FS Low	–	–	2	mA
I_{CC_peak}	AC Peak Current during start−up	0 V < V_{CC} < 3.0 V Not tested in production	–	–	20	mA
V_{CC_slope}	Slew rate for V_{CC} power off	Prepare for Sleep mode	–	–	2.0	V/ms
V_{CC_UVR}	Undervoltage Recovery Threshold	V_{CC} rising	2.0	–	2.9	V
V_{CC_UVD}	Undervoltage Detection Threshold	V_{CC} falling	1.9	–	2.6	V
V_{CC_UVH}	Undervoltage Threshold Hysteresis		250	–	400	mV
ΔV_{CCUV_ENCLB}	Difference: V_{CC_UVD} − V_{IH_ENCLB}		100	–	–	mV
V_B SUPPLY INPUT (Pin V_B)						
V_B	Supply Voltage on Pin V_B (input condition)		7.0	–	32	V
V_{B_PORH}	V_B Power−on Threshold	V_B rising	–	4.5	4.9	V
V_{B_PORL}	V_B Power−off Threshold	V_B falling	4.0	4.4	–	V
$V_{th\_OFF\_CLDR}$	CLDR pin switch off V_B Threshold		–	38	41	V
I_B	Active Mode Supply Current	Without bias network current and dominant driver current (CxDR, CxBH, CxBL open) $V_{ENCHB} = V_{ENCLB}$ = 0 V, $V_{TxD} = V_{CC}$ I_{OH_ENCHB} not activated	–	1.5	6.4	mA
I_{B_LP}	Low−power Mode Supply Current	Standby Mode V_B = 7 V to 24 V	–	15	50	μA
		Sleep Mode V_B = 7 V to 24 V I_{OH_ENCHB} not activated	–	30	80	μA
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH_TxD}	High−level input voltage	Output recessive	2.0	–	–	V
V_{IL_TxD}	Low−level input voltage	Output dominant	–	–	0.8	V
I_{PU_TxD}	Pull−up current	V_{TxD} = GND	−550	–	−100	μA
I_{LEAK_TxD}	Leakage current	$V_{TxD} = V_{CC}$	−1.0	0	+1.0	μA
C_i	Input capacitance	(Note 10)	–	5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH_RxD}	High−level output current	$V_{RxD} = V_{CC}$ − 0.4 V	–	–	−2.0	mA
I_{OL_RxD}	Low−level output current	V_{RxD} = 0.4 V	4.0	–	–	mA
TRANSMITTER MODE SELECT (Pin ENCLB)						
V_{IH_ENCLB}	High−level input voltage		2.0	–	–	V
V_{IL_ENCLB}	Low−level input voltage		–	–	0.8	V
I_{PU_ENCLB}	Pull−up current	V_{ENCLB} = GND	−550	–	−100	μA
I_{LEAK_ENCLB}	Leakage current	$V_{ENCLB} = V_{CC}$	−1.0	0	+1.0	μA
C_i	Input capacitance	(Note 10)	–	5	10	pF

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V to 5.5 V; V_B = 7.0 V to 32 V; for typical values T_A = 25°C, for min/max values T_J = −40°C to +150°C, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 8). Positive currents flow into the respective pin)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TRANSMITTER MODE SELECT, bus wake−up signaling (Pin ENCHB)						
V_{IH_ENCHB}	High−level input voltage		2.0	−	−	V
V_{IL_ENCHB}	Low−level input voltage		−	−	0.8	V
I_{OH_ENCHB}	Pull−up current, bus wake−up signaling	0 V < V_{ENCHB} < 3.0 V; wake−up detected	−5.0	−	−0.5	mA
V_{ENCHB_OUT}	Maximum voltage output if bus wake−up signaling activated	wake−up detected, no load current	3.675	−	5.25	V
I_{LEAK_ENCHB}	Leakage current	V_{ENCHB} = V_{CC}	−1.0	0	+1.0	μA
$I_{LEAK\_ENCHB\_GND}$	Weak pull−up current to internal IO cell supply	V_{ENCHB} = GND	−10.0	−1.5	−0.4	μA
C_i	Input capacitance	(Note 10)	−	5	10	pF
FS INPUT / OUTPUT						
V_{IH_FS}	High−level input voltage		2.0	−	−	V
V_{IL_FS}	Low−level input voltage		−	−	0.8	V
I_{LEAK_FS}	Leakage current	V_{FS} = V_{CC}	−1.0	0	+1.0	μA
I_{RPU_FS}	Pull−up current	V_{FS} = GND, V_{CC} = 5.0 V	−400	−250	−85	μA
V_{OL_FS}	Low−level output voltage	I_{FS} = 5.0 mA	−	−	0.5	V
C_i	Input capacitance	(Note 10)	−	5	10	pF
BUS BIAS PIN (Pin CHBH)						
V_{OH_CHBH}	High−level output voltage	I_{CHBH} = −20 mA, V_B = 32 V, or I_{CHBH} = −4.5 mA, V_B = 7.0 V	V_B − 0.9	−	−	V
I_{LEAK_CHBH}	Leakage current	ENCHB = High, V_{CHBH} = 0 V	−2.0	0	+2.0	μA
BUS BIAS PIN (Pin CLBH)						
V_{OH_CLBH}	High−level output voltage	I_{CLBH} = −40 mA, V_B = 32 V, or I_{CLBH} = −9 mA, V_B = 7.0 V	V_B − 1.0	−	−	V
I_{LEAK_CLBH}	Leakage current	ENCLB = High, V_{CLBH} = 0 V	−2.0	0	+2.0	μA
BUS BIAS PIN (Pin CHBL)						
V_{OL_CHBL}	Low−level output voltage	I_{CHBL} = 40 mA, V_B = 32 V, or I_{CHBL} = 9 mA, V_B = 7.0 V	−	−	400	mV
I_{LEAK_CHBL}	Leakage current	ENCHB = High, V_{CHBL} = V_B	−2.0	0	+2.0	μA
BUS BIAS PIN (Pin CLBL)						
V_{OL_CLBL}	Low−level output voltage	I_{CLBL} = 20 mA, V_B = 32 V, or I_{CLBL} = 4.5 mA, V_B = 7.0 V	−	−	400	mV
I_{LEAK_CLBL}	Leakage current	ENCLB = High, V_{CLBL} = V_B	−2.0	0	+2.0	μA
CAN HIGH SIDE DRIVE (Pin CHDR)						
R_{ON_CHDR}	Driver output resistance	I_{CHDR} = −40 mA	2.0	−	25	Ω
V_{OH_CHDR}	High level output voltage	V_B = 32 V, I_{CHDR} = −115 mA, or V_B = 7.0 V, I_{CHDR} = −26 mA, ENCHB = Low, TxD = Low	V_B − 2.0	−	−	V
I_{LEAK_CHDR}	Leakage current	ENCHB = High, V_{CHDR} = 0 V	−2.0	0	+2.0	μA
CAN LOW SIDE DRIVE (Pin CLDR)						
R_{ON_CLDR}	Driver output resistance	I_{CLDR} = 40 mA	2.0	−	25	Ω

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V to 5.5 V; V_B = 7.0 V to 32 V; for typical values T_A = 25°C, for min/max values T_J = −40°C to +150°C, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 8). Positive currents flow into the respective pin)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN LOW SIDE DRIVE (Pin CLDR)						
V_{OL_CLDR}	High level output voltage	V_B = 32 V, I_{CLDR} = 115 mA, or V_B = 7.0 V, I_{CHDR} = 26 mA, ENCLB = Low, TxD = Low	–	–	2.0	V
I_{LEAK_CLDR}	Leakage current	ENCLB = High, V_{CLDR} = V_B	−2.0	0	+2.0	μA
CAN RECEIVER (Pins CANH and CANL)						
$I_{LEAK(off)}$	Input leakage current	0 < (V_{CANH} = V_{CANL}) < 32 V	−5.0	0	+5.0	μA
$V_{i(th)(diff)\_dom\_A2}$	Differential receiver threshold voltage Voltage (V_{CANL} – V_{CANH}), Comparator A2	Dominant state 2.25 V ≤ V_{CANH}, V_{CANL} ≤ V_B – 2.9 V	−0.65	–	0	V
$V_{i(th)(diff)\_rec\_A2}$	Differential receiver threshold voltage Voltage (V_{CANL} – V_{CANH}), Comparator A2	Recessive state 2.25 V ≤ V_{CANH}, V_{CANL} ≤ V_B – 2.9 V ENCHB, ENCLB = Low	0	–	0.65	V
$V_{i(th)(se)\_A1}$	Receiver threshold voltage Voltage V_{CANH}, Comparator A1	ENCHB = Low, ENCLB = High	0.48	–	0.52	V_B
$V_{i(th)(se)\_A3}$	Receiver threshold voltage Voltage V_{CANL}, Comparator A3	ENCHB = High, ENCLB = Low	0.48	–	0.52	V_B
$V_{i(th)\_A1\_sleep}$	Receiver threshold voltage Comparator A1 in Prepare for sleep and Sleep mode	ENCHB = High, ENCLB = High, TxD = Low	0.43	–	0.47	V_B
$V_{i(th)\_A3\_sleep}$	Receiver threshold voltage Comparator A3 in Prepare for sleep and Sleep mode	ENCHB = High, ENCLB = High, TxD = Low	0.49	–	0.53	V_B
THERMAL SHUTDOWN						
T_{JSD}	Shutdown junction temperature	Junction temperature rising	160	180	200	°C
T_{JSD_HYST}	Shutdown junction temperature hysteresis		–	10	–	°C
TIMING CHARACTERISTICS (see and Figure 6)						
t_{bit125}	Bit time (input condition)	125 kbps	7.9992	8.0	8.0008	μs
t_{bit250}	Bit time (input condition)	250 kbps	3.9996	4.0	4.0004	μs
t_{dri}	Driving delay time	Active mode	–	100	–	ns
t_{rec}	Receiving delay time	Active mode	–	100	–	ns
$t_{del\_r\_d}$	Propagation delay TxD to RxD recessive to dominant transition	Active mode ENCHB = Low, ENCLB = Low t_{del} = t_{dri} + t_{rec} For setup see Figure 9	–	–	350	ns
$t_{del\_d\_r\_amb}$	Propagation delay TxD to RxD dominant to recessive transition	Active mode, 8.0 < V_B < 32 V, T_{AMB} = 25°C ENCHB = Low, ENCLB = Low t_{del} = t_{dri} + t_{rec} For setup see Figure 9 (Note 10)	–	–	400	ns
$t_{del\_d\_r}$	Propagation delay TxD to RxD dominant to recessive transition	Active mode, 8.0 < V_B < 32 V, ENCHB = Low, ENCLB = Low t_{del} = t_{dri} + t_{rec} For setup see Figure 9	–	–	420	ns

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V to 5.5 V; V_B = 7.0 V to 32 V; for typical values T_A = 25°C, for min/max values T_J = −40°C to +150°C, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 8). Positive currents flow into the respective pin)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TIMING CHARACTERISTICS (see and Figure 6)						
$t_{del\_r\_d\_sw}$	Propagation delay TxD to RxD recessive to dominant transition	Active mode, 8.0 < V_B < 32 V, Either ENCLB or ENCHB are High (single wire communication), $t_{del} = t_{dri} + t_{rec}$ For setup see Figure 9	–	–	350	ns
$t_{del\_d\_r\_sw}$	Propagation delay TxD to RxD dominant to recessive transition	Active mode, 8.0 < V_B < 32 V, Either ENCLB or ENCHB are High (single wire communication), $t_{del} = t_{dri} + t_{rec}$ For setup see Figure 9	–	–	500	ns
t_{EN}	Enable / Disable time, ENCLB and ENCHB pins		–	–	4.5	μs
t_{rf}	Rise / Fall time, CAN bus	For setup see Figure 9	–	–	250	ns
t_{err_det}	Bus error detection filter time		–	–	3.5	μs
t_{FS_res}	Delay time for FS reset	(Note 10)	–	–	1.0	μs
$t_{Wake\_width\_L}$	CANL wake−up filter time	Sleep mode, V_{CANL} < 1/3 V_B	1.5	–	7.5	μs
$t_{Wake\_width\_H}$	CANH wake−up filter time	Sleep mode, V_{CANH} > 2/3 V_B	1.5	–	7.5	μs
SYSTEM CHARACTERISTICS						
V_{off_GND}	Ground offset between the two interfaces during two wire operation		−1/8	–	+1/8	V_B

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Values based on design and characterization, not tested in production.

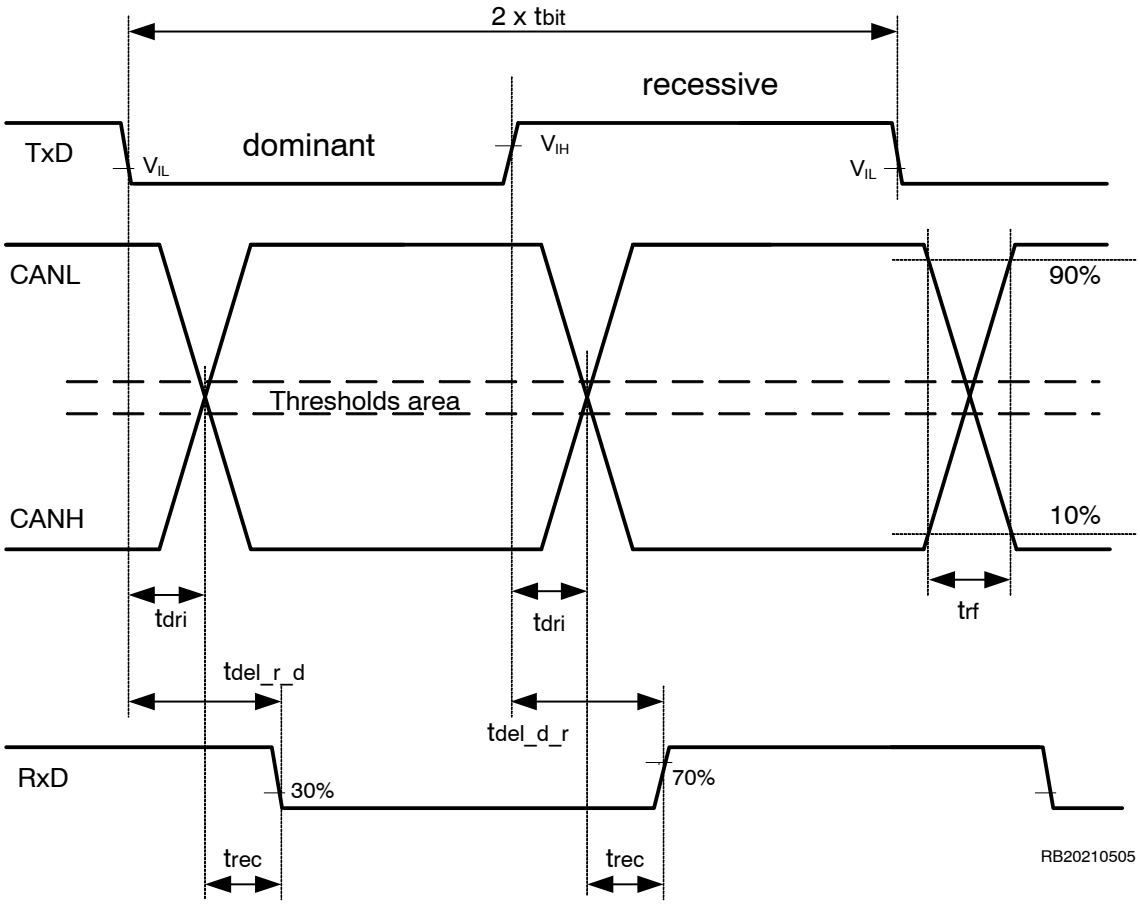


Figure 5. Transceiver Timing Diagram – Propagation Delays

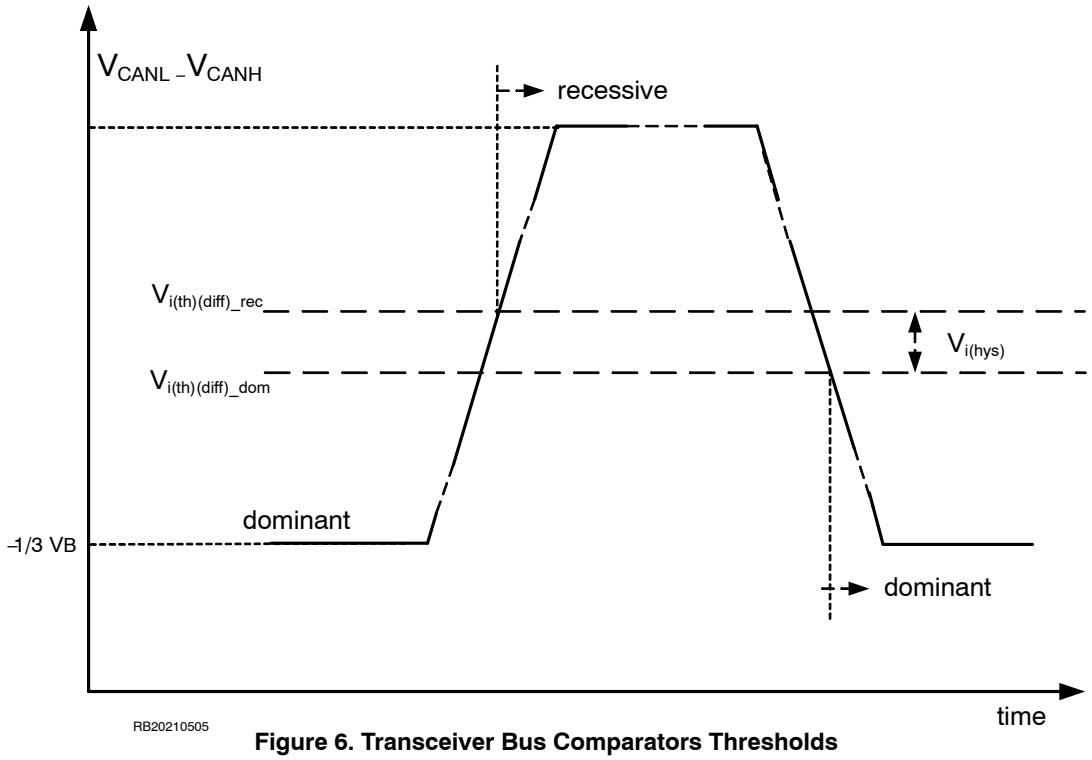


Figure 6. Transceiver Bus Comparators Thresholds

FUNCTIONAL DESCRIPTION

GENERAL FUNCTION

There are two logical states for bus line, dominant or recessive. The bus is in the recessive state, when the driving sections of both transceivers connected to the bus are passive. (TxD is high)

The recessive state is specified by a voltage levels of typ. 1/3 V_B at CANH and typ. 2/3 V_B at CANL.

If at least one driver became active the bus changes into the dominant state. The dominant state is specified by a voltage levels of typ. 2/3 V_B at CANH and typ. 1/3 V_B at CANL. So, the differential voltage (Voltage at pin CANL minus voltage at pin CANH) change from typ. +1/3 V_B in the recessive state to typ. −1/3 V_B in the dominant state (See Figure 6).

The transceiver includes a bus driving section with biasing (CHBH, CLBH, CHBL, CLBL) and driver outputs (CHDR, CLDR) for CANH and CANL. The biasing outputs for the recessive state will be active if the corresponding enable (ENCHB, ENCLB) input is set to a low state.

To change to the dominant state, it is only necessary to activate the driver output by a low level at the input TxD.

The biasing and driver outputs are implemented as open drain push (CHDR, CHBH, CLBH) and pull (CLDR CHBL, CLBL) driver, with a matched (but opposite) slew rate at CHDR and CLDR.

The bus receiving section consists of an integrated RF−Filter followed by three comparators (A1..3). The comparators sense the state of the bus lines CANH and CANL. The reception of a dominant state causes a low level at RxD.

POWER SUPPLY

NCV7390 implements two power supply inputs – battery supply input V_B and logic supply input V_{CC}.

V_B Supply pin

V_B is the main supply pin of the NCV7390. This supply input is used to provide the minimum power required for the operation in case of absence of the V_{CC} supply. Typically, this is the only active supply in a low−power Sleep mode providing power supply to the low−power wake−up detector.

The digital part is supplied by an internal voltage supply derived from V_B.

V_{CC} Supply pin

V_{CC} pin provides supply for the logical interface of NCV7390. In case of missing V_{CC} the bus drivers of the NCV7390 are disabled until $V_{CC} > V_{CC\_UVR}$. After $V_{CC} > V_{CC\_UVR}$ the CANH and CANL driver blocks can be activated by a low level with their corresponding ENCHB and ENCLB pins.

OPERATION MODES

NCV7390 provides different operation modes. These modes are entered according to Figure 7.

Power−off

This virtual mode is entered when the V_B supply voltage falls below V_{B_PORL} level. The internal logic is reset. CAN bus pins are left floating. As soon as V_B voltage rises above V_{B_PORH} level, a power−on event is detected and the device proceeds to Standby mode. Bus receiver is in power down state.

Standby Mode

The NCV7390 proceeds from Power−off mode to Standby mode as soon as the V_B supply is available ($V_B > V_{B\_PORH}$)

If $V_{CC} < V_{CC\_UVD}$ and Prepare−for−sleep−mode is not active the circuit is in Standby mode with minimized current consumption.

Bus error detection counter is reset. Bus pins drivers and biases are off. Bus receiver is in power down state. FS pin is always Low in Standby mode.

Active Mode

In the Active mode (see truth Table in Figure 7), the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD.

The FS output is permanently reset (FS pin is set Low) if ENCHB or ENCLB pin is set High.

Wake−up flag is reset and the I_{OH_ENCHB} current is deactivated upon detecting High to Low level transition on ENCLB pin.

Based on status of pins ENCHB, ENCLB and TxD the active mode has four possible sub modes:

- Two−wire mode
- One−wire mode CANH
- One−wire mode CANL
- Passive sub mode

Two−wire Mode

All bus bias and driver pins are activated.

The differential signal from bus is detected by comparator A2 (see Figure 3) and signaled on RxD pin.

The Bus failure detection is active in this sub mode only.

One−wire Modes

The One−wire modes are failure modes to avoid total breakdown of the data transmission in case of a single bus failure.

To switch over from Two−wire mode to One−wire mode, it is necessary to disable the CANH or CANL line by a high state at the corresponding enable input. By this the corresponding biasing and driver outputs are disabled. In case of One−wire operation on CANH or CANL comparators, A1/A3 compares the voltage level on CANH/CANL pin with an internal reference voltage. Dominant state is signaled if there is voltage below

$V_{i(th)(se)\_A3}$ on CANL pin or voltage level above $V_{i(th)(se)\_A1}$ on CANH pin.

Passive Mode

All bus bias and driver pins are deactivated (High impedance state).

The output RxD is forced to High level by the internal logic.

Prepare for Sleep Mode

Prepare−for−sleep mode is an intermediate state used to put the transceiver into Sleep mode in a controlled way.

Prepare−for−sleep mode is entered from Active mode when ENCHB and ENCHL are set to High and TxD pin is set to Low. This condition will be latched and acknowledged by a high level at FS pin.

Based on status of pins ENCHB, ENCLB and TxD the active mode has three possible sub modes: One−wire mode CANH, Test mode and Passive sub mode.

One−wire Mode CANH:

This mode is identical to one wire mode CANH in Active mode.

Test Mode:

In this mode the RxD pin is signaling result of this logical function of A1 and A3 comparators: NOT (A1 & A3).

Passive Mode:

The output RxD is forced to a high level by the internal logic.

If V_{CC} falls below V_{CC_UVD} level and Prepare for Sleep mode is active, the device proceeds to Sleep mode. For this function, a slew rate of max. V_{CC_slope} at V_{CC} is allowed.

Sleep Mode

Sleep mode is a low−power mode in which the consumption is kept minimal.

The bias and driver outputs are in an off state. The voltage level at FS follows V_{CC} because of the internal pull−up resistor.

Bus wake−up detection is enabled in Sleep mode. A wake−up flag is set when 16 dominant symbols longer that $t_{wake\_width\_H/L}$ are detected by A1 comparator (CANH), or A3 comparator (CANL), or their combination. Short dominant glitches, caused by potential noise, are discarded.

Similarly, permanent bus dominant state caused by potential but short to GND or battery voltage does not lead to bus wake−up event detection.

No wake−up detection timeout is implemented.

ENCHB is pulled up to V_B level by a current source I_{OH_ENCHB} when the wake−up flag is set.

While in Sleep mode and if V_{CC} supply rises above V_{CC_UVR} level the device will transition directly to Active mode (see Figure 7).

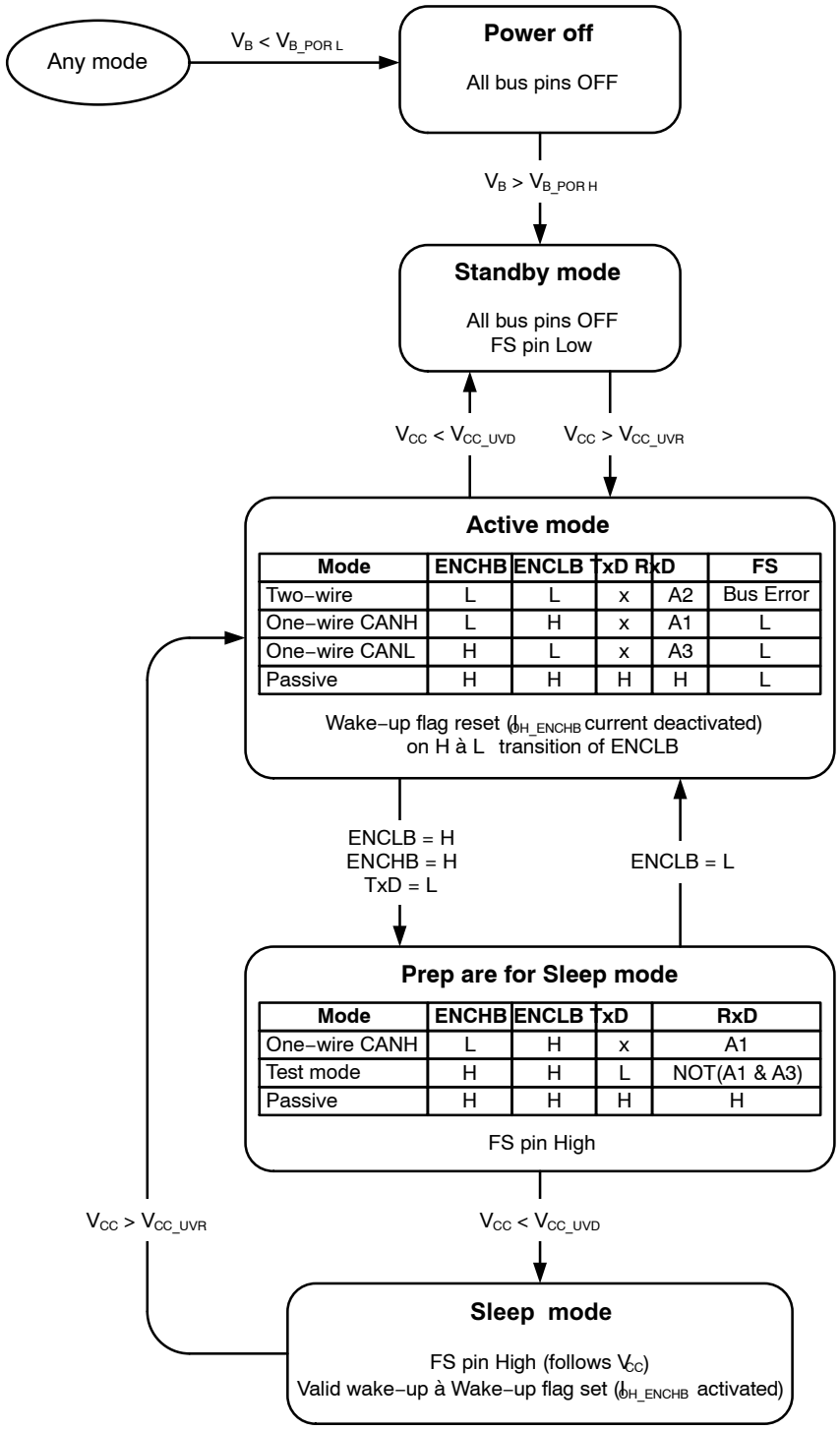


Figure 7. Operation Modes

FAILURE DETECTION

Bus Failures

Several open and short failures can occur that may influence operation. They are shown in Figure 8. Those failures are described in accordance to ISO 11992.

NCV7390 allows to maintain data transmission by control via ENCLB and ENCHB in case of an interruption of CANH or CANL (cases 1 and 2) or a short of one cable to ground (cases 4 and 5) or to supply voltage (cases 3 and 6) or a short circuit between CANH and CANL (case 7). Data transmission is no longer possible if both cables are affected by a short circuit (except case 7) or interruption (case 8).

Bus Failure Detection

The bus failure detection is active in Active Two−wire mode only.

The implemented fault status flags an incorrect 2−wire receiving condition in case of wire break or short condition at one bus line.

An internal error counter is incremented upon following events:

- A2 detects recessive to dominant edge while A1 or A3 is recessive,
- A1 or A3 detects dominant to recessive edge while A2 is dominant.

The first detection condition covers one bus line interruption scenario (case 1 and 2). The bus differential comparator A2 may still receive valid signal, but the single−ended comparators A1 or A3 receives permanent recessive.

The second detection condition covers CANH short to battery supply scenario (case 6) and CANL short to GND scenario (case 4) where the single−ended comparator A1 or A3 still receives correct data while the differential comparator A2 permanently receives dominant state.

The NCV7390 is typically not able to detect following cases, where the differential A2 receiver stays recessive:

- short circuit between CANH and CANL (case 7)
- both CANH and CANL interruption (case 8)
- CANH shorted to GND (case 5)
- CANL shorted to supply voltage (case 3)

These failure modes can be still detected by the microcontroller as a communication timeout since there are no data on RxD output.

A bus failure is detected when the internal error counter reaches value 7. Once the bus failure is detected, the fault status output FS is set High. The FS pin combines an open drain output with an internal pull−up resistor and a digital input that allows to receive an external request to reset the error logic.

The bus error logic can be reset by following events:

- Power on reset
- Low level on TxD pin if the failure was not yet set active (FS still low level)
- High level on ENCHB or ENCLB pins
- Forcing the FS pin Low externally if the pin is in high state

Overtemperature Detection

The thermal protection circuit protects the IC from damage by switching off all CAN bias and driving pins if the junction temperature exceeds the thermal shutdown temperature (See parameter T_{JSD}). The overtemperature is not flagged on FS pin.

All other IC functions continue to operate.

Because these CAN bias and driver pins dissipates most of the power, the power dissipation and temperature of the IC is expected to be reduced once the transmitter is disabled. The CAN bias and driving pins are re−enabled when the junction temperature falls below the thermal shutdown temperature T_{JSD} minus hysteresis. (See T_{JSD_HYST}).

The thermal protection circuit is particularly needed in case of a bus line short condition.

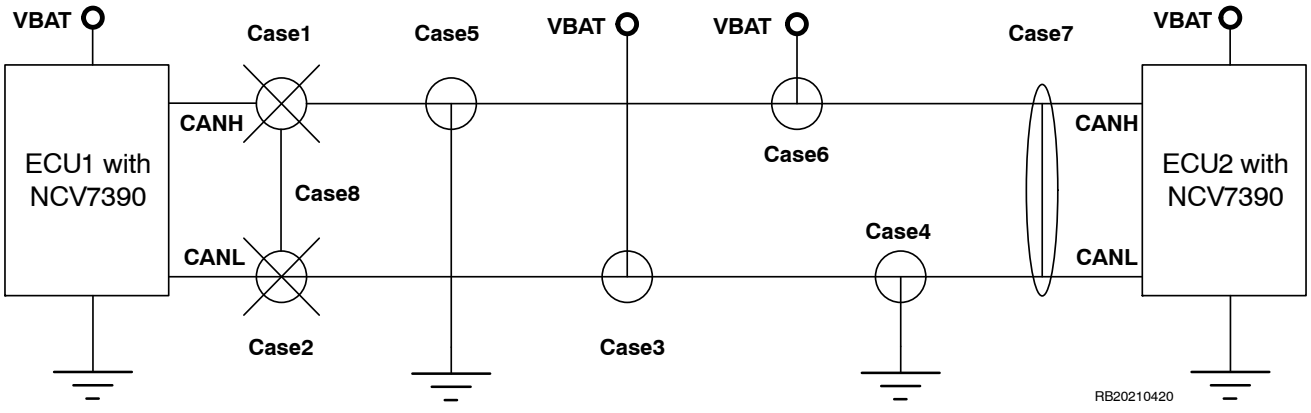


Figure 8. Bus Failures

FAIL SAFE FEATURES

A current−limiting circuit protects the bus bias and driving pins from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The bus is protected from automotive electrical transients (according to ISO 7637; see Figure 10).

Pin TxD and pin ENCLB are pulled high internally should the input become disconnected.

MEASUREMENT SETUPS AND DEFINITIONS

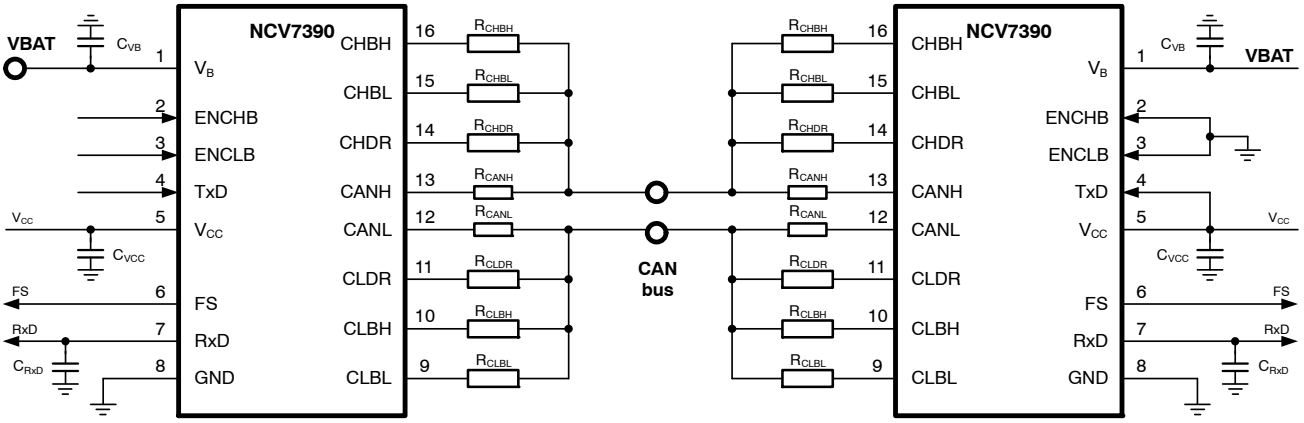


Figure 9. Test Circuit for Timing Characteristics

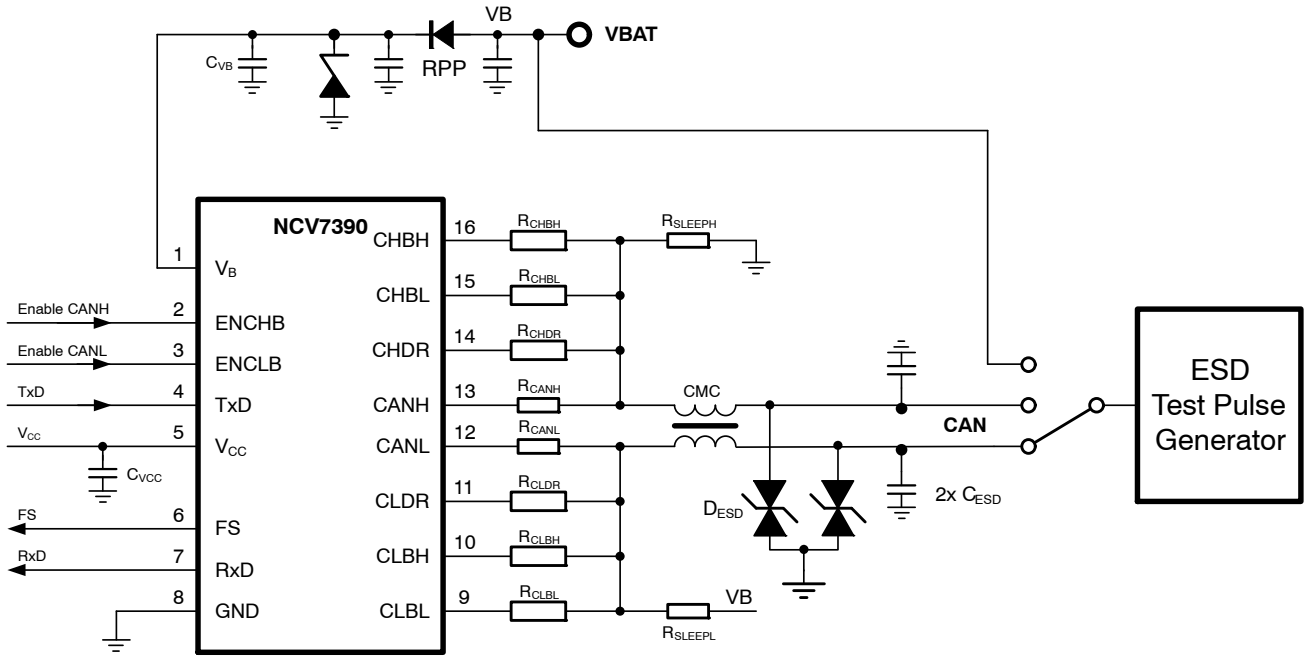
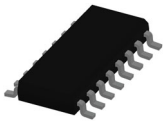


Figure 10. Test Circuit for ESD and Automotive Transients

ORDERING INFORMATION

Part Number	Description	Package	Shipping†
NCV7390DB0R2G	CAN Transceiver, ISO 11992	SOIC−16	2500 / Tape & Reel

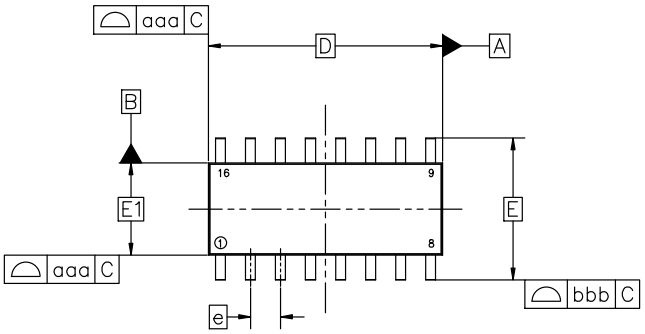
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



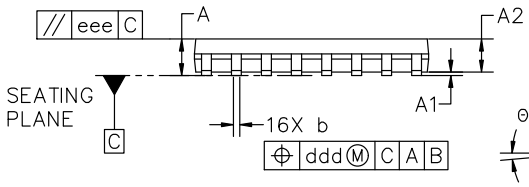
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

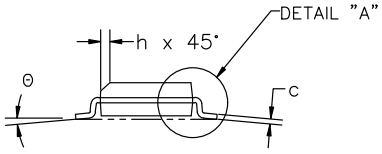
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



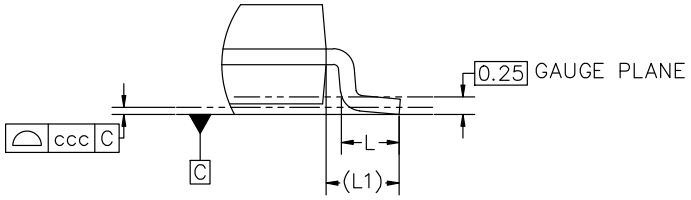
TOP VIEW



SIDE VIEW

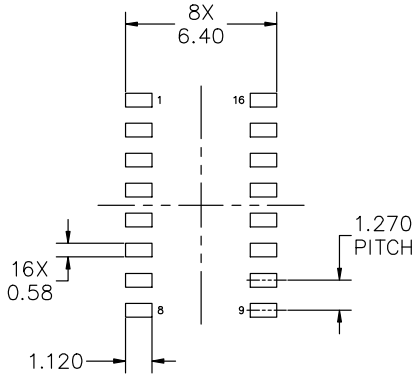


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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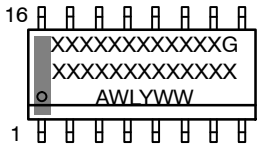
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales