

## Description

The AP33772S is a highly integrated USB Type-C® PD3.1 sink controller to support Extended Power Range (EPR)/Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR) / Programmable Power Supply (PPS) up to 21V. The device is targeted for DC power request and control for flexible Type-C Connector-equipped Devices (TCDs) with an embedded host MCU (Micro Controller Unit) and I2C interface pins (SCL, SDA).

Through the I2C interface interaction and interrupt mechanism, the host MCU sets up proper desired power profile (programmable voltage and current) with relevant threshold (OTP, OCP, etc.) and delegates PD negotiation tasks to the AP33772S. The host MCU further inquiries about status of various I2C registers for intended applications.

Based on high-voltage process, the AP33772S offers short protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. Smart built-in firmware of the AP33772S offers comprehensive safety protection scheme, including overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), over temperature protection (OTP) and moisture detection of the Type-C connector. In addition, external OTP and thermal de-rating are supported by a NTC resistor.

Meanwhile, the AP33772S provides a LED pin to indicate the different PD power negotiation results, and a FLIP pin to show the cable plug-in orientation.

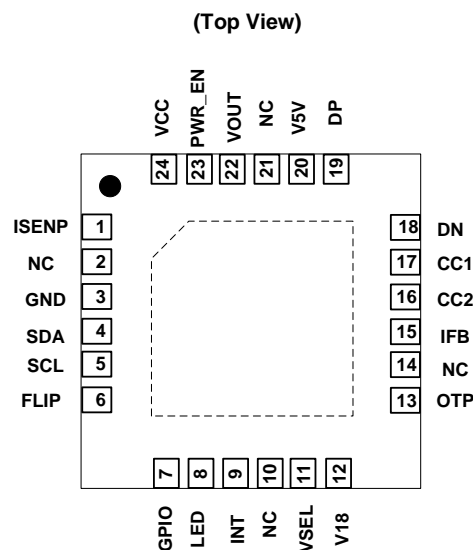
## Features

- USB PD3.1 v1.6 Certified with TID: 10062
- Operating Voltage Range of VCC: 3V to 31V
- Support PD3.1 EPR/AVS Up to 28V and SPR/PPS Up to 21V
- Support OVP with Hard Reset and Auto Restart
- Support UVP, OCP and OTP with Output Latch Off
- Support OTP and Thermal De-Rating through NTC Resistor
- Support OTP through Internal Junction Temperature Detection
- VBUS Short Protection on CC1/CC2 Pins Up to 34V
- I2C Commands for External MCU Monitoring, Control and Parameter Programming
- Dedicated Pins for CC Flip Indication and Interrupt Request
- Support Moisture Detection of the Type-C Connector
- LED Indication for Different Negotiation Results
- Driver for Output Enable N-MOS Switch
- Support Dead Battery Function
- Support Legacy Type-A Charger with Type-A to Type-C Cable
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.**

<https://www.diodes.com/quality/product-definitions/>

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments



W-QFN4040-24 (Type A1)

## Applications

- USB Type-C connector-equipped battery-powered devices
- USB Type-C connector-equipped DC-power input devices
- USB PD3.1 testers

## Typical Application Circuit

The AP33772S is a USB Type-C power delivery sink controller used to request power from an attached USB PD charger for a typical TCD embedded with a host MCU, as shown in the Figure 1 below.

Once the cable attachment is completed, the AP33772S is powered from VCC pin, and starts to do power-on initiation by setting up its internal registers and receiving the TCD configuration parameters from the external host MCU via I2C interface. After the power-on initialization, the AP33772S starts to decode USB PD commands from CC pin and gets the PD source capability. The host MCU makes a choice of the source power output capabilities, Power Data Object (PDOs), and sends request for PDO to the AP33772S through I2C command.

The AP33772S then automatically initiates the PD negotiation progress with the attached Type-C PD compliance charger (through Type-C to Type-C cable) or legacy Type-A charger (through Type-A to Type-C cable). If the PDO is matched, the MOS switch is turned on to connect VBUS to VOUT, and then the source adapter successfully provides power to the AP33772S-embedded TCD device.

The AP33772S supports the dead battery function and can be woken up as soon as an active PD adapter is plugged in the TCD Type-C receptacle. After the power link is set up between source and sink, OVP, UVP, OCP, and OTP protections are enabled to monitor the power charging status. In case power protection is triggered, the AP33772S shuts down the VOUT enable NMOS switch, and the host MCU will need to load new PD\_REQMSG to start a PDO negotiation process to resume charging operation.

The back-to-back N-MOS switches shown in Figure 1 could be simplified to a simple N-MOS switch for the TCD when there is no concern on reverse current from power module back to VBUS.

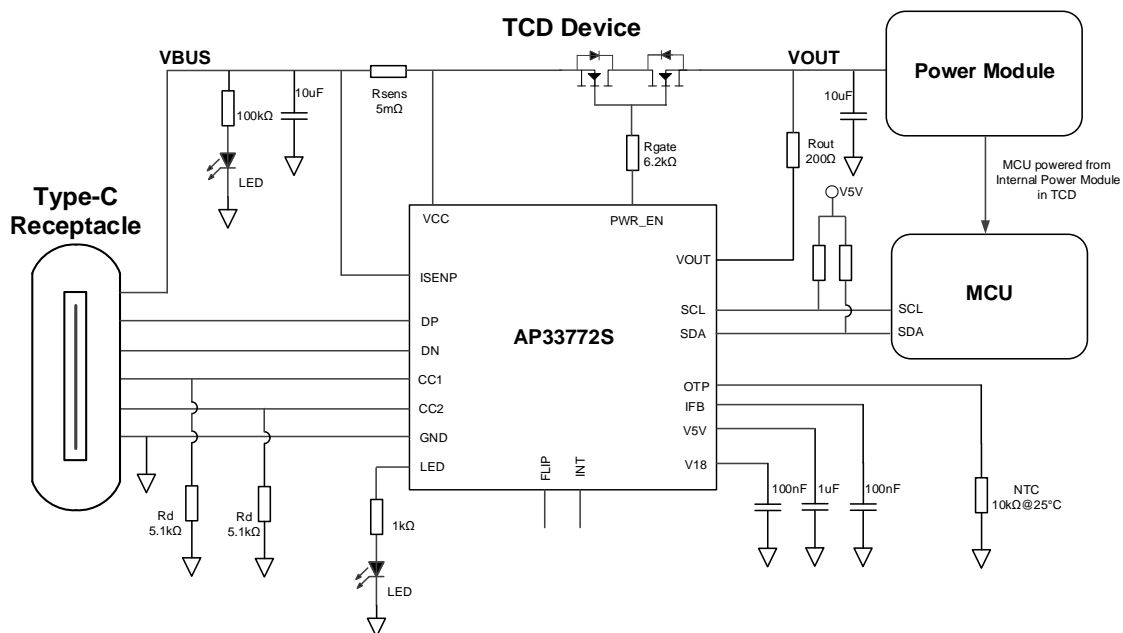


Figure 1. Typical System Configuration of AP33772S PD3.1 Sink Controller in a TCD

## Pin Descriptions

| Pin No. | Pin Name | Type (Note 4) | Pin Function                                                                                                                                                                                                    |
|---------|----------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | ISENP    | AHV           | Current sense positive node, connect to the positive node of the external current sensing resistor                                                                                                              |
| 2       | NC       | —             | No Connection                                                                                                                                                                                                   |
| 3       | GND      | GND           | Ground                                                                                                                                                                                                          |
| 4       | SDA      | DIO           | I2C data, need to be pulled up externally.                                                                                                                                                                      |
| 5       | SCL      | DIO           | I2C clock, need to be pulled up externally.                                                                                                                                                                     |
| 6       | FLIP     | DO            | Flip indicator of Type-C plug. LOW: CC1 detected. HIGH: CC2 detected.                                                                                                                                           |
| 7       | GPIO     | DIO           | General Purpose Input or Output (Function only for AP33772SDKZ-13-FA02)                                                                                                                                         |
| 8       | LED      | DO            | LED indicator pin, refer to Table 13 for detailed description                                                                                                                                                   |
| 9       | INT      | DO            | Interrupt pin is used to inform external MCU. LOW: normal. HIGH: interrupt happened.                                                                                                                            |
| 10      | NC       | —             | No Connection                                                                                                                                                                                                   |
| 11      | VSEL     | AI            | Voltage selection pin, connect resistance to ground to set Voltage (Function only for AP33772SDKZ-13-FA02)                                                                                                      |
| 12      | V18      | DP            | 1.8V LDO output for internal use only. Connect a 100nF cap to GND. This pin cannot drive external load.                                                                                                         |
| 13      | OTP      | AIO           | 100μA current source output for NTC connected to ground. This NTC is used to monitor temperature variation.                                                                                                     |
| 14      | NC       | —             | No Connection                                                                                                                                                                                                   |
| 15      | IFB      | AI            | For current measurement, a 100nF cap to Ground is suggested.                                                                                                                                                    |
| 16      | CC2      | AIO           | Type-C Configuration Channel 2 (CC2). The CC2 pin detects, configures and manages the connections across a USB Type-C cable.                                                                                    |
| 17      | CC1      | AIO           | Type-C Configuration Channel 1 (CC1). The CC1 pin detects, configures and manages the connections across a USB Type-C cable.                                                                                    |
| 18      | DN       | AIO           | DN of Type-C Connector                                                                                                                                                                                          |
| 19      | DP       | AIO           | DP of Type-C Connector                                                                                                                                                                                          |
| 20      | V5V      | AP            | Output of the internal LDO with VCC as input. A 1μF cap is required to connect this pin to GND. When VCC is off, V5V pin could be an alternative power path for the AP33772S when provided a 5V external power. |
| 21      | NC       | —             | No Connection                                                                                                                                                                                                   |
| 22      | VOUT     | AHV           | Terminal for VOUT Monitoring                                                                                                                                                                                    |
| 23      | PWR_EN   | AHV           | NMOS Switch gate control to switch the NMOS on or off.                                                                                                                                                          |
| 24      | VCC      | AHV           | The power supply of the IC. A 1μF cap is required to connect this pin to GND pin.                                                                                                                               |
| —       | EPAD     | GND           | Exposed pad is suggested to connect to Ground for better thermal dissipation.                                                                                                                                   |

**Table 1. Pin Descriptions of AP33772S Sink Controller**

Note 4:

AHV – Analog High Voltage pin.  
AP – Power for Analog Circuit and Analog I/O pins, 5.0V operation.  
AI – Analog Input pin.  
DP – Power for Digital Circuit operation.  
AIO – Analog Input/Output pin with 5.0V operation. However, DP/DN & CC1/CC2 pins are 3.3V operation.  
DI – Digital Input pin. All are 5.0V operation.  
DO – Digital Output pin. All are 5.0V operation.  
DIO – Digital Input/Output pin. All are 5.0V operation.

## Functional Block Diagram

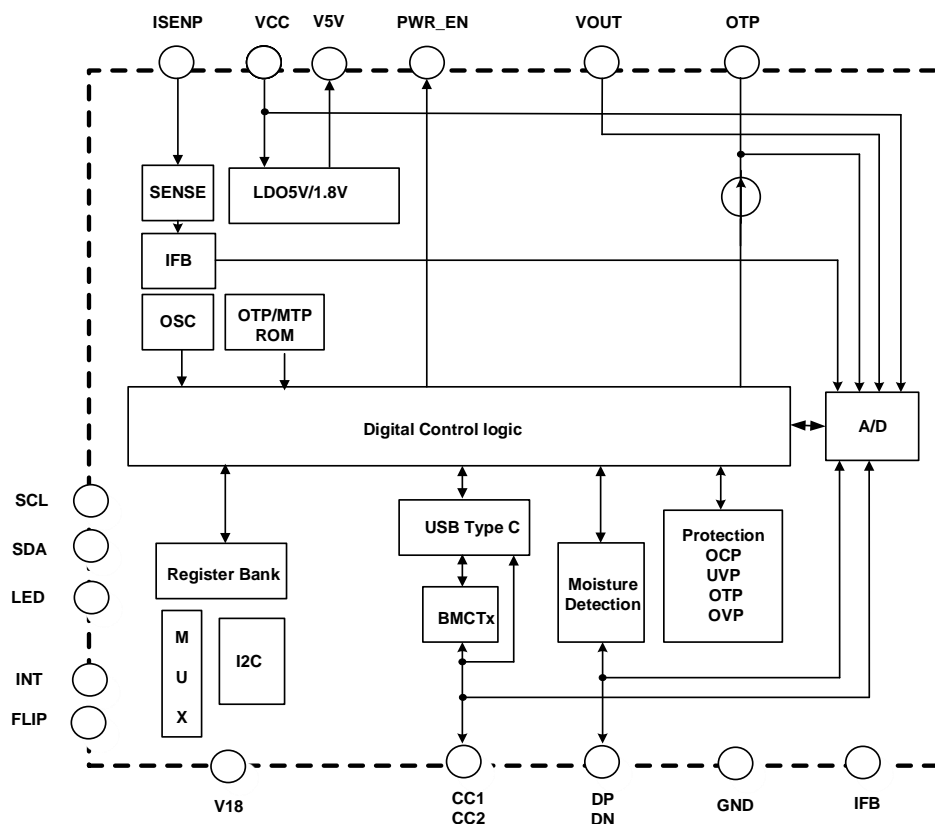


Figure 2. The Functional Block Diagram of AP33772S PD3.1 Sink Controller

## Absolute Maximum Ratings (Note 5)

| Symbol                                                                     | Parameter                                 | Rating      | Unit |
|----------------------------------------------------------------------------|-------------------------------------------|-------------|------|
| V <sub>VCC</sub>                                                           | Input Voltage at VCC Pin                  | -0.3 to 34  | V    |
| V <sub>V5V</sub>                                                           | Input Voltage at V5V Pin                  | -0.3 to 7   | V    |
| V <sub>V18</sub>                                                           | Input Voltage at V18 Pin                  | -0.3 to 5   | V    |
| V <sub>FLIP</sub> , V <sub>INT</sub> , V <sub>OTP</sub> , V <sub>LED</sub> | Input Voltage at FLIP, INT, OTP, LED Pins | -0.3 to 7   | V    |
| V <sub>VOU</sub> , V <sub>ISENP</sub>                                      | Input Voltage at VOU, ISENP Pins          | -0.3 to 31  | V    |
| V <sub>PWR_EN</sub>                                                        | Input Voltage at PWR_EN Pin               | -0.3 to 38  | V    |
| —                                                                          | Voltage from PWR_EN to VCC Pin            | -30 to 4    | V    |
| V <sub>CC1</sub> , V <sub>CC2</sub>                                        | Input Voltage at CC1, CC2 Pins            | -0.3 to 34  | V    |
| V <sub>DP</sub> , V <sub>DN</sub>                                          | Input Voltage at DP, DN Pins              | -0.3 to 7   | V    |
| V <sub>SCL</sub> , V <sub>SDA</sub>                                        | Input Voltage at SCL, SDA Pins            | -0.3 to 7   | V    |
| T <sub>J</sub>                                                             | Operating Junction Temperature            | -40 to +150 | °C   |
| T <sub>STG</sub>                                                           | Storage Temperature                       | -65 to +150 | °C   |
| T <sub>LEAD</sub>                                                          | Lead Temperature (Soldering, 10s)         | +300        | °C   |
| ESD                                                                        | Human Body Model                          | 2           | kV   |
| ESD                                                                        | Charged Device Model                      | 750         | V    |

Note: 5. Stresses greater than those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods can affect device reliability.

## Package Thermal Information (Note 6)

| Symbol                | Parameter                                    | Value | Unit |
|-----------------------|----------------------------------------------|-------|------|
| R <sub>θJA</sub>      | Junction-to-Ambient Thermal Resistance       | 28    | °C/W |
| R <sub>θJC(top)</sub> | Junction-to-Case (Top) Thermal Resistance    | 16    | °C/W |
| R <sub>θJB</sub>      | Junction-to-Board Thermal Resistance         | 11.2  | °C/W |
| Ψ <sub>JT</sub>       | Junction-to-Top Characterization Parameter   | 0.4   | °C/W |
| Ψ <sub>JB</sub>       | Junction-to-Board Characterization Parameter | 11.4  | °C/W |
| R <sub>θJC(bot)</sub> | Junction-to-Case (Bottom) Thermal Resistance | 6.0   | °C/W |

Note: 6. Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

## Recommended Operating Conditions

| Symbol                              | Parameter                            | Min  | Max  | Unit |
|-------------------------------------|--------------------------------------|------|------|------|
| V <sub>VCC</sub>                    | Power Supply Voltage at VCC Pin      | 3.3  | 31   | V    |
| V <sub>V5V</sub>                    | Input Voltage at V5V Pin             | 4.37 | 5.33 | V    |
| V <sub>DP</sub> , V <sub>DN</sub>   | Input Voltage at DP, DN Pins         | 2.75 | 3.25 | V    |
| V <sub>SCL</sub> , V <sub>SDA</sub> | Input Voltage at SCL, SDA Pins       | 4.37 | 5.33 | V    |
| T <sub>J</sub>                      | Operating Junction Temperature Range | -40  | +125 | °C   |
| T <sub>A</sub>                      | Operating Ambient Temperature        | -40  | +85  | °C   |

# Electrical Characteristics (@ T<sub>A</sub> = +25°C, unless otherwise specified.)

| Symbol                                      | Parameter                                                                                      | Condition             | Min  | Typ   | Max  | Unit |
|---------------------------------------------|------------------------------------------------------------------------------------------------|-----------------------|------|-------|------|------|
| <b>VCC SECTION</b>                          |                                                                                                |                       |      |       |      |      |
| V <sub>ST</sub>                             | Startup Voltage                                                                                | —                     | 2.5  | 2.8   | 3.5  | V    |
| V <sub>UVLO</sub>                           | Minimum Operating Voltage                                                                      | —                     | 2.3  | 2.7   | 3    | V    |
| V <sub>VCC_HYS</sub>                        | VCC Hysteresis (V <sub>ST</sub> -V <sub>UVLO</sub> )                                           | —                     | 0.05 | —     | —    | V    |
| I <sub>VCC_OPR</sub>                        | Operating Supply Current                                                                       | V <sub>VCC</sub> = 5V | —    | 3.3   | 6    | mA   |
| <b>CC1/CC2 SECTION</b>                      |                                                                                                |                       |      |       |      |      |
| V <sub>L_RD3A</sub>                         | Low Voltage Threshold Used to Distinguish R <sub>D</sub> Attached or Detached for 3A Delivery  | —                     | —    | 1.35  | —    | V    |
| V <sub>H_RD3A</sub>                         | High Voltage Threshold Used to Distinguish R <sub>D</sub> Attached or Detached for 3A Delivery | —                     | —    | 2.0   | —    | V    |
| <b>CURRENT SOURCE SECTION</b>               |                                                                                                |                       |      |       |      |      |
| I <sub>OTP</sub>                            | OTP Current Source (Note 8)                                                                    | —                     | —    | 100   | —    | μA   |
| I <sub>OTP_RANGE</sub>                      | OTP Current Source Range (Note 8)                                                              | —                     | -8   | —     | +8   | %    |
| <b>FLIP, INT, OTP, LED, and I2C SECTION</b> |                                                                                                |                       |      |       |      |      |
| V <sub>GPIOD</sub>                          | FLIP, INT, OTP, LED Pins Output Voltage Range (Note 8)                                         | V <sub>VCC</sub> = 5V | 4.37 | 4.85  | 5.33 | V    |
| V <sub>GPIOD_HI</sub>                       | FLIP, INT, OTP, LED Pins Input High Voltage (Note 8)                                           | V <sub>VCC</sub> = 5V | 1.4  | —     | —    | V    |
| V <sub>GPIOD_LO</sub>                       | FLIP, INT, OTP, LED Pins Input Low Voltage (Note 8)                                            | V <sub>VCC</sub> = 5V | —    | —     | 0.4  | V    |
| I <sub>GPIOD</sub>                          | FLIP, INT, OTP, LED Pins Sink/Source Capability (Note 8)                                       | —                     | 2    | —     | —    | mA   |
| V <sub>I2CO</sub>                           | SDA, SCL Power Supply Range (Note 8)                                                           | V <sub>VCC</sub> = 5V | —    | 4.85  | —    | V    |
| V <sub>I2C_HI</sub>                         | SDA, SCL Input Low Voltage (Note 8)                                                            | V <sub>CC</sub> = 5V  | 1.4  | —     | —    | V    |
| V <sub>I2C_LO</sub>                         | SDA, SCL Input Low Voltage (Note 8)                                                            | V <sub>CC</sub> = 5V  | —    | —     | 0.4  | V    |
| F <sub>SCL</sub>                            | SCL Clock Frequency (Note 8)                                                                   | —                     | —    | —     | 400  | kHz  |
| <b>PROTECTION FUNCTION SECTION</b>          |                                                                                                |                       |      |       |      |      |
| V <sub>OVP5V</sub>                          | OVP_5V Enable Voltage (Notes 7, 8)                                                             | —                     | —    | 7     | —    | V    |
| V <sub>OVP20V</sub>                         | OVP_20V Enable Voltage (Notes 7, 8)                                                            | —                     | —    | 22    | —    | V    |
| V <sub>OVP28V</sub>                         | OVP_28V Enable Voltage (Notes 7, 8)                                                            | —                     | —    | 31    | —    | V    |
| t <sub>DEBOUNCE_OVP</sub>                   | OVP Debounce Time (Note 9)                                                                     | —                     | —    | 90    | —    | ms   |
| t <sub>OV_DELAY</sub>                       | Delay from OVP Threshold Trip to NMOS Gate Turn-Off (Note 8)                                   | —                     | —    | —     | 50   | ms   |
| T <sub>OTP</sub>                            | Internal OTP Temperature                                                                       | —                     | —    | +130  | —    | °C   |
| <b>V5V SECTION</b>                          |                                                                                                |                       |      |       |      |      |
| V <sub>V5V</sub>                            | V5V Output Range                                                                               | —                     | 4.37 | 4.85  | 5.33 | V    |
| I <sub>V5V</sub>                            | V5V Source Capability                                                                          | —                     | —    | 30    | —    | mA   |
| <b>ADC SECTION</b>                          |                                                                                                |                       |      |       |      |      |
| V <sub>FS</sub>                             | Full Swing Range                                                                               | —                     | —    | 2.048 | —    | V    |
| —                                           | Resolution                                                                                     | —                     | —    | 8     | —    | Bit  |
| —                                           | DNL                                                                                            | —                     | —    | 1     | —    | LSB  |

Notes: 7. 110% OVP setting @ PDO > 18V. PDO+2V OVP setting @ PDO ≤ 18V.

8. Guaranteed by design.

9. OVP blanking time during V<sub>O</sub> transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

## Functional Description

### Overview

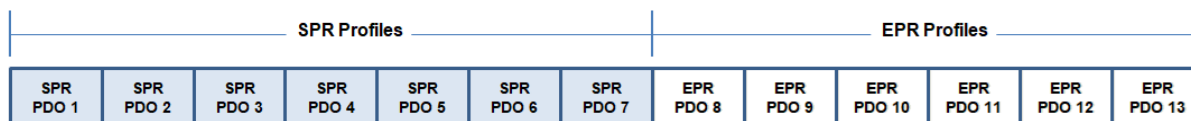
The AP33772S, a highly integrated USB Type-C PD3.1 sink controller, supports EPR/AVS up to 28V and provides SPR/PPS up to 21V. The device is targeted for DC power request and control for flexible Type-C Connector-equipped Devices (TCDs) with an embedded host MCU (Micro Controller Unit) and I2C interface pins (SCL, SDA).

### Cable Attachment and Power-On Initialization

After plugging the cable from a powered PD source adapter into the AP33772S-equipped TCD device, both  $R_d$  (shown in Figure 1, a 5.1k $\Omega$  resistor defined by the USB Type-C Cable and Connector Specification, Revision 2.0, which can be downloaded from the official USB website) are connected to the Configuration Channel pins (CC1/CC2). According to the USB PD Type C definition, only one of the CC1/CC2 can be pull down by  $R_d$  as the cable configuration channel (CC) wire, the other CC1 or CC2 wire will act as VCONN to power the plug from the source side USB PD controller (like to power the e-Marker chip in the cable), thus the CC/VCONN configuration and flip polarity are established. As soon as the above cable attachment flow is completed, the PD source adapter starts broadcasting PD source capabilities to the PD sink through CC pin, which is connected to the AP33772S internal Bi-phase Mark Code (BMC) block.

Meanwhile, the AP33772S starts to do power on initiation as soon as its VCC pin is powered from the 5V VBUS. After its internal MCU default configuration and registers are set up, the AP33772S will act as a I2C slave device and wait for the external host MCU to load the TCD configuration parameters to the internal I2C registers of the AP33772S, and then to update the AP33772S internal configuration accordingly.

During the negotiation, the source capabilities are stored in the AP33772S internal registers and the external MCU will read the source capabilities information through I2C interface. A total of 13 PDO registers are used to store the source capabilities of PD adapter, including 7 for SPR and 6 for EPR as Figure 3 below.



**Figure 3. A Total of 13 PDO Registers Are Used to Store the Source Capabilities of PD Adapter**

Once the source capability is received, the AP33772S will reply with a CRC good command and first request a default 5V from the source adapter. The AP33772S is now powered by the 5V profile from the source adapter and waiting for host MCU to deliver requests for a new PDO power profile or other control commands through the I2C interface.

### I2C Interface and Control

I2C interface (SCL, SDA pins) and INT pin are used as the communication channels between the AP33772S and the host MCU of the TCD device. During the power on initialization, the host MCU needs to deliver the system configuration parameters to the AP33772S for its internal set up. After the system set up, the host MCU can timely update the power profiles from the source adapter capability. Meanwhile, the system MCU can monitor the AP33772S internal registers and then give a control of the system operation through I2C commands accordingly.

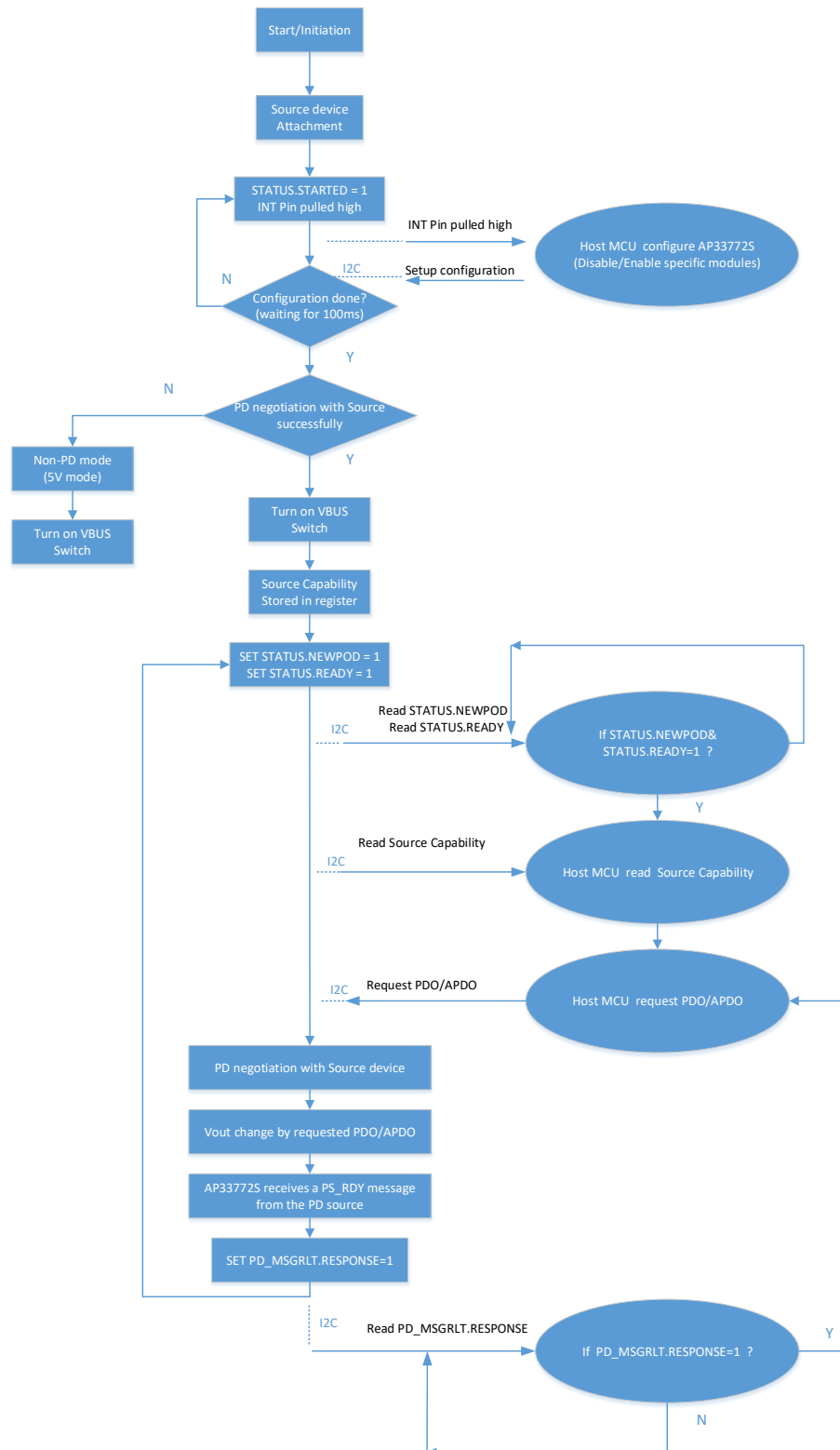
All of the I2C commands used in the AP33772S are summarized in Table 16. The functions include:

1. PDO information getting and New PDO request (i.e. Table 2, 3)
2. Protection threshold setting (i.e. Table 4, 5, 6, 7, 8)
3. System configuration setting (i.e. Table 3, 9, 10)
4. System data acquisition
5. System status inquiry (i.e. Table 11, 12, 13)
6. Legacy support (i.e. Table 14)

## Functional Description (continued)

### Power Policy Management Flowchart

Below is the power policy management flowchart of the AP33772S. Any source side power device connected to the AP33772S, it will follow this flow to handle power requests and related actions.





## Functional Description (continued)

### Source PDO Information Getting

Before selecting a new PDO profile, the host MCU should get the total PDO register information that has been placed in the AP33772S I2C registers through the I2C read commands. The AP33772S provides a 26-byte I2C command SRCPDO (0x20), which can read all the 13 PDOs at one time. In addition, there are 13 commands provided for host MCU to read each PDO information individually, where SRC\_SPR\_PDO1 (0x21) to SRC\_SPR\_PDO7 (0x27) and SRC\_EPR\_PDO8 (0x28) to SRC\_EPR\_PDO13 (0x2D) are used for SPR PDOs and EPR PDOs respectively.

The AP33772S will echo each PDO read command with a 2-byte data which include the PDO type (SPR, EPR, Fixed, PPS, AVS), voltage range (minimum, maximum) and current maximum.

### Request a New Source PDO

The host MCU can select a suitable PDO to fit in the system application request and then deliver it to the AP33772S through I2C command PD\_REQMSG (0x31). It is a 16-bit word used to send the message of requested PDO, Operating Current and Output Voltage settings for APDO at runtime as shown in Table 2 below, where:

1. PDO\_INDEX can assign the target PDO from the PDO index (information stored in the PDO register).
2. CURRENT\_SEL can set the operating current value of RDO.
3. VOLTAGE\_SEL can set the output voltage value of PPS/AVS RDO, only for assigned APDO (Augmented PDO).

| PD_REQMSG   | Bit   | Attribute | Pwr-On | Description                                                                                                                                                                                                                         |
|-------------|-------|-----------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PDO_INDEX   | 12:15 | WO        | 0h     | [0001] to [0111]: For SPR PDO1 to PDO7,<br>[1000] to [1101]: For EPR PDO8 to PDO13,<br>if its corresponding PDO is detected.<br>Others = Reserved                                                                                   |
| CURRENT_SEL | 8:11  | WO        | 0h     | Operating Current Select<br>[0000] to [1111] = 1.00A to 5.00A                                                                                                                                                                       |
| VOLTAGE_SEL | 0:7   | WO        | 0h     | VOLTAGE_SEL has no meaning for Fixed PDO selected<br>If set B [15] = 0 (select SPR):<br>output voltage in 100mV/unit for PPS APDO selected<br>If set B [15] = 1 (select EPR):<br>output voltage in 200mV/unit for AVS APDO selected |

**Table 2. The I2C Command PD\_REQMSG (0x31) Is Used to Refresh Existing Sink RDO**

After the AP33772S receiving PD\_REQMSG command, it will generate a new RDO of voltage and current and then starts to negotiate with PD source. Once the negotiation is completed, both the registers of STATUS and PD\_MSGRLT are updated accordingly.

Meanwhile, the AP33772S also provides a simple command to request Maximum current and Maximum voltage of the selected source PDO by setting only the PDO\_INDEX to the desired source PDO and keep CURRENT\_SEL = 0xF and VOLTAGE\_SEL = 0xFF.

For example, if source PDO3 is valid then the host MCU can write PD\_REQMSG with 0x3FFF, and the AP33772S will request the Maximum current and Maximum voltage of source PDO3.

### Support EPR / AVS

If the PD Source supports EPR Mode, after the first negotiation, the AP33772S will try to enter EPR Mode when PDCONFIG (0x05) is set to 1 at EPR\_MODE bit, as Table 3 below. If successfully entering EPR Mode, the AP33772S stores the EPR Source Capability in SRC\_EPR\_PDOx registers (0x28 to 0x2D) and enables EPR request.

| PDCONFIG    | Bit | Attribute | Pwr-On | Description                                                                                                 |
|-------------|-----|-----------|--------|-------------------------------------------------------------------------------------------------------------|
| —           | 7:4 | RW        | 0h     | Reserved                                                                                                    |
| —           | 3   | RW        | 0h     | Reserved                                                                                                    |
| DRSWP_EN    | 2   | RW        | 0h     | 0/1: Reject/Accept Data Role Swap from Port Partner,<br>and set Dual-Role Data bit of Sink Fixed PDO to 0/1 |
| PPS_AVS_EN  | 1   | RW        | 1h     | 0/1: Disable/Enable sink PPS and AVS capability                                                             |
| EPR_MODE_EN | 0   | RW        | 1h     | 0/1: Disable/Enable EPR mode                                                                                |

**Table 3. The I2C Command PDCONFIG (0x05) Is Used to Enable Sink EPR Mode**

## Functional Description (continued)

### Default Voltage Selection (Function only for AP33772SDKZ-13-FA02)

Before the host MCU completes a PDO negotiation with the AP33772S. The AP33772S supports setting up a desired original default voltage values through external resistor setting, up to eight resistors are supported for voltage selections where are connected to VSEL pin. It is recommended to use the resistors with  $\pm 1\%$  accuracy or better, to connect to the VSEL pin to ensure the request selection. The mapping between VSEL selection and resistance values are illustrated in Table 4. The original default voltage set by external resistor will be covered by the selected PDO after host MCU establish communication with the AP33772S through I2C. If the VSEL setting does not match the PD Source capability, the AP33772S will request the default Fixed\_5V PDO and the maximum current to negotiate with the source.

| Index                   | 1               | 2  | 3   | 4   | 5   | 6   | 7        | 8        |
|-------------------------|-----------------|----|-----|-----|-----|-----|----------|----------|
| VSEL                    | 5V              | 9V | 12V | 15V | 20V | 28V | Reserved | Reserved |
| RVSEL (k $\Omega$ , 1%) | 100 or Floating | 82 | 66  | 52  | 39  | 26  | 15       | 5.1      |

**Table 4. The Mapping between VSEL Amplitudes and Resistance Values**

### Integrated Power Protection

Based on high-voltage process, the AP33772S offers short-protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. In addition, the built-in firmware of the AP33772S offers comprehensive safety protection schemes, including OTP, OCP, OVP and UVP. Besides, moisture detection of the connector is provided. When the protection occurs, the associated VOUT MOS switch is turned off to disconnect VBUS from VOUT.

### Overtemperature Protection (OTP) and Thermal De-rating

A NTC thermistor is used to measure temperature of potential hot spot on the board. NTC can be connected to a constant current source of 100 $\mu$ A at OTP pin. As the temperature changes NTC resistance changes, with the AP33772S internal ADC, OTP pin voltage is measured and the NTC resistance can be calculated. The AP33772S then estimates the temperature value based on the 4 user-input NTC resistance values (refer to **Temperate Estimation**) and this estimated temperature can be read by accessing TEMP (0x13) register through I2C command.

The I2C command OTPTHR (0x1A) register, as shown in Table 5 below, is used to set OTP threshold, and is 78h (+120 $^{\circ}$ C) by default. If the TEMP value rises over the OTPTHR value after the de-bouncing time, the OTP is triggered, and STATUS Bit [6] is set to High. The associated output enable MOS switch will be turned off.

| OTPTHR | Bit | Attribute | Pwr-On | Description                                                                                                                                        |
|--------|-----|-----------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| OTPTHR | 7:0 | RW        | 78h    | OTP threshold, Unit: $^{\circ}$ C<br>The temperature threshold triggers the OTP function, the default value for OTPTHR is 78h (+120 $^{\circ}$ C). |

**Table 5. The I2C Command OTPTHR (0x1A) Is Used to Set OTP Threshold**

Furthermore, the AP33772S includes I2C command DRTHR (0x1B) register, as shown in Table 6 below, which can be used to program threshold temperature to trigger power de-rating function. If TEMP value rises above DRTHR, for PDO supporting PPS APDO, after de-bouncing time (30ms), the device will send out new RDO to negotiate with PDO source device, to reduce the input current by 50%. The AP33772S monitors the temperature at the potential hot spot continuously (with 1kHz sampling frequency), through NTC. If TEMP value falls 10C below DRTHR, the device negotiates with PDO again and recovers the charging power.

| DRTHR | Bit | Attribute | Pwr-On | Description                                                                                                                                                      |
|-------|-----|-----------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DRTHR | 7:0 | RW        | 78h    | De-Rating threshold, Unit: $^{\circ}$ C<br>The temperature threshold triggers Power De-Rating procedure, the default value for DRTHR is 78h (+120 $^{\circ}$ C). |

**Table 6. The I2C Command DRTHR (0x1B) Is Used to Set De-Rating Threshold**

In addition, the internal OTP is supported through Internal junction temperature detection. When the temperature goes beyond the internal OTP threshold, the associated VOUT MOS switch is turned off to disconnect VBUS from VOUT.

## Functional Description(continued)

### Overcurrent protection (OCP) Threshold Setting

The AP33772S supports OCP to control the output load condition by monitoring the output current through detection of IR drop on the 5mΩ Rsense resistor. Once the TCD device draws more current than the OCP threshold level after de-bounce time (30ms), the AP33772S enters FAULT states by turning off the VOUT MOS Switches.

Table 7 bellow shows the correspondence between OCPTHR and OCP Threshold Current, where the OCPTHR stands for **IOCPTHR**, OCP threshold current defined by user via I2C command OCPTHR (0x19). The user defined OCPTHR value is an 8-bit register with 50mA/LSB and 00h by default.

After successful negotiation with the PD source, if the OCPTHR value is still 00h, the OCP Threshold Current would be 110% of the I<sub>MAX</sub>, maximum current of the selected PDO/APDO. If the OCPTHR value has been updated through I2C command, the OCP Threshold Current would be 110% of **IOCPTHR** value.

| OCPTHR      | OCP Threshold Current             |
|-------------|-----------------------------------|
| OCPTHR = 0  | I <sub>MAX</sub> * 110% (Note 10) |
| OCPTHR != 0 | IOCPTHR* 110%                     |

Note 10: I<sub>MAX</sub>: Maximum Current of PDO/APDO.

**Table 7. Correspondence between OCPTHR and OCP Threshold Current**

### Overvoltage Protection (OVP) Threshold and Adjustment

The AP33772S triggers the OVP protection when VBUS voltage is higher than OVP threshold voltage. The Table 8 bellow summarizes the correspondence between V<sub>VREQ</sub>, V<sub>OVPOS</sub> and OVP threshold voltage, where V<sub>VREQ</sub> is the voltage requested after successful power negotiation with the PD source adapter, and V<sub>OVPOS</sub> is the OVP offset, refer to Table 16 for V<sub>OVPOS</sub> programming via I2C command OVPTHR (0x18). If VBUS voltage is higher than OVP threshold value in OVPTHR after the de-bounce time limit, the AP33772S enters the FAULT state, where the VOUT MOS Switches are turned off.

| Mode     | Criteria                                        | OVP Threshold Voltage                  |
|----------|-------------------------------------------------|----------------------------------------|
| SPR Mode | (V <sub>VREQ</sub> + V <sub>OVPOS</sub> ) ≤ 20V | V <sub>VREQ</sub> + V <sub>OVPOS</sub> |
|          | (V <sub>VREQ</sub> + V <sub>OVPOS</sub> ) > 20V | V <sub>VREQ</sub> * 110%               |
| EPR Mode | (V <sub>VREQ</sub> + V <sub>OVPOS</sub> ) ≤ 40V | V <sub>VREQ</sub> + V <sub>OVPOS</sub> |
|          | (V <sub>VREQ</sub> + V <sub>OVPOS</sub> ) > 40V | V <sub>VREQ</sub> * 110%               |

**Table 8. Correspondence between V<sub>VREQ</sub>, V<sub>OVPOS</sub> and OVP Threshold Voltage**

### Undervoltage Protection (UVP) Threshold Adjustment

The AP33772S triggers the UVP protection when VBUS voltage is lower than UVP threshold Voltage. The Table 9 bellow shows the relation between under voltage protection level, UVPTHR, and UVP threshold voltage. The default value of UVPTHR is 80%, which can be modified via I2C command UVPTHR (0x17). If VBUS voltage is lower than UVP threshold after de-bounce time, the AP33772S enters FAULT state, where the VOUT MOS switches are turned off.

| UVPTHR | UVP Threshold Voltage   |
|--------|-------------------------|
| 1      | V <sub>VREQ</sub> * 80% |
| 2      | V <sub>VREQ</sub> * 75% |
| 3      | V <sub>VREQ</sub> * 70% |

**Table 9. Correspondence between V<sub>VREQ</sub>, UVPTHR and UVP Threshold Voltage**

### Moisture Detection

The AP33772S supports the moisture detection of the connector. As soon as the Type-C connector is plugged in, the impedance between DN/DP pin and ground is evaluated by internal ADC digitization and firmware calculation. If the impedance level is below the pre-determined threshold, the VOUT MOS switch is turned off to disconnect VBUS from VOUT, and the LED is tuned off and on, with the "MOISTURE" pattern accordingly, see LED Indication section for details. If the impedance check is normal, the AP33772S starts to negotiate with the source.

## Functional Description (continued)

### VOUT Enable Switch

Taking VBUS voltage as input, the built-in charge-pump circuit generates a high-voltage gate driver (PWR\_EN) to drive an external high-side NMOS switch. A 6.2kΩ resistance is suggested to connect the PWR\_EN to the NMOS gate. Once the PDO negotiations between source and sink are successful, and the VVREQ, the requested voltage, is greater than VVSELMIN, the PWR\_EN enables the NMOS switch and connects VBUS to VOUT. Otherwise, the NMOS switch will remain turned off, and VBUS is disconnected from VOUT.

Meanwhile, the NMOS VOUT enable switch is also used for power protection. Whenever output overvoltage, undervoltage, overcurrent, or over temperature occurs, the AP33772S enters the FAULT state, where the VOUT MOS Switches are turned off to protect the host system from possible damage. To get out of the Fault state, the host MCU will need to load new RDO to start a PDO negotiation process to resume charging operation.

### Protection Mode Configuration

To fit the comprehensive application scenarios, the power protection modes in the AP33772S are configurable through the I2C command CONFIG (0x04) as shown in Table 10 below.

| CONFIG | Bit | Attribute | Pwr-On | Description                                 |
|--------|-----|-----------|--------|---------------------------------------------|
| DR_EN  | 7   | RW        | 1h     | 0/1: Disable/enable DR (De-Rating) function |
| OTP_EN | 6   | RW        | 1h     | 0/1: Disable/enable OTP function            |
| OCP_EN | 5   | RW        | 1h     | 0/1: Disable/enable OCP function            |
| OVP_EN | 4   | RW        | 1h     | 0/1: Disable/enable OVP function            |
| UVP_EN | 3   | RW        | 1h     | 0/1: Disable/enable UVP function            |
| —      | 2   | RW        | 0h     | Reserved                                    |
| —      | 1   | RW        | 0h     | Reserved                                    |
| —      | 0   | RW        | 0h     | Reserved                                    |

Table 10. The CONFIG Command Is Used to Configure the Power Protection Schemes

### Interrupt Signal

The AP33772S supports a level-triggered interrupt signal through INT pin to the host MCU. The I2C command MASK (0x02) defines enable or disable of each interruptible event as shown in Table 11 below. The interrupt initialization is required before use. When the defined interruptible event happens, the AP33772S will set the INT pin output to level HIGH if the relevant event of the MASK register is enabled.

| MASK        | Bit | Attribute | Pwr-on | Description            |
|-------------|-----|-----------|--------|------------------------|
| —           | 7   | RW        | 0h     | Reserved               |
| OTP_MSK     | 6   | RW        | 0h     | 1: OTP status mask     |
| OCP_MSK     | 5   | RW        | 0h     | 1: OCP status mask     |
| OVP_MSK     | 4   | RW        | 0h     | 1: OVP status mask     |
| UVP_MSK     | 3   | RW        | 0h     | 1: UVP status mask     |
| NEWPDO_MSK  | 2   | RW        | 0h     | 1: NEWPDO status mask  |
| READY_MSK   | 1   | RW        | 1h     | 1: READY status mask   |
| STARTED_MSK | 0   | RW        | 1h     | 1: STARTED status mask |

Table 11. The MASK Register Defines Enable or Disable of Each Interruptible Event

### System Data Acquisition

During the normal operation, the host MCU can monitor the PDO negotiation result (VREQ and IREQ), and its VOUT timely status (VOUT voltage and current) through I2C commands. VREQ (0x14) and IREQ (0x15) are used to read the voltage and current requested, and VOLTAGE (0x11) and CURRENT(0x12) are used to read Output status. Meanwhile, the I2C command TEMP (0x13) is used to read the system temperature.

### System Status and Operating Mode Inquiry

The Host system MCU can monitor the PD system status through I2C interface. The Status command (0x01) is an 8-bit register and used to store the AP33772S status as Table 12 below.

Meanwhile, the user can read out the PD operating modes through I2C command OPMODE (0x03), as shown in Table 13 below, where CC Flip information and power source type are provided.

## Functional Description (continued)

### System Status and Operating Mode Inquiry (continued)

| STATUS  | Bit | Attribute | Pwr-On | Description                                                                         |
|---------|-----|-----------|--------|-------------------------------------------------------------------------------------|
| —       | 7   | RC        | 0h     | Reserved                                                                            |
| OTP     | 6   | RC        | 0h     | 1: OTP status                                                                       |
| OCP     | 5   | RC        | 0h     | 1: OCP status                                                                       |
| OVP     | 4   | RC        | 0h     | 1: OVP status                                                                       |
| UVP     | 3   | RC        | 0h     | 1: UVP status                                                                       |
| NEWPDO  | 2   | RC        | 0h     | 1: New source PDOs received (Valid when PDMOD = 1)                                  |
| READY   | 1   | RC        | 0h     | 1: Ready to receive I2C request/command                                             |
| STARTED | 0   | RC        | 0h     | 1: System started. Allow system configuration (register) to be updated within 100ms |

Table 12. The STATUS Command Is Used to Monitor AP33772S Operating Status

| OPMODE  | Bit | Attribute | Pwr-On | Description                                                                         |
|---------|-----|-----------|--------|-------------------------------------------------------------------------------------|
| CCFLIP  | 7   | RO        | 0h     | 0: CC1 is connected to CC line or unattached mode<br>1: CC2 is connected to CC line |
| DR      | 6   | RO        | 0h     | 0: Normal mode<br>1: DR (De-rating) mode                                            |
| DATARL  | 5   | RO        | 0h     | The current Port Data Role                                                          |
| —       | 4   | RO        | 0h     | Reserved                                                                            |
| —       | 3   | RO        | 0h     | Reserved                                                                            |
| —       | 2   | RO        | 0h     | Reserved                                                                            |
| PDMOD   | 1   | RO        | 0h     | 1: PD source connected                                                              |
| LGCYMOD | 0   | RO        | 0h     | 1: Legacy source connected (non-PD)                                                 |

Table 13. The OPMODE Command Is Used to Monitor if PD or Legacy Source Is Connected

### GPIO Control (Function only for AP33772SDKZ-13-FA02)

The Host system MCU can control the status of GPIO pin through I2C interface. The GPIO command (0x52) is an 8-bit register and used to control the GPIO (PIN 7) status as Table 14 below.

| GPIO       | Bit | Attribute | Pwr-On | Description                             |
|------------|-----|-----------|--------|-----------------------------------------|
| GPIO_PU_EN | 7   | RW        | 0h     | Enable GPIO internal pull-up resistor   |
| GPIO_PD_EN | 6   | RW        | 0h     | Enable GPIO internal pull-down resistor |
| —          | 5   | RO        | 0h     | —                                       |
| —          | 4   | RO        | 0h     | —                                       |
| GPIO_DI    | 3   | RO        | 0h     | GPIO input data                         |
| GPIO_IE    | 2   | RW        | 0h     | Enable GPIO input data                  |
| GPIO_DO    | 1   | RW        | 0h     | 0: output 'LO'<br>1: output 'HI'        |
| GPIO_OE    | 0   | RW        | 0h     | Enable GPIO output mode                 |

Table 14. The GPIO Command Is Used to Control the GPIO Pin

## Functional Description (continued)

### LED Indication

The AP33772S drives external LED lighting to show state indication through LED pin. The Table 15 below summarizes the LED indication and VOUT result in each state.

| State    | LED Indication  | VOUT | Comments                                                       |
|----------|-----------------|------|----------------------------------------------------------------|
| INIT     | NA              | OFF  | VBUS/Rp attached and AP33772S initialization                   |
| CHARGING | 4-sec Breathing | ON   | Successful negotiation or enter Non-PD Mode and start charging |
| MISMATCH | Full Light      | OFF  | VSELMIN mismatch ( $V_{REQ} < V_{SELMIN}$ )                    |
| MOISTURE | 2-sec Flicker   | OFF  | Abnormal impedance detected in the Type-C connector            |
| FAULT    | 0.6-sec Flicker | OFF  | OVP, OCP, UVP or OTP occurs                                    |

Table 15. LED Indication for Different Negotiation Results

### Legacy Type-A Charger Support

When the energy source is from a legacy Type-A charger with Type-A to Type-C cable connection to the TCD, the AP33772S enters the Non-PD Mode after PD negotiation fails. When VSELMIN is greater than VREQ, the associated VOUT MOS Switches are turned off. The Table 16 below shows the Non-PD Mode state of the AP33772S.

| Non-PD Mode State |                      |           |
|-------------------|----------------------|-----------|
| $V_{REQ}$         | $V_{SELMIN}$         | $V_{OUT}$ |
| $V_{REQ} = 5V$    | $V_{SELMIN} = 5V$    | ON        |
| $V_{REQ} = 5V$    | $V_{SELMIN} \geq 9V$ | OFF       |

Table 16. VOUT Voltage Status versus  $V_{SELMIN}$  under Non-PD Mode

### Temperature Estimation

An external NTC Thermistor can be connected to OTP pin to measure external temperature. OTP pin is connected to constant current source internally. As temperature changes NTC resistance changes, which is measure to estimate the temperature. With the AP33772S internal ADC, OTP pin voltage is measured and the NTC resistance can be calculated. The AP33772S then estimates the temperature value based on the 4 user-input NTC resistance values (TR25, TR50, TR75 and TR100), as shown in Figure 4 below, where the "LINEAR INTERPOLATION" and "LINEAR EXTRAPOLATION" are used for the inner range and outer range respectively. The estimated temperature is updated to internal register for I2C command TEMP (0x13) reading.

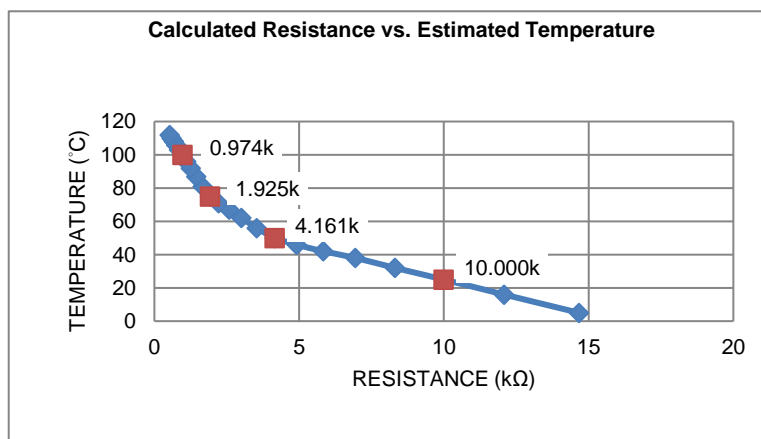


Figure 4. Calculated Resistance vs. Estimated Temperature Plot (RED Dot Shows Default Setting Values)

## Functional Description (continued)

### Temperature Estimation (continued)

The host MCU must initialize the TR25, TR50, TR75 and TR100 registers before reading TEMP register or enabling OTP protection and power derating functions. Otherwise, the Murata NTC NCP03XH103 4-point data as Table 17 below are used as default. The user can change the default 4-point data through I2C commands: TR25 (0x0C), TR50 (0x0D), TR75 (0x0E) and TR100 (0x0F), if a different NTC make is chosen.

| Register | Default Value | NTC Resistance (kΩ) | Temperature (°C) |
|----------|---------------|---------------------|------------------|
| TR25     | 2710h         | 10                  | +25              |
| TR50     | 1041h         | 4.161               | +50              |
| TR75     | 0788h         | 1.928               | +75              |
| TR100    | 03CEh         | 0.974               | +100             |

Table 17. The 4-Point NTC Resistances and Temperatures Are Used as Default in AP33772S

### Data Role Swap function (Function only for AP33772SDKZ-13-FA02)

DRSWP\_EN bit of register PDGONFIG can set 1 to accept Data Role Swap from Port Partner and set 0 to reject Data Role Swap from Port Partner. Default value of DRSWP\_EN bit of register PDGONFIG is 0.

Current Port Data Role can be read in the DATARL bit of register OPMODE

Write 1 DRSWP bit of register PD\_CMDMSG to send Data Role Swap information to Port Partner

| PD_CMDMSG | Bit | Attribute | Pwr-On | Description                 |
|-----------|-----|-----------|--------|-----------------------------|
| —         | 7:4 | WO        | 0h     | Reserved                    |
| —         | 3   | WO        | 0h     | Reserved                    |
| —         | 2   | WO        | 0h     | Reserved                    |
| DRSWP     | 1   | WO        | 0h     | 1: Issue DR_Swap command    |
| HRST      | 0   | WO        | 0h     | 1: Issue Hard Reset command |

Table 18. The PD\_CMDMSG Command

## Functional Description (continued)

### I2C Command Set Summary

The I2C commands used in the AP33772S are listed in Table 19 below.

| Register      | Command | Length | Pwr-On  | Description                                                                     |
|---------------|---------|--------|---------|---------------------------------------------------------------------------------|
| STATUS        | 0x01    | 1      | 00h     | Status                                                                          |
| MASK          | 0x02    | 1      | 03h     | Interrupt enable mask                                                           |
| OPMODE        | 0x03    | 1      | 00h     | Operation mode                                                                  |
| CONFIG        | 0x04    | 1      | F8h     | System configuration options                                                    |
| PDCONFIG      | 0x05    | 1      | 03h     | PD mode configuration options                                                   |
| SYSTEM        | 0x06    | 1      | 10h     | System control and information                                                  |
| TR25          | 0x0C    | 2      | 2710h   | Thermal Resistance @+25°C, Unit: Ω                                              |
| TR50          | 0x0D    | 2      | 1041h   | Thermal Resistance @+50°C, Unit: Ω                                              |
| TR75          | 0x0E    | 2      | 0788h   | Thermal Resistance @+75°C, Unit: Ω                                              |
| TR100         | 0x0F    | 2      | 03CEh   | Thermal Resistance @+100°C, Unit: Ω                                             |
| VOLTAGE       | 0x11    | 2      | 0000h   | The VOUT Voltage, LSB 80mV                                                      |
| CURRENT       | 0x12    | 1      | 00h     | The VOUT Current, LSB 24mA                                                      |
| TEMP          | 0x13    | 1      | 19h     | Temperature, Unit: °C<br>The default value is 19h (+25°C).                      |
| VREQ          | 0x14    | 2      | 0000h   | The latest requested voltage negotiated with the source, LSB 50mV               |
| IREQ          | 0x15    | 2      | 0000h   | The latest requested current negotiated with the source, LSB 10mA               |
| VSELMIN       | 0x16    | 1      | 19h     | The Minimum Selection Voltage, LSB 200mV<br>The default value is 19h (5000mV).  |
| UVPTHR        | 0x17    | 1      | 01h     | UVP threshold, percentage (%) of VREQ<br>The default value is 01h (80%).        |
| OVPTHR        | 0x18    | 1      | 19h     | OVP threshold, offset from VREQ. LSB 80mV<br>The default value is 19h (2000mV). |
| OCPTHR        | 0x19    | 1      | 00h     | OCP threshold, LSB 50mA                                                         |
| OTPTHR        | 0x1A    | 1      | 78h     | OTP threshold, Unit: °C<br>The default value is 78h (+120°C).                   |
| DRTHR         | 0x1B    | 1      | 78h     | De-rating threshold, Unit: °C<br>The default value is 78h (+120°C).             |
| SRCPDO        | 0x20    | 26     | All 00h | Get All PD Source Power Capabilities (PDO1 to PDO13)                            |
| SRC_SPR_PDO1  | 0x21    | 2      | 0000h   | Source SPR PDO1                                                                 |
| SRC_SPR_PDO2  | 0x22    | 2      | 0000h   | Source SPR PDO2                                                                 |
| SRC_SPR_PDO3  | 0x23    | 2      | 0000h   | Source SPR PDO3                                                                 |
| SRC_SPR_PDO4  | 0x24    | 2      | 0000h   | Source SPR PDO4                                                                 |
| SRC_SPR_PDO5  | 0x25    | 2      | 0000h   | Source SPR PDO5                                                                 |
| SRC_SPR_PDO6  | 0x26    | 2      | 0000h   | Source SPR PDO6                                                                 |
| SRC_SPR_PDO7  | 0x27    | 2      | 0000h   | Source SPR PDO7                                                                 |
| SRC_EPR_PDO8  | 0x28    | 2      | 0000h   | Source EPR PDO8                                                                 |
| SRC_EPR_PDO9  | 0x29    | 2      | 0000h   | Source EPR PDO9                                                                 |
| SRC_EPR_PDO10 | 0x2A    | 2      | 0000h   | Source EPR PDO10                                                                |
| SRC_EPR_PDO11 | 0x2B    | 2      | 0000h   | Source EPR PDO11                                                                |
| SRC_EPR_PDO12 | 0x2C    | 2      | 0000h   | Source EPR PDO12                                                                |
| SRC_EPR_PDO13 | 0x2D    | 2      | 0000h   | Source EPR PDO13                                                                |
| PD_REQMSG     | 0x31    | 2      | 0000h   | Send request message with selected voltage, current and PDO index               |
| PD_CMDMSG     | 0x32    | 1      | 00h     | Send specific PD command message                                                |
| PD_MSGRLT     | 0x33    | 1      | 00h     | Result and status of PD request or command message                              |
| GPIO          | 0x52    | 1      | 00h     | GPIO (Function only for AP33772SDKZ-13-FA02)                                    |

Table 19. The I2C Commands Provided in AP33772S PD3.1 Sink Controller Are Illustrated



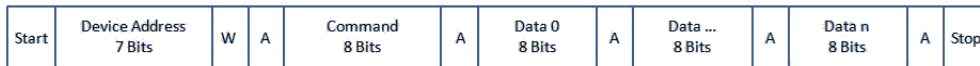
## Functional Description (continued)

### I2C Command Format

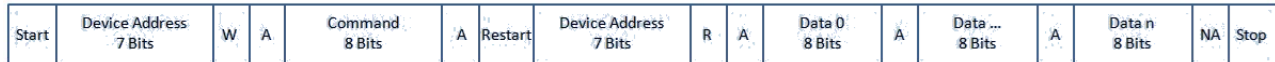
The AP33772S supports I2C communication with external system MCU through SDA, SCL and Interrupt pins after the power on reset. As an I2C slave device, the physical address of the AP33772S is 0x52. The I2C read and write operations are illustrated as below. All transactions begin with a Start and end with a Stop. A Start condition is defined as a HIGH to LOW transition of the SDA while SCL is HIGH. A Stop condition is defined as a LOW to HIGH transition of the SDA while SCL is HIGH. Start and Stop conditions are always generated by the I2C master, the host MCU of the TCD.

Data transfers follow the format shown below. After the Start condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data read/write bit (R/W) - a 'zero' indicates a data write (W), a 'one' indicates a data read (R). A data transfer is always terminated by a Stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated Start condition (Restart) and address another slave without first generating a Stop condition. Each byte has to be followed by an acknowledge bit (A). The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line to indicate data received during the acknowledge clock pulse.

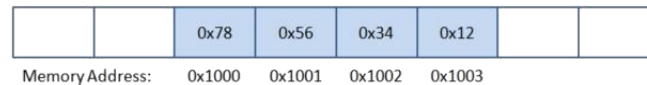
I2C Format for Write Data:



I2C Format for Read Data:



The memory representation of multi-byte data types on the AP33772S is Little Endian Byte Order. The least significant byte (the "little end") of the data is placed at the byte with the lowest address. For example, if the integer is stored as 4 bytes, then a variable X with value of 0x12345678 will be stored as Figure 5 below:

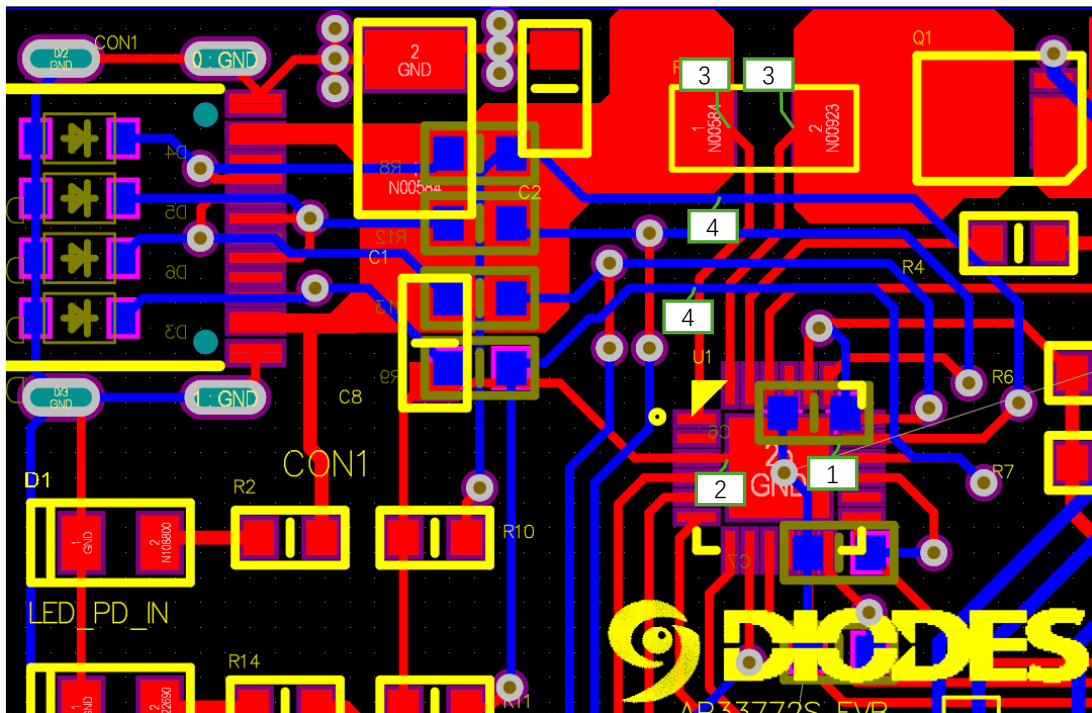


**Figure 5. The Little Endian Byte Order is Used in AP33772S**

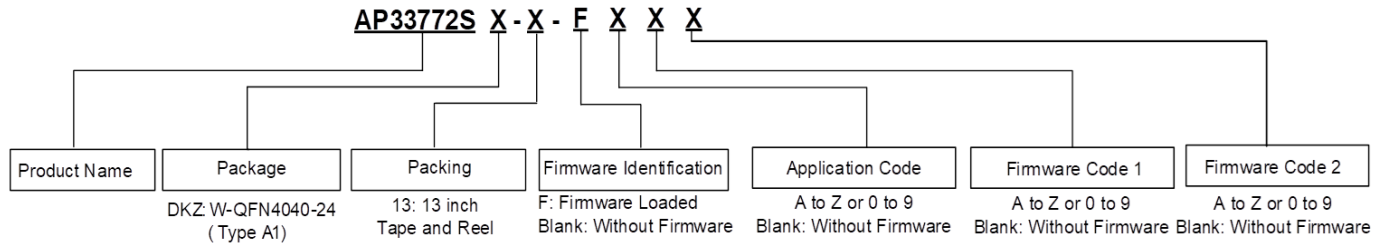
## PCB Layout Guideline

Suitable PCB layout is critical for stable operation and better ESD performance. Follow some guidelines as below:

1. Place the Vcc/V5V decoupling capacitor as close to the pins as possible.
2. The exposed pad of the IC must be connected to GND. It is better for noise immunity.
3. Current sensing traces must start directly from the footprint pads of current sensing resistor.
4. Use traces to connect CC1/CC2 pins to the USB Type-C receptacle as short as possible.



## Ordering Information (Note 12)



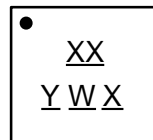
| Orderable Part Number<br>(Note 11) | Package                   | Identification<br>Code | Firmware Inside                                           | Packing |                 |
|------------------------------------|---------------------------|------------------------|-----------------------------------------------------------|---------|-----------------|
|                                    |                           |                        |                                                           | Qty.    | Carrier         |
| AP33772SDKZ-13-FA02                | W-QFN4040-24<br>(Type A1) | 6Y                     | Standard Firmware<br>(Function as Described in Datasheet) | 3000    | 13" Tape & Reel |
| AP33772SDKZ-13-FXXX                |                           |                        | Customized Firmware                                       |         |                 |

Notes: 11. It is recommended to order Standard Firmware device based on functions described in datasheet. For without firmware and customized options, please contact local distributor or Diodes Incorporated.  
 12. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information

W-QFN4040-24 (Type A1)

( Top View )

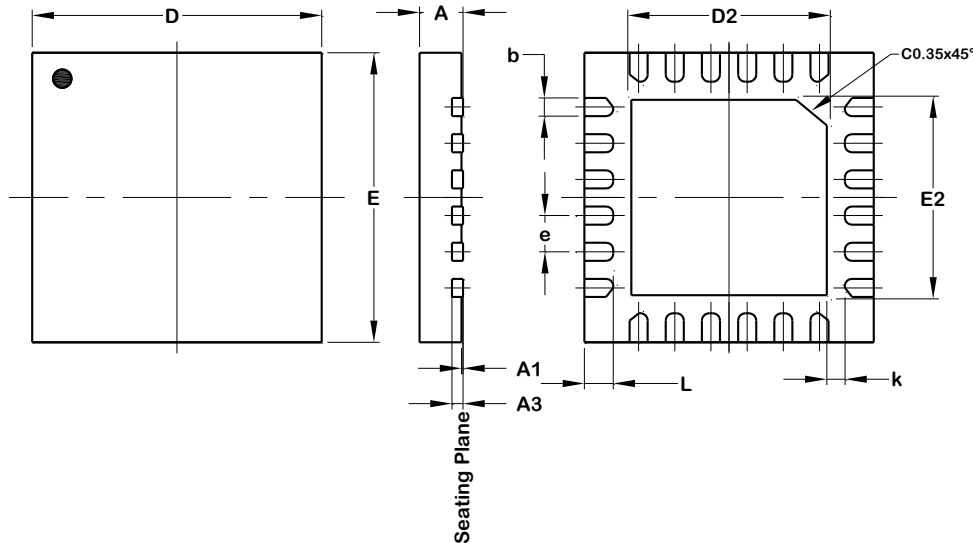


XX : Identification Code  
Y : Year : 0 to 9  
W : Week : A to Z : 1 to 26 Week;  
 a to z : 27 to 52 Week; z Represents  
 52 and 53 Week  
X : Internal Code

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**W-QFN4040-24 (Type A1)**

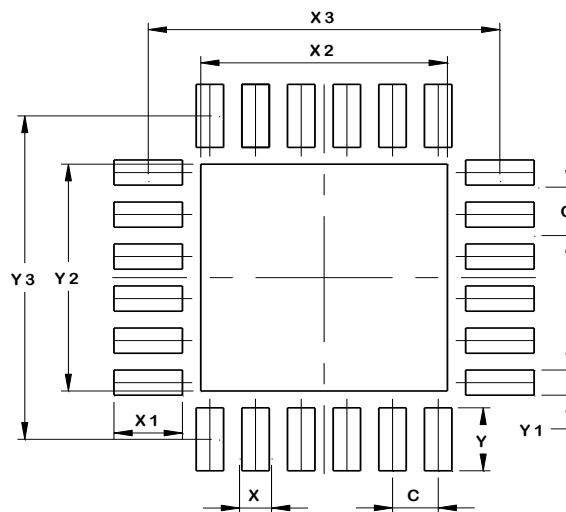


| W-QFN4040-24<br>(Type A1) |           |      |      |
|---------------------------|-----------|------|------|
| Dim                       | Min       | Max  | Typ  |
| A                         | 0.70      | 0.80 | 0.75 |
| A1                        | 0.00      | 0.05 | 0.02 |
| A3                        | 0.203 REF |      |      |
| b                         | 0.18      | 0.30 | 0.25 |
| D                         | 4.00 BSC  |      |      |
| D2                        | 2.65      | 2.75 | 2.70 |
| E                         | 4.00 BSC  |      |      |
| E2                        | 2.65      | 2.75 | 2.70 |
| e                         | 0.50 BSC  |      |      |
| k                         | 0.20      | --   | --   |
| L                         | 0.35      | 0.45 | 0.40 |
| All Dimensions in mm      |           |      |      |

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**W-QFN4040-24 (Type A1)**



| Dimensions | Value<br>(in mm) |
|------------|------------------|
| C          | 0.500            |
| X          | 0.300            |
| X1         | 0.750            |
| X2         | 2.700            |
| X3         | 3.850            |
| Y          | 0.750            |
| Y1         | 0.300            |
| Y2         | 2.700            |
| Y3         | 3.850            |

## Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin Plated Leads, Solderable per J-STD-202 ②③
- Weight: 0.041 grams (Approximate)

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