BROADCOM®

Preliminary Data Sheet

QCPL-WB3N

3.5/4 Amp Output Current IGBT Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched SO6

Description

The Broadcom® QCPL-WB3N contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving IGBT with ratings up to 1200V/200A. For IGBTs with higher ratings, this optocoupler can be used to drive a discrete power stage, which drives the IGBT gate. The QCPL-WB3N has the highest insulation voltage V_{IORM} = 1140 V_{peak}, in the IEC/EN/DIN EN 60747-5-5.

Features

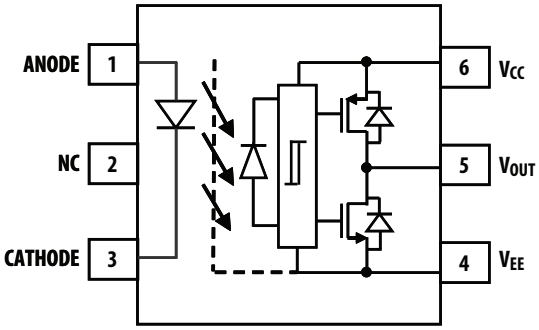
- 4.0-A maximum peak output current (105°C)
- 3.5-A maximum peak output current (125°C)
- 3.0-A minimum peak output current
- Rail-to-rail output voltage
- 200-ns maximum propagation delay
- 100-ns maximum propagation delay difference
- LED current input with hysteresis
- 35 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500V
- I_{CC} = 3.0 mA maximum supply current
- Under voltage lock-out protection (UVLO) with hysteresis
- Wide operating V_{CC} range: 15V to 30V
- Industrial temperature range: –40°C to 125°C
- Safety approval:
  - UL Recognized 5000 V_{RMS} for 1 min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1140 V_{peak}

Applications

- IGBT/MOSFET gate drive
- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial inverters
- Switching power supplies

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Diagram



NOTE: A 1-µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	$V_{CC} - V_{EE}$ "POSITIVE GOING" (that is, TURN-ON)	$V_{CC} - V_{EE}$ "NEGATIVE GOING" (that is, TURN-OFF)	V_O
OFF	0–30 V	0–30 V	LOW
ON	0–12.1 V	0–11.1 V	LOW
ON	12.1–13.5 V	11.1–12.4 V	TRANSITION
ON	13.5–30 V	12.4–30 V	HIGH

Ordering Information

QCPL-WB3N is UL Recognized with 5000 V_{RMS} for 1 minute per UL1577. (Pending).

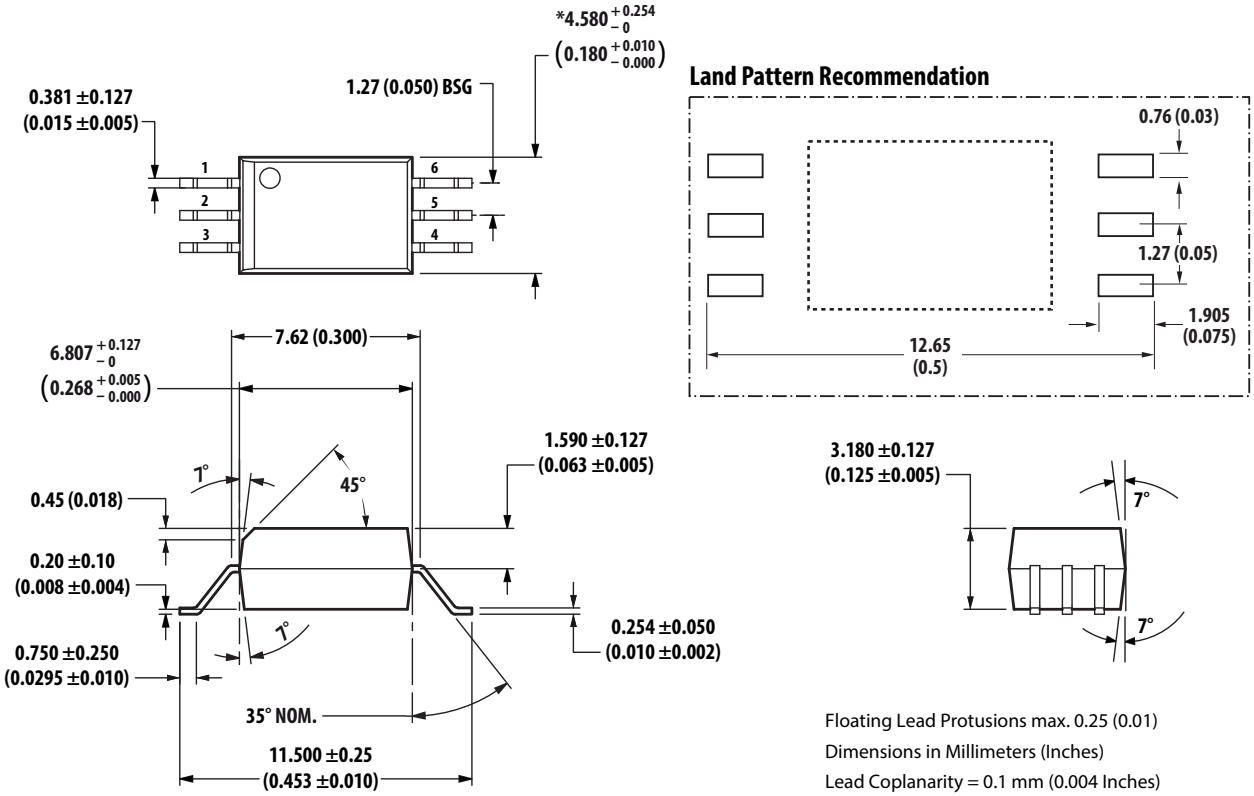
Part Number	Option: RoHS Compliant	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
QCPL-WB3N	-560E	Stretched SO-6	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings

QCPL-WB3N Stretched SO-6 Package (8-mm Clearance)



Floating Lead Protusions max. 0.25 (0.01)
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004 Inches)
* Total package length (inclusive of mold flash)
4.834 ± 0.254 (0.190 ± 0.010)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The QCPL-WB3N is pending approval by the following organizations:

- UL
  Recognized under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}.
- CSA
  CSA Component Acceptance Notice #5, File CA 88324
- IEC/EN/DIN EN 60747-5-5 (Option 060 Only)
  Maximum working insulation voltage V_{IORM} = 1140 V_{peak}.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060 – Under Evaluation)

Description	Symbol	QCPL-WB3N Option 060	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – IV	
for rated mains voltage≤ 1000 V_{rms}		I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1s, Partial discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10s, Partial discharge < 5 pC	V_{PR}	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Broadcom Regulatory Guide to Isolation Circuits*, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for “safe electrical isolation” only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface-mount classification is Class A in accordance with CECC 00802.

Insulation and Safety-Related Specifications

Parameter	Symbol	QCPL-WB3N	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

NOTE: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended land pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques, such as grooves and ribs, that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors, such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
Output IC Junction Temperature	T_J	—	150	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage	V_R	—	5	V	
“High” Peak Output Current (105°C)	$I_{OH(PEAK)}$	—	4.0	A	b
“High” Peak Output Current (125°C)	$I_{OH(PEAK)}$	—	3.5	A	b
“Low” Peak Output Current (105°C)	$I_{OL(PEAK)}$	—	4.0	A	b
“Low” Peak Output Current (125°C)	$I_{OL(PEAK)}$	—	3.5	A	b
Total Output Supply Voltage	$(V_{CC} – V_{EE})$	0	35	V	
Input Current (Rise/Fall Time)	$t_{r(IN)} / t_{f(IN)}$	—	500	ns	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output IC Power Dissipation	P_O	—	700	mW	c
Total Power Dissipation	P_T	—	745	mW	d
Lead Solder Temperature	260° C for 10 sec., 1.6 mm below seating plane				

a. Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 µs. This value is intended to allow for component tolerances for designs with I_O peak minimum = 3.0A. See the applications section for additional details on limiting I_{OH} peak.

c. Derate linearly 110°C free-air temperature at a rate of 17.5 mW/°C.

d. Derate linearly 110° C free-air temperature at a rate of 18.6 mW/°C. The maximum LED junction temperature should not exceed 150°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Operating Temperature	T_A	–40	125	°C	
Output Supply Voltage	$(V_{CC} – V_{EE})$	15	30	V	
Input Current (ON)	$I_{F(ON)}$	7	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.8	V	

Electrical Specifications (DC)

Unless otherwise noted, all typical values are at T_A = 25°C, V_{CC} – V_{EE} = 30V, V_{EE} = Ground; all minimum and maximum specifi cations are at recommended operating conditions (T_A = –40°C to 125°C, $I_{F(ON)}$ = 7 mA to 16 mA, $V_{F(OFF)}$ = –3.6V to 0.8V, V_{EE} = Ground, V_{CC} = 15V to 30V).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Peak Output Current	I_{OH}	–1.0	–2.8	—	A	$V_O = V_{CC} – 4V$	3, 4, 20	a
		–3.0	—	—	A	$V_{CC} – V_O \le 15V$		b
Low Level Peak Output Current	I_{OL}	1.0	3.5	—	A	$V_O = V_{EE} + 2.5V$	6, 7, 21	a
		3.0	—	—	A	$V_O – V_{EE} \le 15V$		c
High Output Transistor RDS(ON)	$R_{DS,OH}$	—	1.4	2.5	Ω	I_{OH} = –3.0A	8	d
Low Output Transistor RDS(ON)	$R_{DS,OL}$	—	0.6	1.5	Ω	I_{OL} = 3.0A	9	d
High Level Output Voltage	V_{OH}	V_{CC} – 0.3	V_{CC} – 0.2	—	V	I_O = –100 mA	2, 4, 22	e, f
High Level Output Voltage	V_{OH}	—	V_{CC}	—	V	I_O = 0 mA, I_F = 10 mA	1	
Low Level Output Voltage	V_{OL}	—	0.1	0.2	V	I_O = 100 mA	5, 7, 23	
High Level Supply Current	I_{CCH}	—	1.9	3.0	mA	Rg = 10Ω, Cg = 25 nF, I_F = 10 mA	10, 11	
Low Level Supply Current	I_{CCL}	—	1.9	3.0	mA	Rg = 10Ω, Cg = 25 nF, V_F = 0V		
Threshold Input Current Low to High	I_{FLH}	—	1.5	4.0	mA	Rg = 10Ω, Cg = 25 nF, V_O > 5V	12, 13, 24	
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V			
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 10 mA	19	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.7	—	mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 100 µA		
Input Capacitance	C_{IN}	—	70	—	pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	12.1	12.8	13.5	V	V_O > 5V, I_F = 10 mA	25	
	V_{UVLO-}	11.1	11.8	12.4				
UVLO Hysteresis	$UVLO_{HYS}$	—	1.0	—	V			

a. Maximum pulse width = 50 µs.

b. Output is sourced at –3.0A with a maximum pulse width = 10 µs. $V_{CC} – V_O$ is measured to ensure 15V or below.

c. Output is sourced at 3.0A with a maximum pulse width = 10 µs. $V_O – V_{EE}$ is measured to ensure 15V or below.

d. Output is sourced at –3.0A/3.0A with a maximum pulse width = 10 µs.

e. In this test, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches 0 amps.

f. Maximum pulse width = 1 ms.

Switching Specifications (AC)

Unless otherwise noted, all typical values are at T_A = 25°C, V_{CC} – V_{EE} = 30V, V_{EE} = Ground; all minimum and maximum specifications are at recommended operating conditions (T_A = –40°C to 125°C, $I_{F(ON)}$ = 7 mA to 16 mA, $V_{F(OFF)}$ = –3.6V to 0.8V, V_{EE} = Ground, V_{CC} = 15V to 30V).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	50	98	200	ns	R_g = 10Ω, C_g = 25 nF, f = 20 kHz, Duty Cycle = 50%, I_F = 7 mA to 16 mA, V_{CC} = 15V to 30V	14, 15, 16, 17, 18, 26	
Propagation Delay Time to Low Output Level	t_{PHL}	50	95	200	ns			
Pulse Width Distortion	PWD	—	22	70	ns			a
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} – t_{PLH})	–100	—	100	ns		33, 34	b
Rise Time	t_R	—	43	—	ns	V_{CC} = 30V	26	
Fall Time	t_F	—	40	—	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	35	50	—	kV/µs	T_A = 25°C, I_F = 10 mA, V_{CC} = 30V, V_{CM} = 1500V with split resistors	27	c, d
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	35	50	—	kV/µs	T_A = 25°C, V_F = 0V, V_{CC} = 30V, V_{CM} = 1500V with split resistors		c, e

a. Pulse Width Distortion (PWD) is defi ned as $|t_{PHL} - t_{PLH}|$ for any given device.

b. The diff erence between t_{PHL} and t_{PLH} between any two QCPL-WB3N parts under the same test condition.

c. Pin 2 must be connected to LED common.

d. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (that is, V_O > 15.0V).

e. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (that is, V_O < 1.0V).

Package Characteristics

Unless otherwise noted, all typical values are at T_A = 25°C; all minimum/maximum specifications are at recommended operating conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	5000	—	—	V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		b, c
Input-Output Resistance	R_{I-O}	—	$> 50^{12}$	—	Ω	V_{I-O} = 500 V_{DC}		b
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f =1 MHz		
LED-to-Ambient Thermal Resistance	R_{11}	—	135	—	°C/W			d
LED-to-Detector Thermal Resistance	R_{12}	—	27	—				
Detector-to-LED Thermal Resistance	R_{21}	—	39	—				
Detector-to-Ambient Thermal Resistance	R_{22}	—	47	—				

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

b. The device is considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.

c. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≤ 6000 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} < 5 μA).

d. The device was mounted on a high conductivity test board as per JEDEC 51-7.

Figure 1: High Output Rail Voltage vs. Temperature

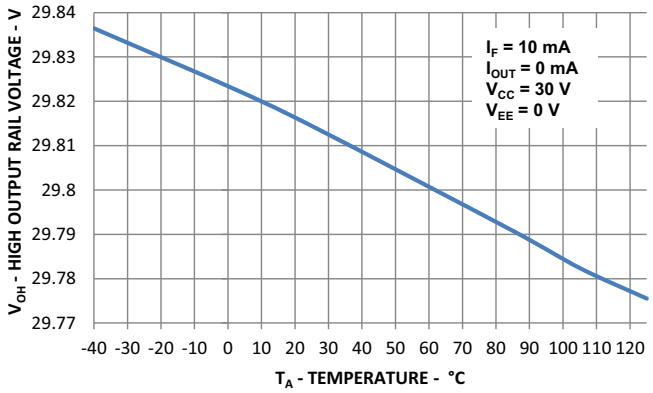


Figure 2: V_{OH} vs. Temperature

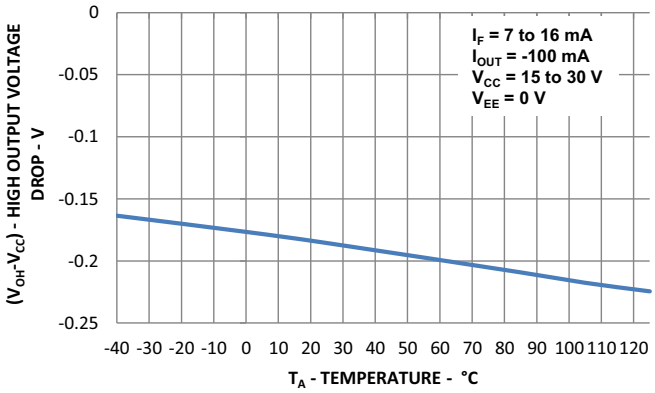


Figure 3: I_{OH} vs. Temperature

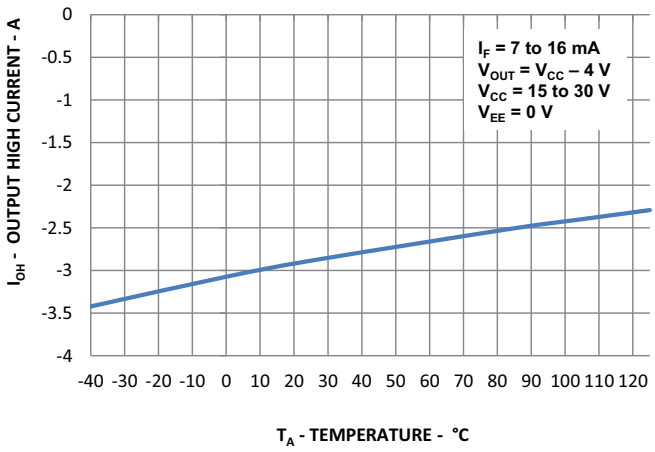


Figure 4: I_{OH} vs. V_{OH}

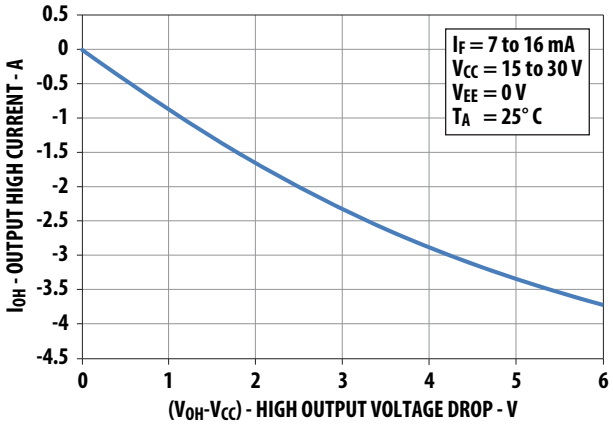


Figure 5: V_{OL} vs. Temperature

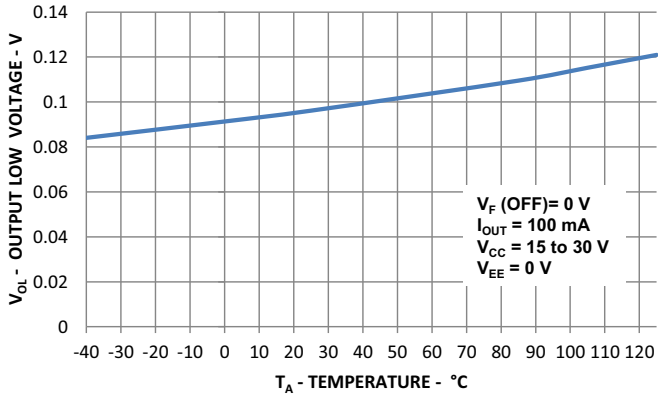


Figure 6: I_{OL} vs. Temperature

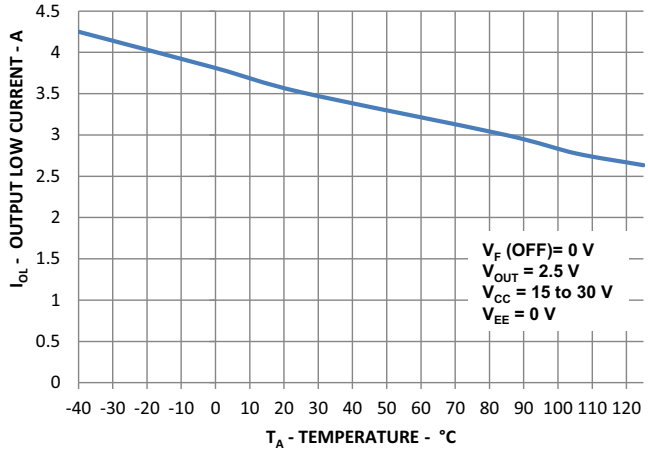


Figure 7: I_{OL} vs. V_{OL}

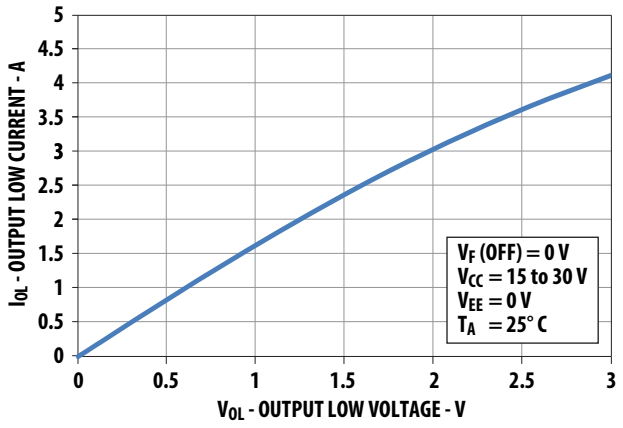


Figure 8: $R_{DS,OH}$ vs. Temperature

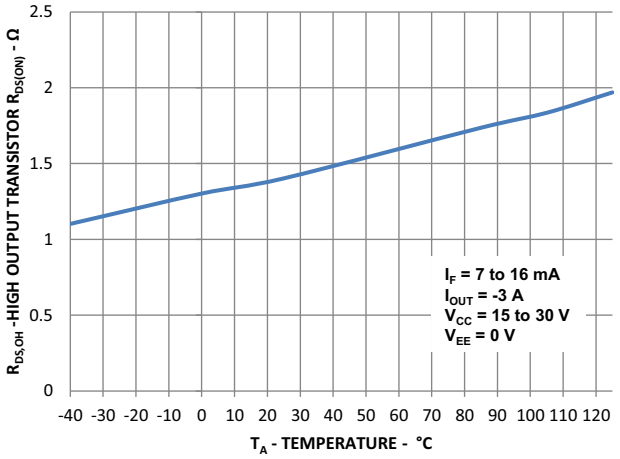


Figure 9: $R_{DS,OL}$ vs. Temperature

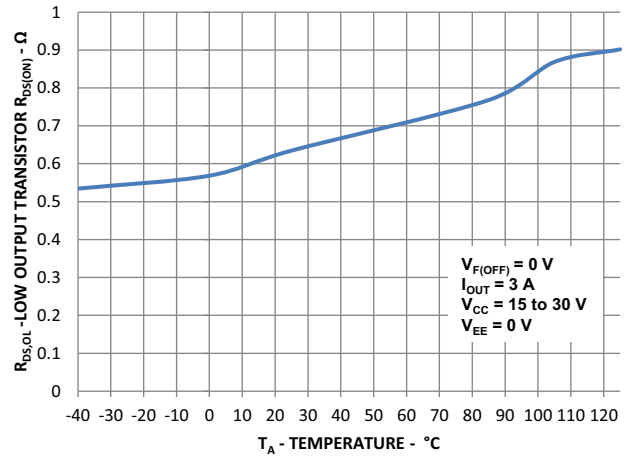


Figure 10: I_{CC} vs. Temperature

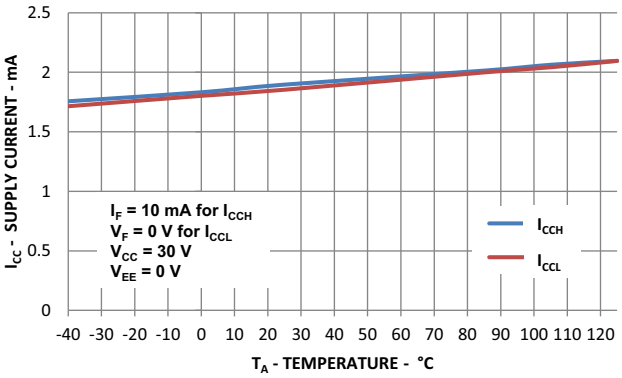


Figure 11: I_{CC} vs. V_{CC}

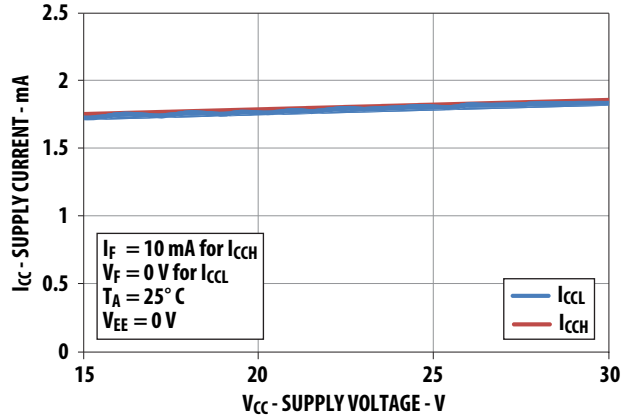


Figure 12: I_{FLH} Hysteresis

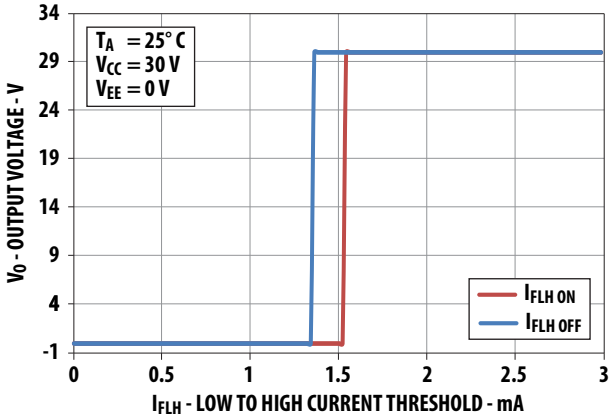


Figure 13: I_{FLH} vs. Temperature

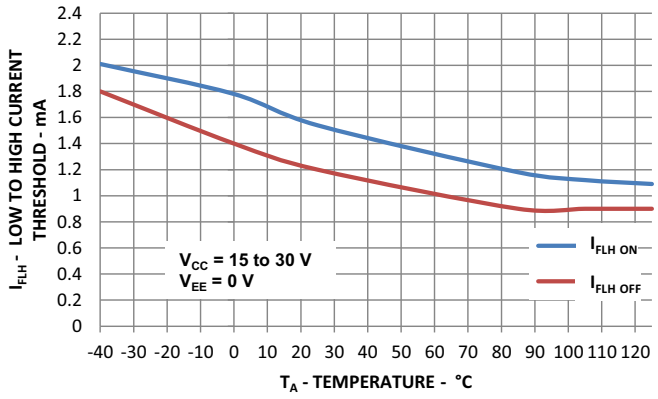


Figure 14: Propagation Delays vs. V_{CC}

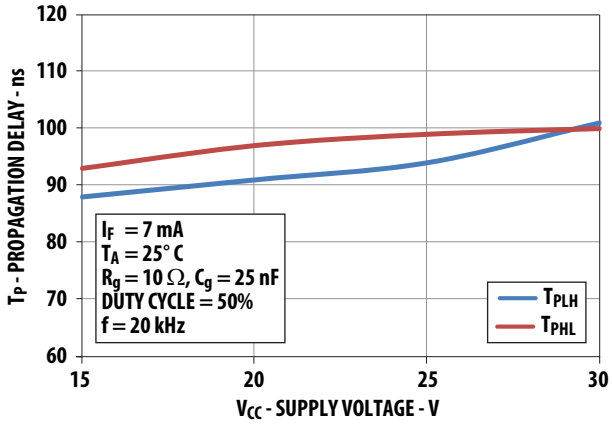


Figure 15: Propagation Delays vs. I_F

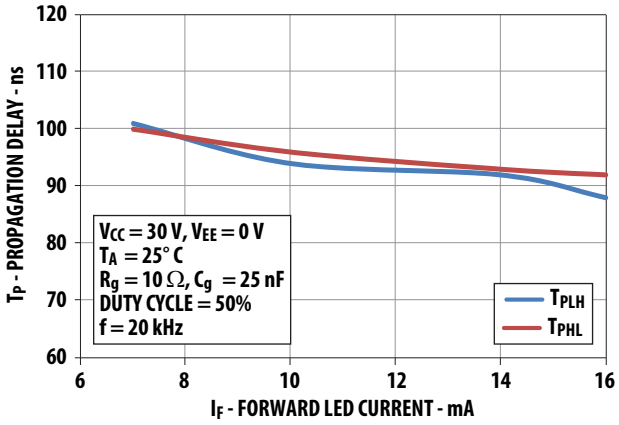


Figure 16: Propagation Delays vs. Temperature

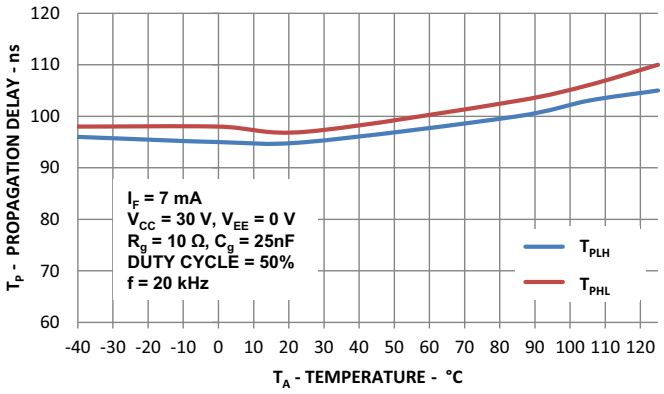


Figure 17: Propagation Delay vs. Rg

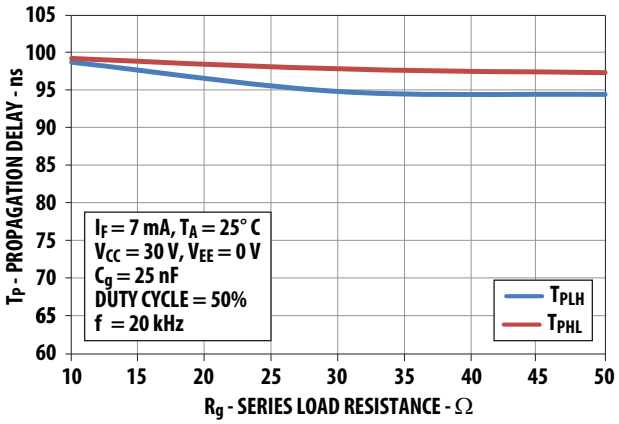


Figure 18: Propagation Delay vs. Cg

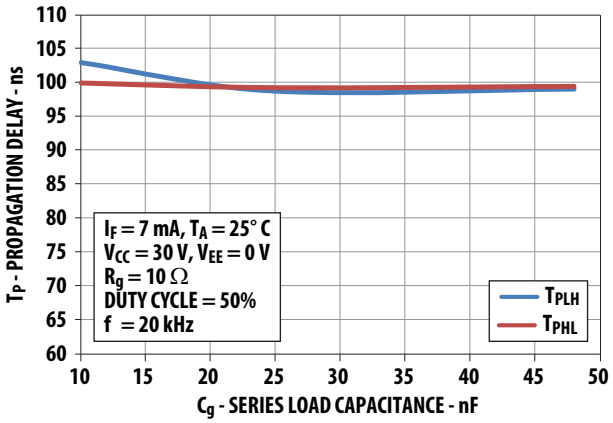


Figure 19: Input Current vs. Forward Voltage

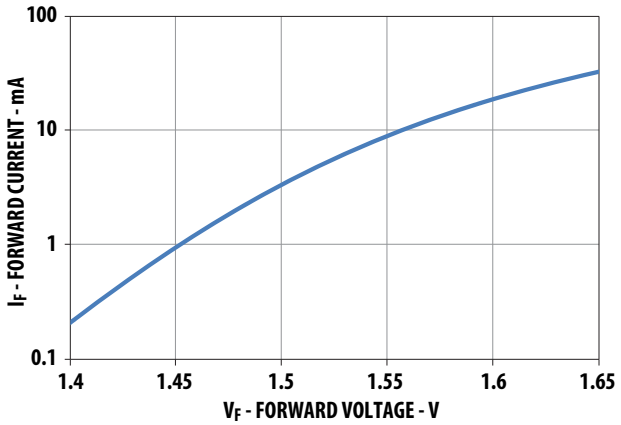


Figure 20: I_{OH} Test Circuit

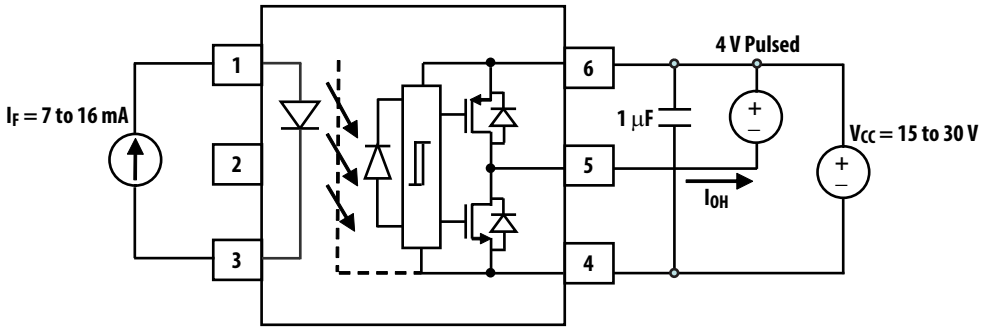


Figure 21: I_{OL} Test Circuit

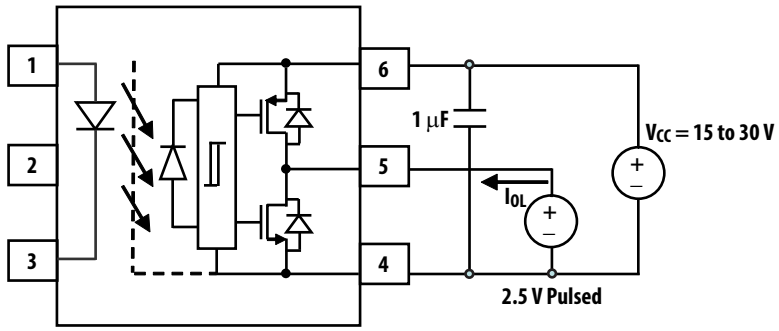


Figure 22: V_{OH} Test Circuit

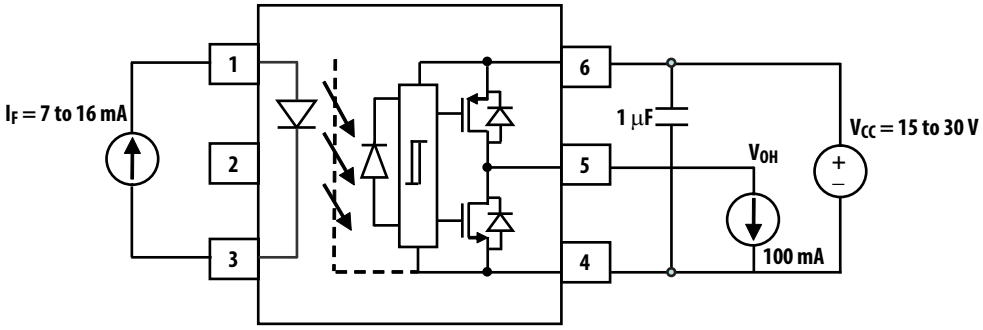


Figure 23: V_{OL} Test Circuit

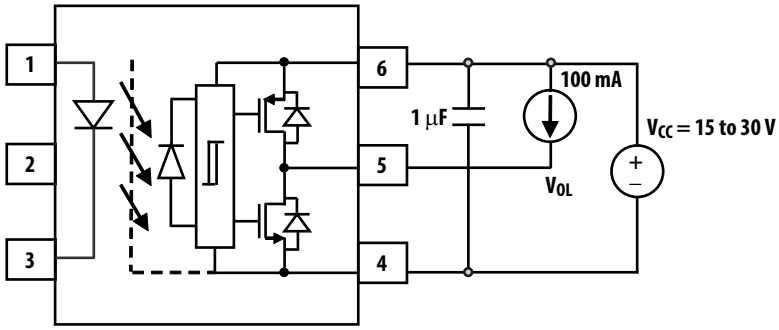


Figure 24: I_{FLH} Test Circuit

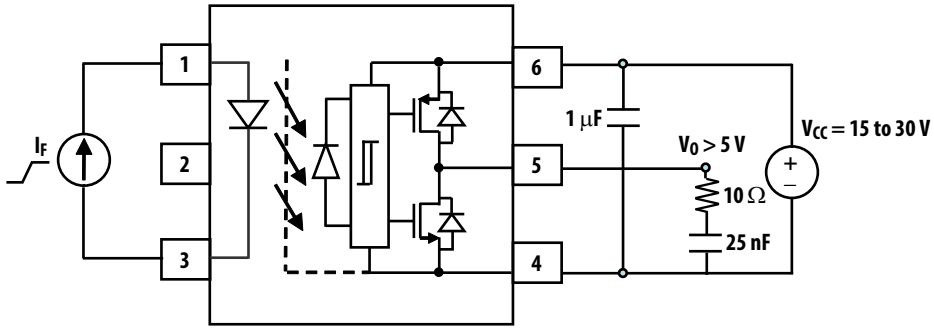


Figure 25: UVLO Test Circuit

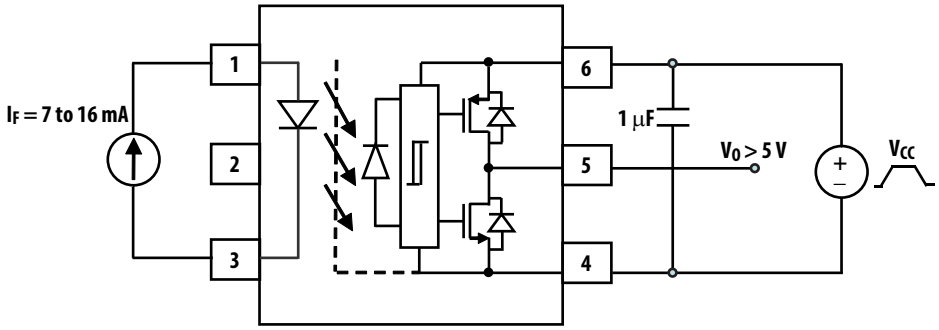


Figure 26: t_{PHL}, t_{PHL}, t_r and t_f Test Circuit and Waveforms

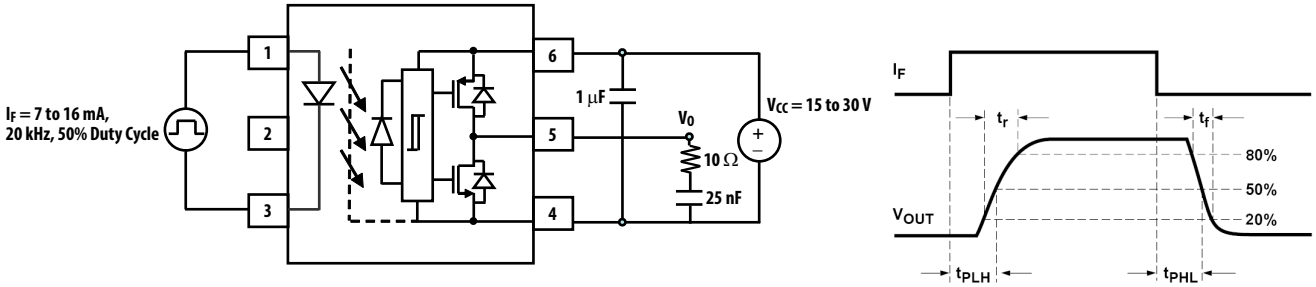
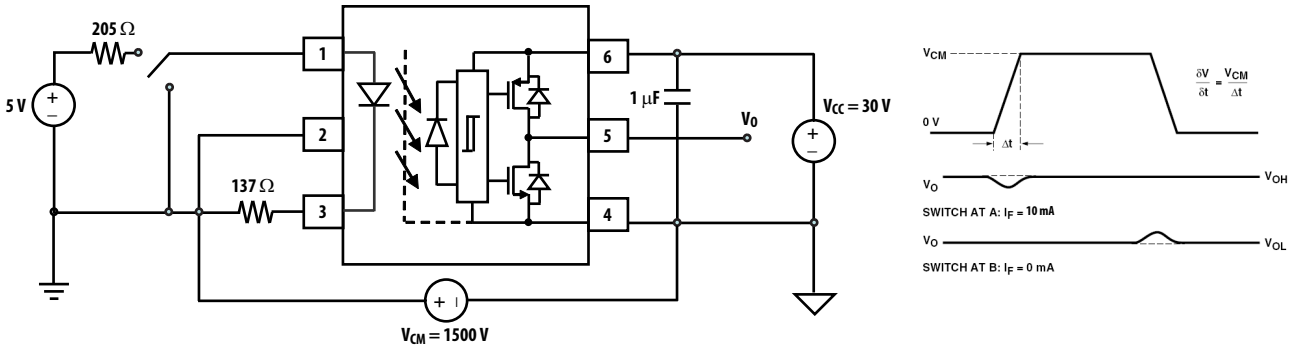


Figure 27: CMR Test Circuit with Split Resistors Network and Waveforms



Application Information

Product Overview Description

The QCPL-WB3N is an optically isolated power output stage capable of driving IGBTs of up to 200A and 1200V. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage performance and two times faster speed than the previous generation products.

The high peak output current and short propagation delay are needed for fast IGBT switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the IGBT's gate voltage is driven to the optimum intended level with no power loss across IGBT. This helps the designer lower the system power which is suitable for bootstrap power supply operation.

It has very high CMR (common mode rejection) rating which allows the microcontroller and the IGBT to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This will eliminates the need of additional Schmitt trigger circuit at the input LED.

The stretched SO6 package which is up to 50% smaller than conventional DIP package facilitates smaller more compact design. These stretched packages are compliant to many industrial safety standards, such as IEC/EN/DIN EN 60747-5-5, UL 1577, and CSA.

Recommended Application Circuit

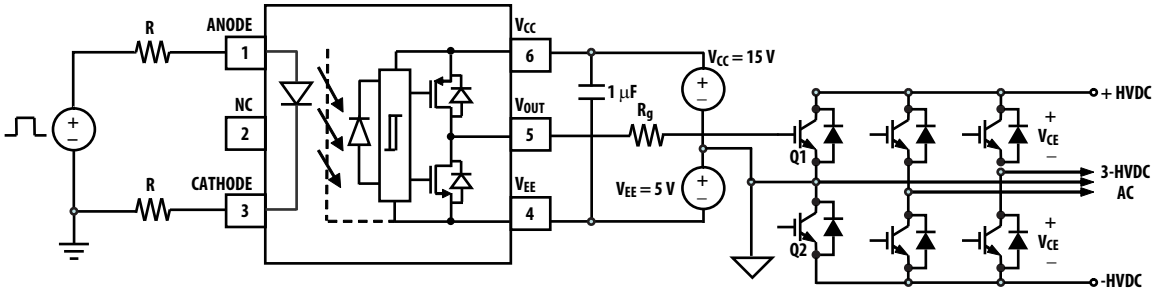
The recommended application circuit shown in Figure 28 illustrates a typical gate drive implementation using the QCPL-WB3N. The following describes about driving IGBT. However, it is also applicable to MOSFET. Designers will need to adjust the V_{CC} supply voltage, depending on the MOSFET or IGBT gate threshold requirements (recommended V_{CC} = 15V for IGBT and 12V for MOSFET).

The supply bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (3.0 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1.5:1) across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

The gate resistor R_G serves to limit gate charge current and controls the IGBT collector voltage rise and fall times.

In PC board design, care should be taken to avoid routing the IGBT collector or emitter traces close to the QCPL-WB3N input as this can result in unwanted coupling of transient signals into QCPL-WB3N and degrade performance.

Figure 28: Recommended Application Circuit with Split Resistors LED Drive



Rail-to-Rail Output

Figure 29 shows a typical gate driver's high current output stage with three bipolar transistors in darlington configuration. During the output high transition, the output voltage rises rapidly to within three diode drops of V_{CC}. To ensure the V_{OUT} is at V_{CC} to achieve IGBT rated $V_{CE(ON)}$ voltage. The level of V_{CC} will need to be raised to beyond $V_{CC}+3(V_{BE})$ to account for the diode drops. And to limit the output voltage to V_{CC}, a pull-down resistor, $R_{PULL-DOWN}$ between the output and V_{EE} is recommended to sink a static current while the output is high.

QCPL-WB3N uses a power PMOS to deliver the large current and pull it to V_{CC} to achieve rail-to-rail output voltage as shown in Figure 30. This ensures that the IGBT's gate voltage is driven to the optimum intended level with no power loss across IGBT even when an unstable power supply is used.

Figure 29: Typical Gate Driver with Output Stage in Darlington Confi guration

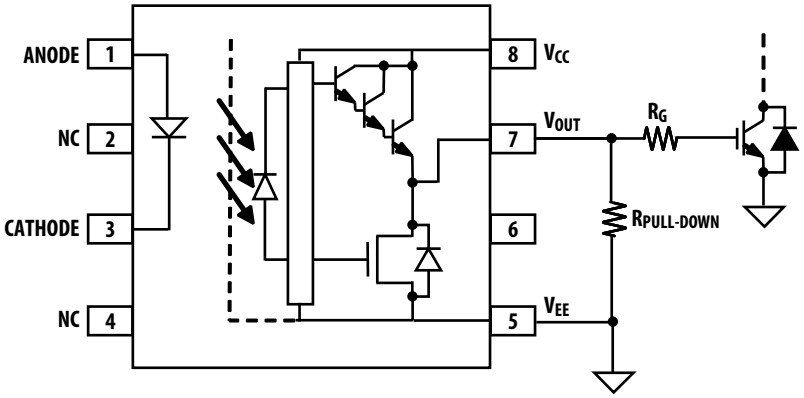
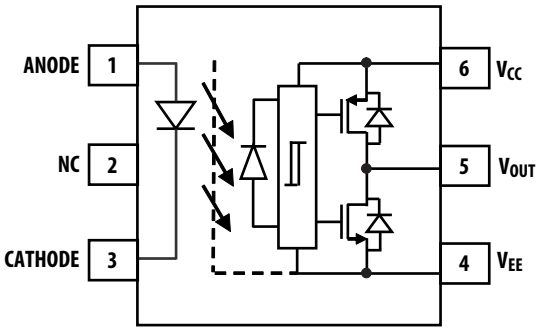


Figure 30: QCPL-WB3N with PMOS and NMOS Output Stage for Rail-to-Rail Output Voltage



Selecting the Gate Resistor (Rg)

Step 1: Calculate Rg minimum from the IOL peak specification. The IGBT and Rg in Figure 28 can be analyzed as a simple RC circuit with a voltage supplied by QCPL-WB3N.

$Rg \geq (V_{CC} - V_{EE} - V_{OL}) / I_{OLPEAK}$

$= (15V + 5V - 2.5V) / 3.5A$

$= 5\Omega$

The V_{OL} value of 2.5V in the previous equation is the V_{OL} at the peak current of 3.5A (see Figure 7).

Step 2: Check the QCPL-WB3N power dissipation and increase Rg if necessary. The QCPL-WB3N total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$PT = P_E + P_O$

$PE = I_F \times V_F \times \text{Duty Cycle}$

$PO = P_{O(BIAS)} + P_{O(SWITCHING)}$

$= I_{CC} \times (V_{CC} - V_{EE}) + E_{SW}(Rg;Cg) \times f$

Using I_F(worst case) = 16 mA, Rg = 5Ω, Max Duty Cycle = 80%, Cg = 25 nF, f = 25 kHz and T_A max = 125°C:

$PE = 16\ mA \times 1.95V \times 0.8 = 25\ mW$

$PO = 3\ mA \times 20V + 5\ mJ \times 25\ kHz$

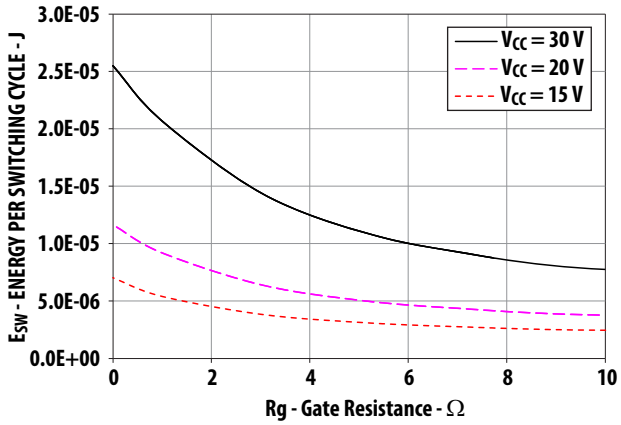
$= 60\ mW + 125\ mW$

$= 185\ mW < 437.5\ mW\ (P_{O(MAX)}\ @\ 125°C)$

The value of 3 mA for I_{CC} in the previous equation is the maximum I_{CC} over the entire operating temperature range.

Because P_O is less than $P_{O(MAX)}$, Rg = 5Ω is alright for the power dissipation.

Figure 31: Energy Dissipated in the QCPL-WB3N for Each IGBT Switching Cycle



LED Drive Circuit Considerations for High CMR Performance

Figure 32 shows the recommended drive circuit for the QCPL-WB3N that gives optimum common-mode rejection. The two current setting resistors balance the common mode impedances at the LED's anode and cathode. Common-mode transients can be capacitive coupled from the LED anode, through CL_A (or cathode through CL_C) to the output-side ground causing current to be shunted away from the LED (which is not wanted when the LED should be on) or conversely cause current to be injected into the LED (which is not wanted when the LED should be off).

Table 1 shows the directions of I_{LP} and I_{LN} depend on the polarity of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CM_H, since the output is at "high" state) depends on LED current (I_F). For conditions where I_F is close to the switching threshold (I_{FLH}), CM_H also depends on the extent to which I_{LP} and I_{LN} balance each other. In other words, any condition where a common-mode transient causes a momentary decrease in I_F (that is, when $dV_{CM}/dt > 0$ and $|I_{LP}| > |I_{LN}|$, referring to Table 1) will cause a common-mode failure for transients which are fast enough.

Likewise for a common-mode transient that occurs when the LED is off (that is, CM_L, since the output is at "low" state), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient "signal" may cause the output to spike above 1V, which constitutes a CM_L failure. The balanced I_{LED}-setting resistors help equalize the common mode voltage change at the anode and cathode. The shunt drive input circuit will also help to achieve high CM_L performance by shunting the LED in the off state.

Figure 32: Recommended High-CMR Drive Circuit for the QCPL-WB3N

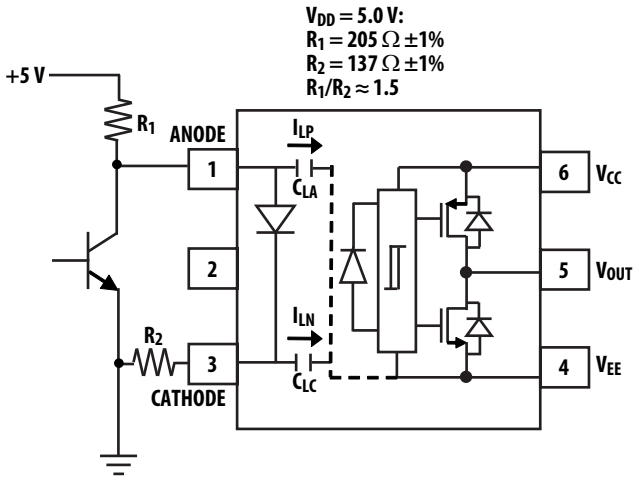


Table 1: Common Mode Pulse Polarity and LED Current Transients

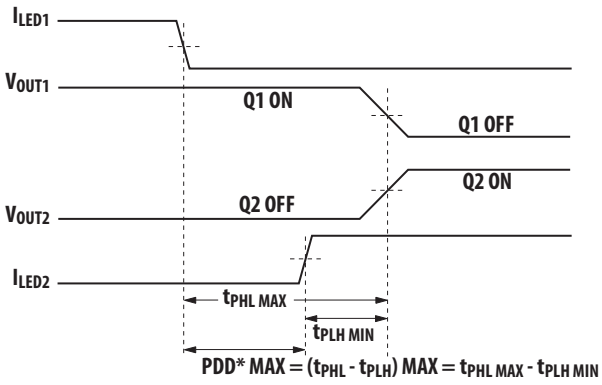
dV_{CM}/dt	I_{LP} Direction	I_{LP} Direction	If $\|I_{LP}\| < \|I_{LN}\|$, I_F Is Momentarily	If $\|I_{LP}\| > \|I_{LN}\|$, I_F Is Momentarily
Positive (>0)	Away from LED anode through CLA	Away from LED cathode through CLC	Increase	Decrease
Negative(<0)	Toward LED anode through CLA	Toward LED cathode through CLC	Decrease	Increase

Dead Time and Propagation Delay Specifications

The QCPL-WB3N includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 28) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 33. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 100 ns over the operating temperature range of 40°C to 125°C.

Figure 33: Minimum LED Skew for Zero Dead Time

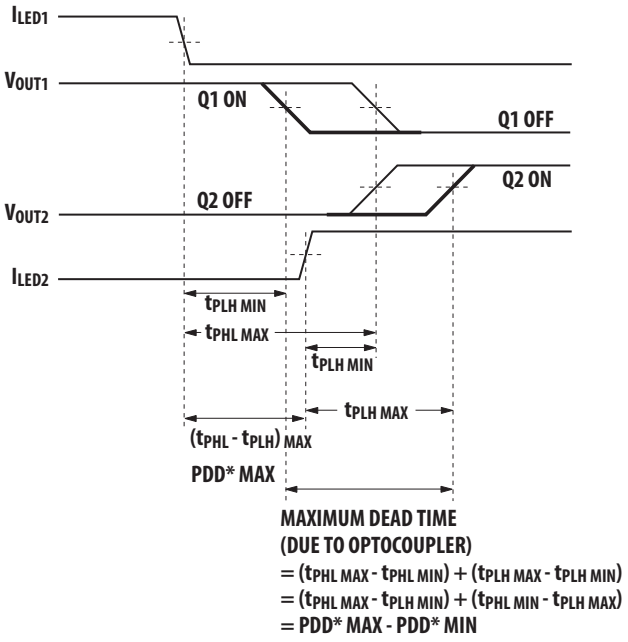


*PDD = Propagation Delay Difference
Note: for PDD calculations the propagation delays
Are taken at the same temperature and test conditions.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 34. The maximum dead time for the QCPL-WB3N is 200 ns (= 100 ns – (–100 ns)) over an operating temperature range of –40°C to 125°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

Figure 34: Waveforms for Dead Time



*PDD = Propagation Delay Difference
Note: For Dead Time and PDD calculations all propagation delays are taken at the same temperature and test conditions.

LED Current Input with Hysteresis

The detector has optical receiver input stage with built in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 12) provides differential mode noise immunity and minimizes the potential for output signal chatter.

Under Voltage Lockout

The QCPL-WB3N Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the QCPL-WB3N output low during power-up. IGBTs typically require gate voltages of 15V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 13V typically, the $V_{CE(ON)}$ voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply (V_{CC}) is applied. Once V_{CC} exceeds V_{UVLO+} (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals.

Thermal Model for QCPL-WB3N Stretched SO6 Package Optocoupler

Definitions

R_{11}: Junction to ambient thermal resistance of LED due to heating of LED.

R_{12}: Junction to ambient thermal resistance of LED due to heating of detector (output IC).

R_{21}: Junction to ambient thermal resistance of detector (output IC) due to heating of LED.

R_{22}: Junction to ambient thermal resistance of detector (output IC) due to heating of detector (output IC).

P_1: Power dissipation of LED (W).

P_2: Power dissipation of detector/output IC (W).

T_1: Junction temperature of LED (°C).

T_2: Junction temperature of detector (°C).

Ta: Ambient temperature.

Ambient Temperature

Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23°C in still air.

Thermal Resistance	°C/W
R_{11}	135
R_{12}	27
R_{21}	39
R_{22}	47

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm × 7.62 cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and detector junctions of the optocoupler can be calculated using the following equations.

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + Ta \quad (1)$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + Ta \quad (2)$$

Using the given thermal resistances and thermal model formula in this data sheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperature should be within the absolute maximum rating.

For example, given P_1 = 25 mW, P_2 = 185 mW, Ta = 125° C:

LED junction temperature,

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + Ta$

$= (135 \times 0.025 + 27 \times 0.185) + 125$

$= 133.4°$ C

Output IC junction temperature,

$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + Ta$

$= (39 \times 0.025 + 47 \times 0.185) + 125$

$= 134.7°C$

T_1 and T_2 should be limited to 150°C based on the board layout and part placement.

Related Application Notes

- AN5336 – *Gate Drive Optocoupler Basic Design for IGBT/MOSFET*
- AN1043 – *Common-Mode Noise: Sources and Solutions*
- AV02-0310EN – *Plastics Optocouplers Product ESD and Moisture Sensitivity*

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