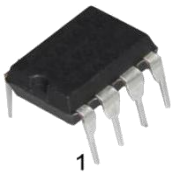
I²C-Compatible Serial E²PROM

Features

- Single Supply Voltage and High Speed Mode
  - Minimum operating voltage down to 1.7V
  - 400kHz/1 MHz clock from 1.7V to 5.5V
- Low power CMOS technology
  - Read current 0.2mA (400kHz), typical
  - Write current 0.8mA (400kHz), typical
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- Page Write Modes, Partial Page Writes Allowed
- Write protection of the whole memory array
- Additional Write Lockable Page and 128 bits Serial Number
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection (HBM): 6 kV
  - Latch up Capability: ± 200mA (25°C)
- Package: DIP8, SOP8, TSSOP8, MSOP8,DFN-8, SOT23-5


DIP-8


SOP-8


TSSOP-8


MSOP-8


DFN-8


SOT-23-5

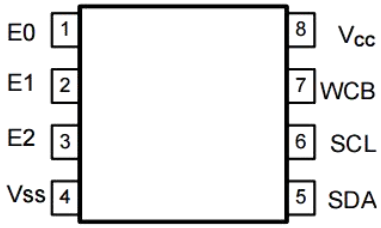
Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG24C128N	DIP-8	24C128	TUBE	2000pcs/box
HG24C128M/TR	SOP-8	24C128	REEL	2500pcs/reel
HG24C128MM/TR	MSOP-8	C128	REEL	3000pcs/reel
HG24C128MT/TR	TSSOP-8	C128	REEL	5000pcs/reel
HG24C128DQ2/TR	DFN-8 2*2	C128	REEL	4000pcs/reel
HG24C128DQ3/TR	DFN-8 3*3	C128	REEL	5000pcs/reel
HG24C128M5/TR	SOT-23-5	DBMU,C128	REEL	3000pcs/reel

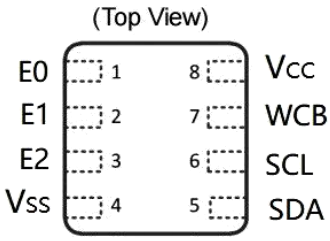
1. General Description

The HG24C128 is I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 128 Kbits (16 Kbytes), which is organized in 64 bytes per page.

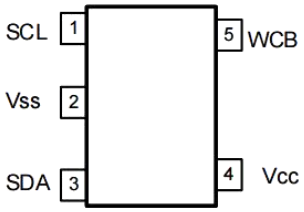
1.1 Pin Configuration



DIP-8/SOP-8/MSOP-8/TSSOP-8



DFN-8 3*3/2*2



SOT-23-5

1.2 Pin Definition

Table 1-1 Pin Definition for DIP8/SOP8/MSOP8/TSSOP8/DFN8 Packages

Pin	Name	Type	Description
1	E0	Input	Slave Address Setting
2	E1	Input	Slave Address Setting
3	E2	Input	Slave Address Setting
4	Vss	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	VCC	Power	Power

Table 1-2 Pin Definition for SOT23-5 Packages

Pin	Name	Type	Description
1	SCL	Input	Serial Clock Input
2	Vss	Ground	Ground
3	SDA	I/O	Serial Data Input and Serial Data Output
4	V_{CC}	Power	Power
5	WCB	Input	Write Control, Low Enable Write

1.3 Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-OR'ed with any number of other open-drain or open-collector devices.

Device Addresses (E2, E1, E0): The E2, E1, and E0 pins are device address inputs. Typically, the E2, E1, and E0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the E2, E1, and E0 pins will be internally pulled down to Vss.

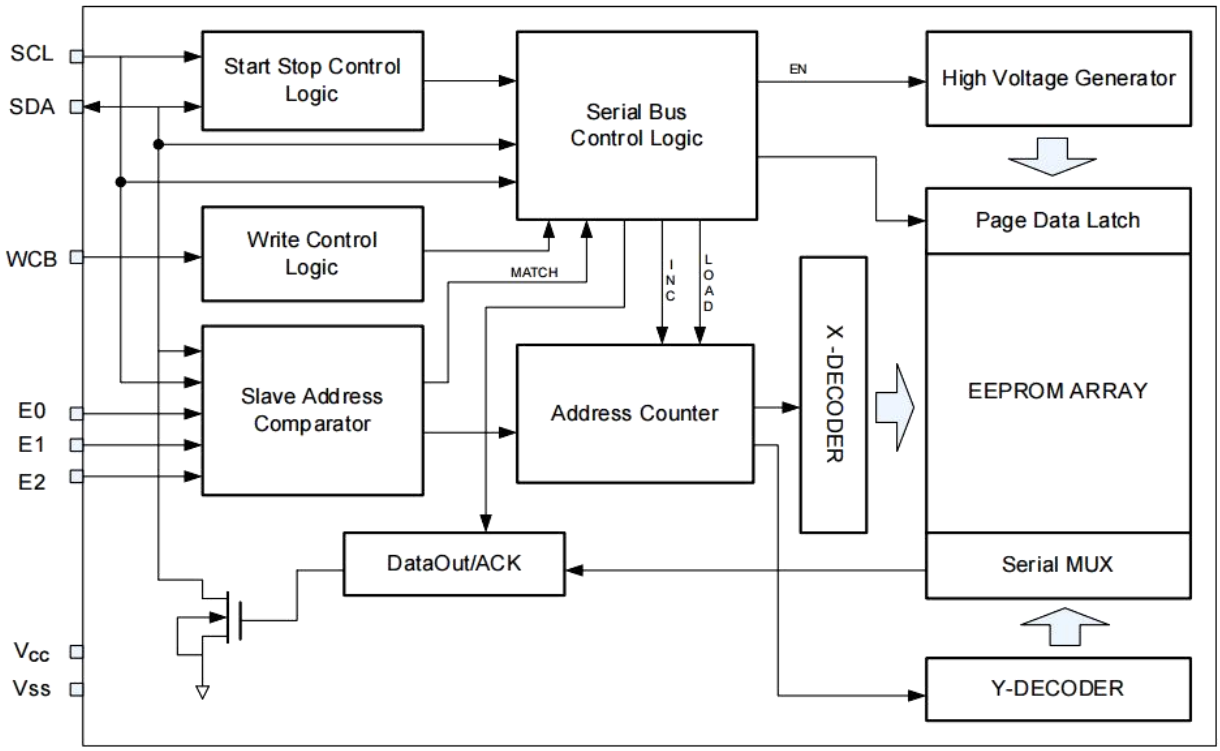
Write Control (WCB): The Write Control input, when WCB is connected directly to VCC, all write operations to the memory are inhibited. When connected to Vss, allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to Vss.

Supply Voltage (V_{CC}): V_{CC} is the supply voltage.

Ground (Vss): Vss is the reference for the V_{CC} supply voltage.

2. Block Diagram

Figure 2-1 Block Diagram



3. Electrical Characteristics

Table 3-1 Absolute Maximum Ratings [1]

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient operating temperature range [2]	-40	125	°C
V_{CC}	Supply Voltage	-0.5	6.5	V
V_{IO}	Input or output range	-0.5	6.5	V
I_{OL}	DC output current (SDA=0)	-	5	mA
T_L	Lead Temperature (Soldering, 10 seconds)	-	260	°C

Note: [1] Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
[2] Operating temperature range: -40°C to +125°C. This product is designed for industrial grade applications. For automotive grade versions compliant with AEC-Q100, please conduct internal screening per the standard or contact our sales team for availability.

Table 3-2 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$= Vss
C_{IN}	Input Capacitance (E0, E1,E2,WCB,SCL)	6	pF	V_{IN}= Vss

Note: [1] Test Conditions: T_A = 25°C, f_{SCL} = 1MHz, Vcc = 5.0V.

Table 3-3DC Characteristics

（Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 125°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	
		1.8	-	5.5	V	
		2.5	-	5.5	V	
Isb	Standby Current	-	-	1.0	μA	Vcc = 3.3V, T_A = 85°C
		-	-	2.0	μA	Vcc = 5.5V, T_A = 85°C
		-	-	3.0	μA	Vcc = 5.5V, T_A = 105°C
I_{CC1}	Supply Current	-	0.2	0.4	mA	Vcc = 5.5V, Read at 400Khz
I_{CC2}	Supply Current	-	0.8	1.6	mA	Vcc = 5.5V Write at 400Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = V_{CC} or Vss
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = V_{CC} or Vss
V_{IL}	Input Low Level	–0.5	-	0.3V_{CC}	V	
V_{IH}	Input High Level	0.7V_{CC}	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC} = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 0.15 mA
V_{OL2}	Output Low Level V_{CC} = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

Table 3-4 AC Characteristics

（Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 125°C, C_L=100pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤V_{CC}≤5.5			1.7≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	START Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	START Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.1	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	STOP Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	μs
$t_{HD.WCB}$	WCB pin Hold Time	1.2	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- R_L (connects to V_{CC}): 1.3kΩ (2.5V, 5.5V), 10kΩ (1.7V)
- Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
- Input rise and fall times: ≤50ns
- Input and output timing reference voltages: 0.5V_{CC}

Table 3-5 Reliability Characteristics [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR[2]	Endurance	1,000,000			Write cycles
DRET[3]	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

[3] Test condition: T_A = 55°C

Figure 3-1 Bus Timing

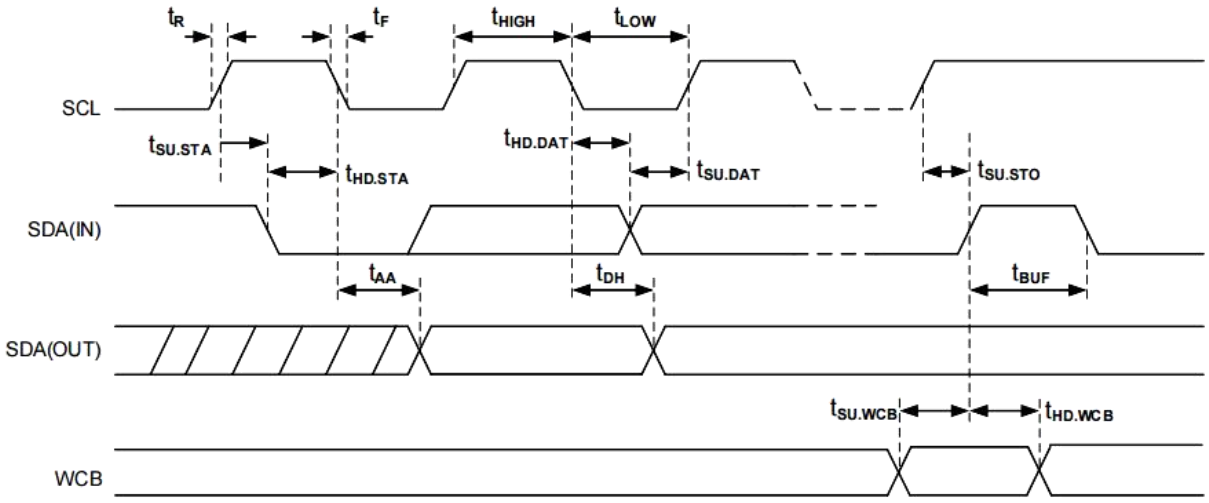
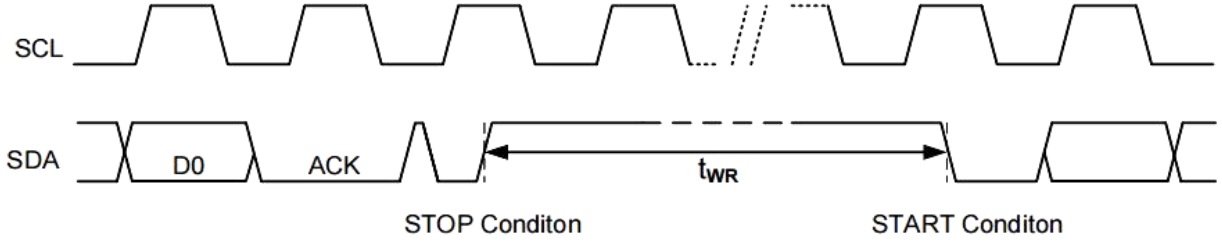


Figure 3-2 Write Cycle Timing



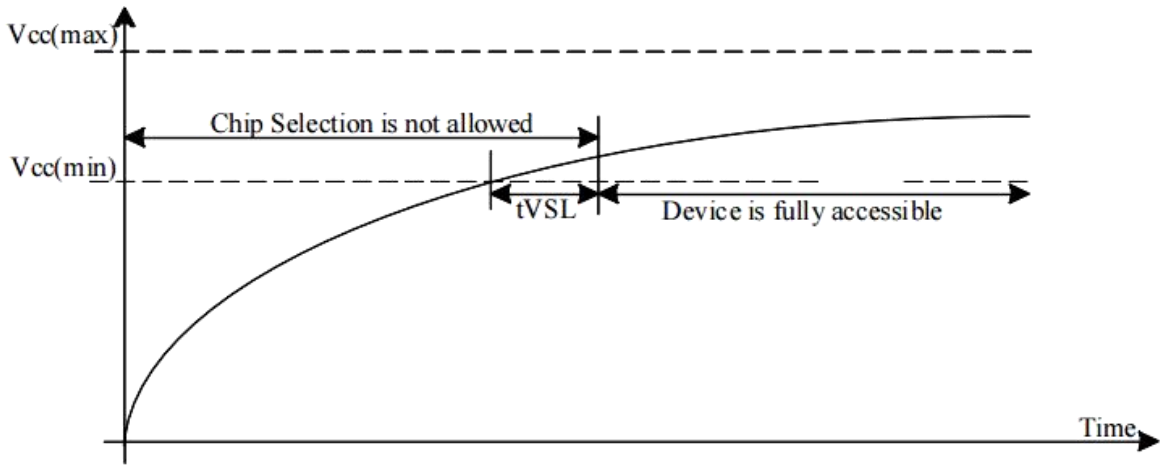
Note: [1] The write cycle time tWR is the time from a valid STOP condition of a write sequence to the end of the internal clear/write cycle.

Device Power-Up

The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status. tVSL is the time required to initialize the EEPROM. No instructions are accepted during this time.

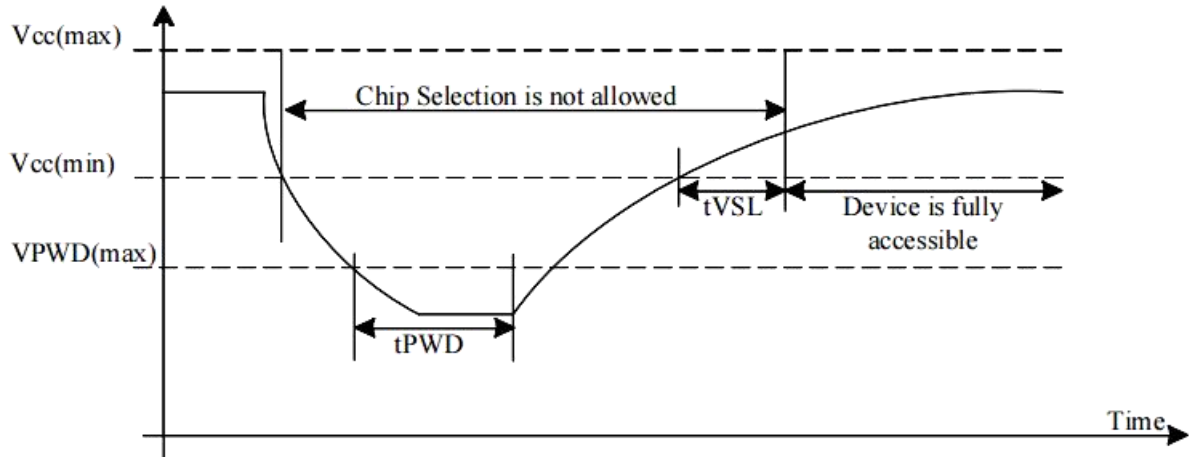
Figure 3-3 Power up Timing



Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of EEPROM device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 3-4 Power down-up Timing



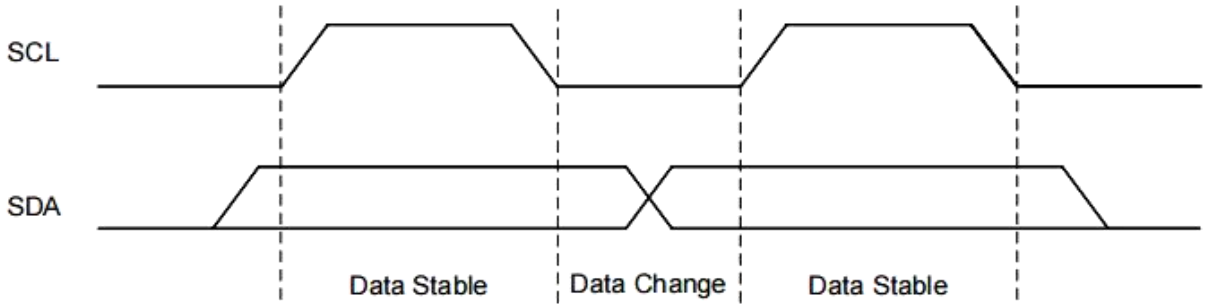
Symbol	Parameter	min	max	unit
VPWD	V_{CC} voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	V_{CC}(min.) to device operation	70		us
tVR	V_{CC} Rise Time	1	500000	us/V

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low period (Refer to Figure 4-1). Data changes during SCL high period will indicate a START or STOP condition as defined below.

Figure 4-1 Data Validity



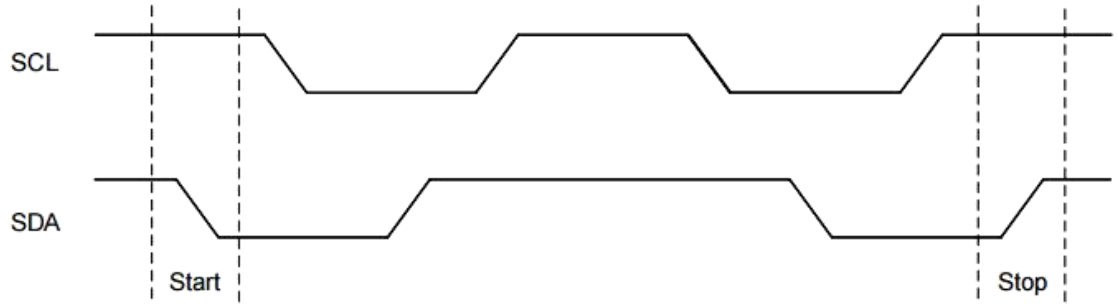
4.2 START Condition

A high-to-low transition of SDA with SCL high is a START condition which must precede any other command bits. (Refer to Figure 4-2).

4.3 STOP Condition

A low-to-high transition of SDA with SCL high is a STOP condition. After a read sequence, the STOP bit will place the HG24C128 in a standby mode (Refer to Figure 4-2).

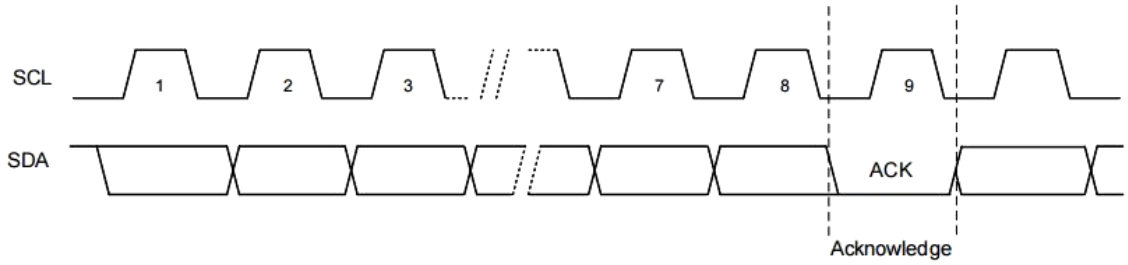
Figure 4-2 START and STOP Definition



4.4 Acknowledge (ACK)

All addresses and data are serially transmitted to and from the HG24C128 in 8-bit data. The HG24C128 sends a “0” to acknowledge that it has received each data. This happens during the ninth clock cycle.

Figure 4-3 Acknowledge Bit Definition



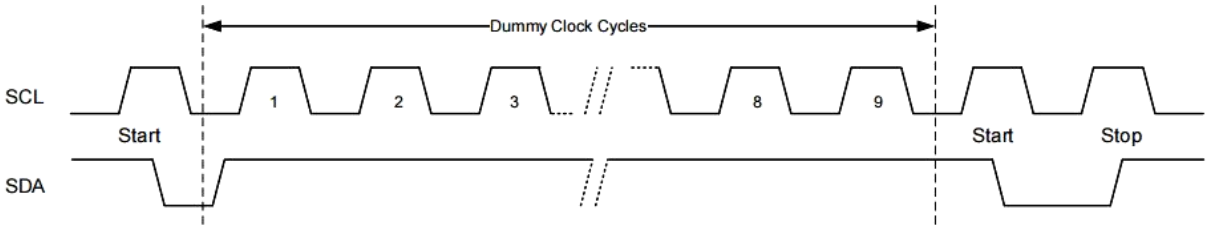
4.5 Standby Mode

The HG24C128 features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation.

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, the device can be reset by following steps: (a) Create a START condition, (b) Clock in nine data bits “1”, and (c) create another START bit followed by STOP bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.7 Device Addressing

The HG24C128 requires an 8-bit device address following a START condition to enable the chip for a read or write operation (Refer to table below). The device address consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 4-1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HG24C128	Normal Area	1	0	1	0	E2	E1	E0	R/W
	ID Page	1	0	1	1	E2	E1	E0	R/W
	Lock Bit	1	0	1	1	E2	E1	E0	R/W
	Serial Number	1	0	1	1	E2	E1	E0	1

Table 4-2 Word Address0

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HG24C128	Normal Area	X	X	A13	A12	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	X	1	X	X
	Serial Number	X	X	X	X	1	0	X	X

Table 4-3 Word Address1

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HG24C128	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	X	X	A5	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	Serial Number	X	X	X	X	A3	A2	A1	A0

The E2, E1 and E0 bits allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The E2, E1 and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating. The bit0 of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a matched comparison result, the Chip will output a zero. If not, the device will return to a standby state.

4.8 Data Security

HG24C128 has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is high.

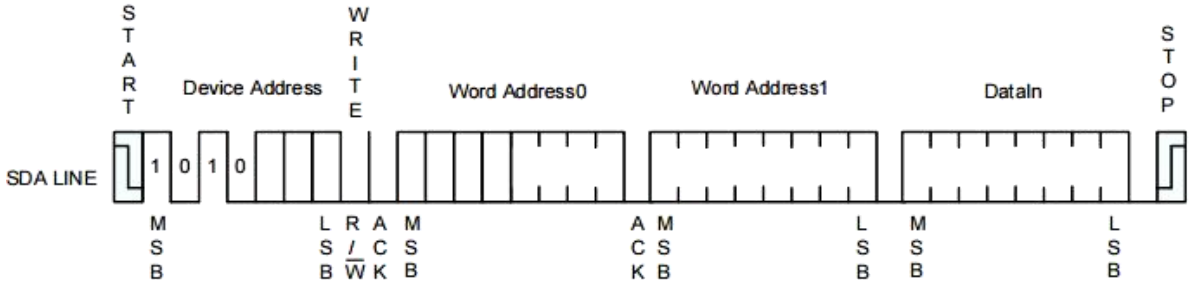
5. Instructions

5.1 Write Operations

5.1.1 Byte Write

A write operation requires an 8-bit device address following a two-byte word address and acknowledgment. Upon receipt of this device address, the HG24C128 will again respond with a “0” and then clock in the first 8-bit data. Following receipt of the 8-bit data, the HG24C128 will output a “0” and the master, such as a master, must terminate the write sequence with a STOP condition. And then the HG24C128 enters an internally timed write cycle. All inputs are disabled during this write cycle and the HG24C128 will not respond until the write is complete (Refer to Figure 5-1).

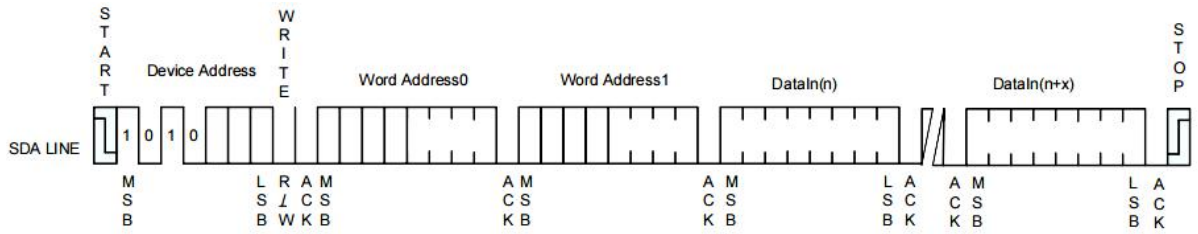
Figure 5-1 Byte Write



5.1.2 Page Write

A page write is initiated in the same way as a byte write, but the master does not send a STOP condition after the first data is clocked in. Instead, after the HG24C128 acknowledges receipt of the first data, the master can transmit more data continuously. The HG24C128 will respond with a “0” after each data byte received. The master must terminate the page write sequence with a STOP condition.

Figure 5-2 Page Write



The lowest six bits of the word address are internally incremented following the receipt of each data. The higher word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data are transmitted to the HG24C128, the word address will roll-over and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started, the HG24C128 inputs are disabled and acknowledge polling can be initiated. This involves sending a START condition followed by the device address. The read/write bit is representative of the operation desired. Until the internal write cycle has completed will the device respond “0”, allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Address bits A11~A10 must be '00'.
- Address bits A5~A0 define the byte address inside the Identification page.
- Other Address bits are don't care.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) instruction with the following specific conditions:

- Device type identifier = 1011b
- Address bit A11~A10 must be '01'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

5.2 Read Operations

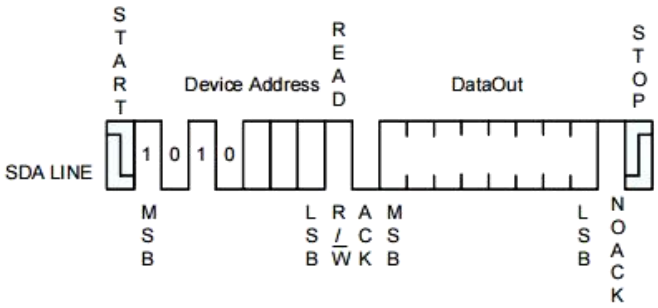
Read operations are initiated in the same way as write operations with the exception that the read/write select bit in the device address is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

The last address accessed during the last read or write operation is always incremented by one after the STOP condition of the last command. Then the Current Address Read instruction read data start from that address and increased by one after every data byte read. The address counter rolls over to the first byte of the first page if the last byte of the last memory page is encountered.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the device, the data at the current address is serially clocked out. The master does not respond with an input "0" but does generate a following STOP condition (Refer to Figure 5-3).

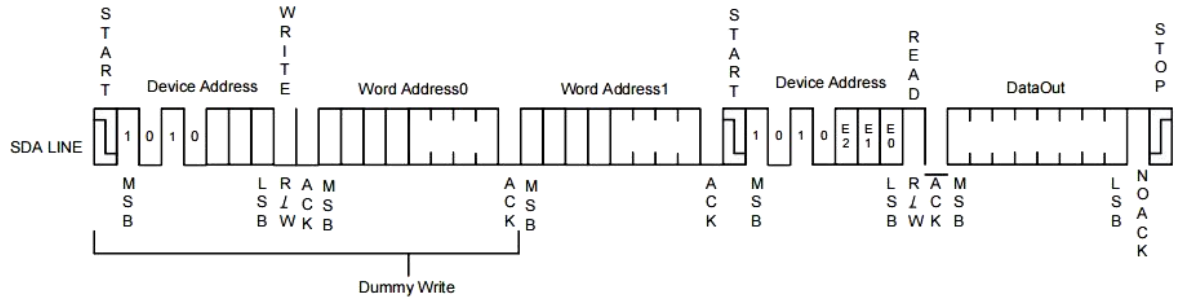
Figure 5-3 Current Address Read



5.2.2 Random Read

A Random Read requires a "dummy" byte write sequence to load in the word address. Once the device address and word address are clocked in and acknowledged by the device, the master must generate another START condition. The master now initiates a Current Address Read by sending a device address with the read/write select bit high. The device acknowledges the device address and serially clocks out the data. The master does not respond with a "0" but does generate a following STOP condition (Refer to Figure 5-4).

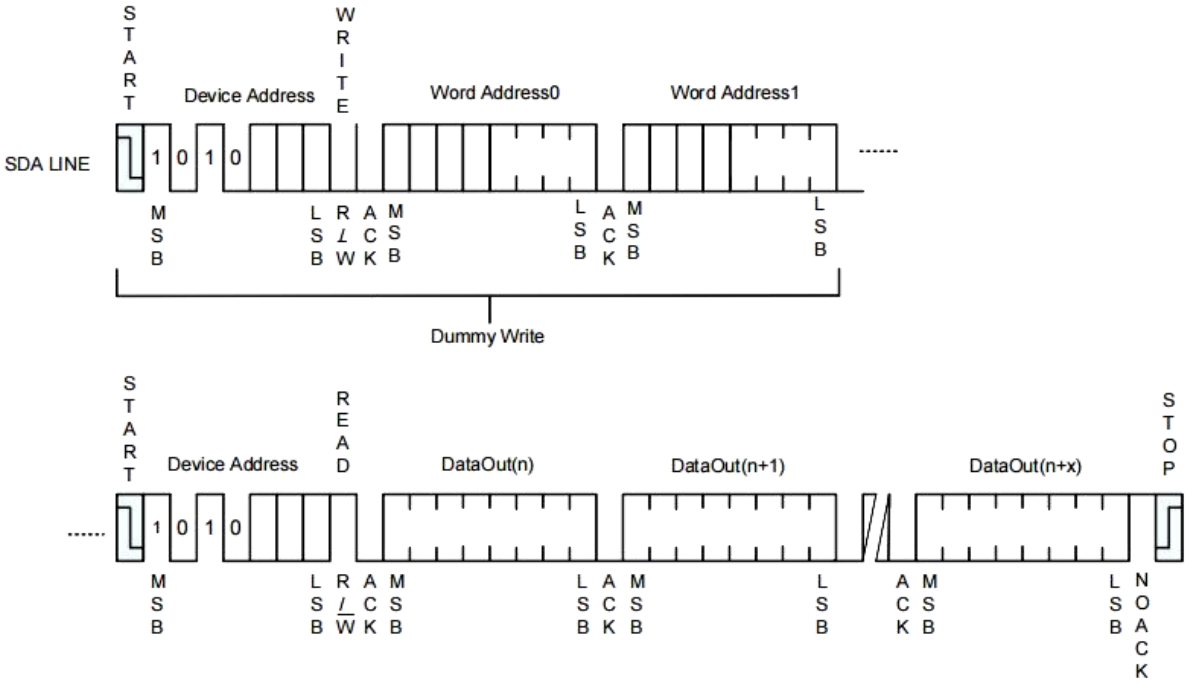
Figure 5-4 Random Read



5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the master receives a data word, it responds with acknowledge. As long as the device receives acknowledge, it will continue to increment the word address and serially clock out sequential data. When the memory address limit is reached, the word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the master does not respond with a “0” but does generate a following STOP condition (Refer to Figure 5-5)

Figure 5-5 Sequential Read



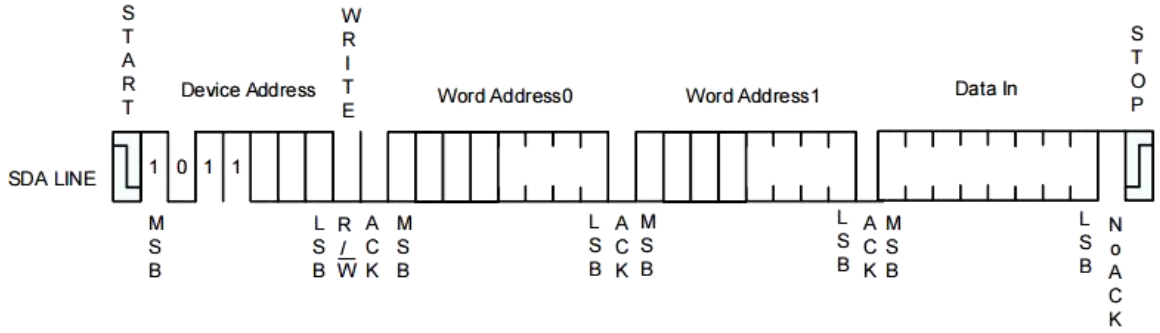
5.2.4 Read Identification Page

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A11 and A10 must be 0 and the LSB address bits A5~A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 58d, the number of bytes should be less than or equal to 6, as the ID page boundary is 64 bytes).

5.2.5 Read the Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a No-ACK bit if the Identification page is locked. (Refer to Figure 5-6).

Figure 5-6 Lock Status Read (When Identification page locked, return No-ACK after the data-in)



5.2.6 Read Serial Number

Reading the serial number is similar to the sequential read sequence but requires use of the device address refer to Table 4-1, a dummy write, and the use of a specific word address. The entire 128 bits value must be read from the starting address of the serial number block to guarantee a unique number.

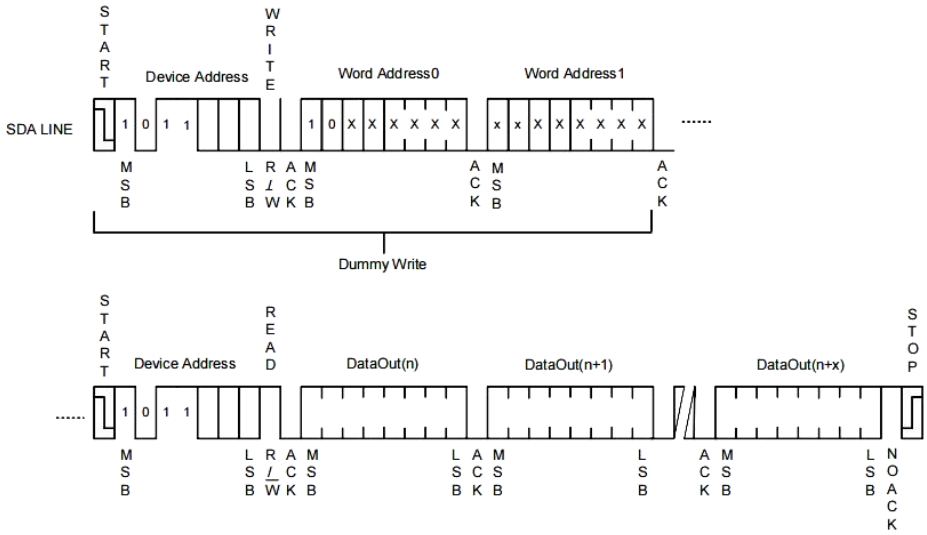
Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a '10' sequence in bit A11 and A10 of the word address, regardless of the intended address as depicted in Table 4-2. If a word address other than '10' is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

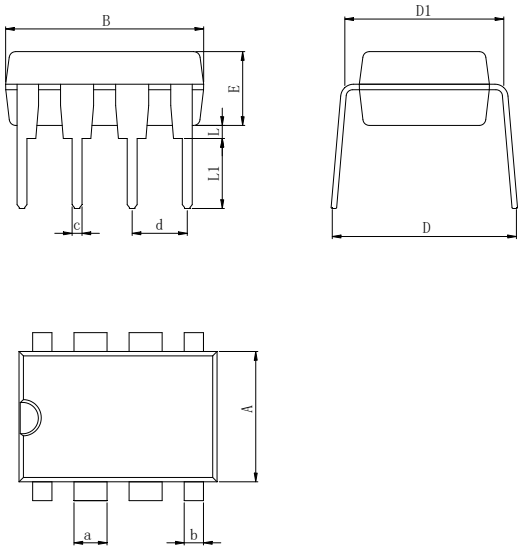
The Serial Number Read operation is terminated when the master does not respond with a zero (ACK) and instead issues a STOP bit (Refer to Figure 5-7)

Figure 5-7 Serial number Read



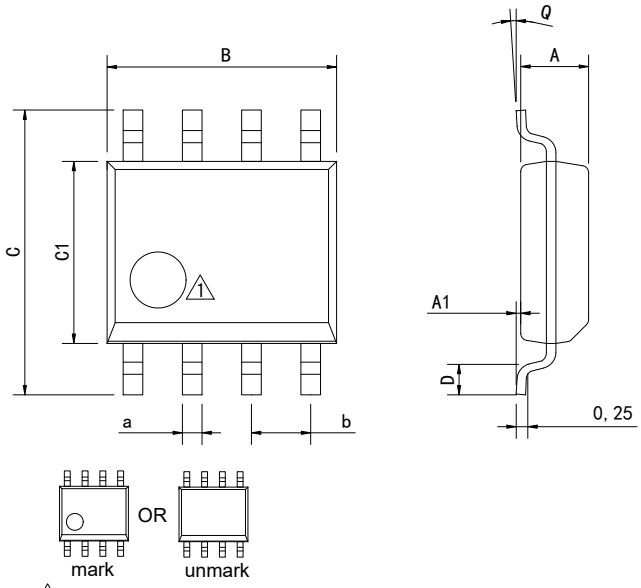
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	**A**	**B**	**D**	**D1**	**E**	**L**	**L1**	**a**	**b**	**c**	**d**
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP-8

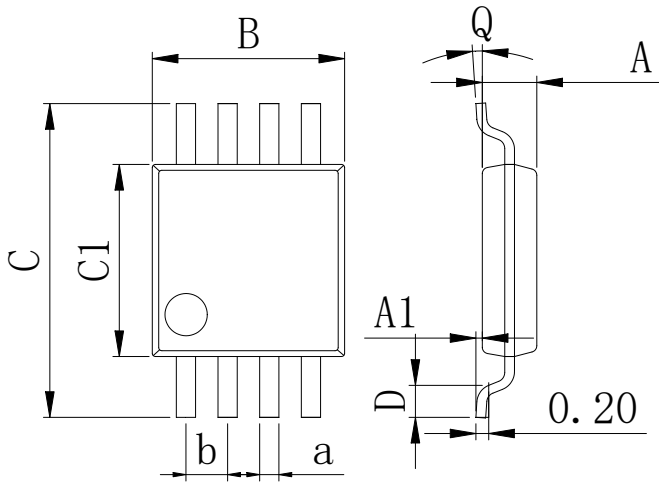


1 Package top mark may be in lower left corner or unmark

Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

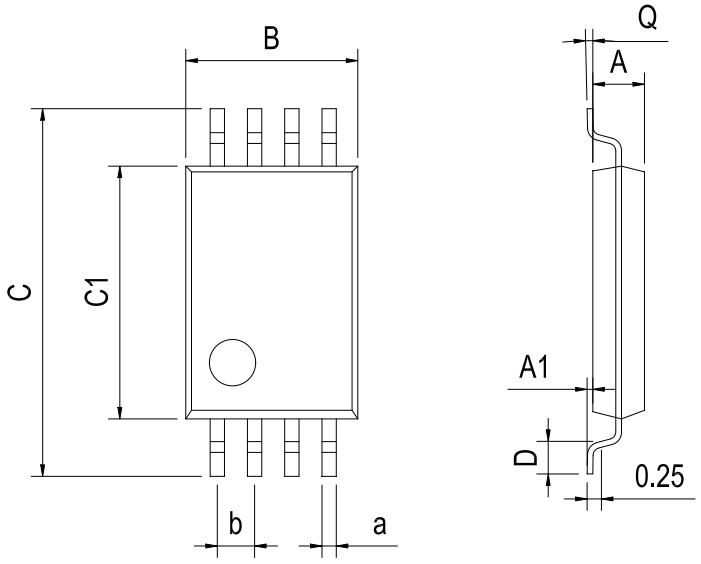
Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

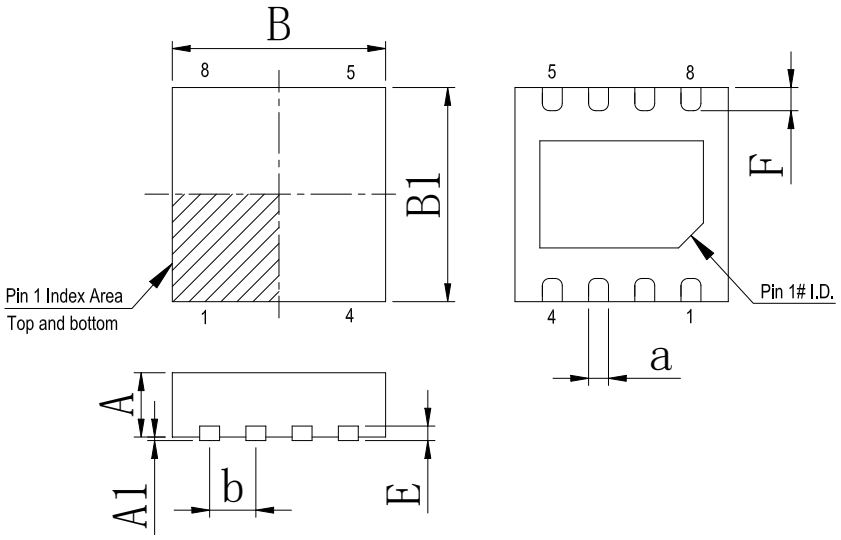
TSSOP-8 (4.4*3.0)



Dimensions In Millimeters(TSSOP-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	0.85	0.05	2.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	3.10	6.60	4.50	0.80	8°	0.25	

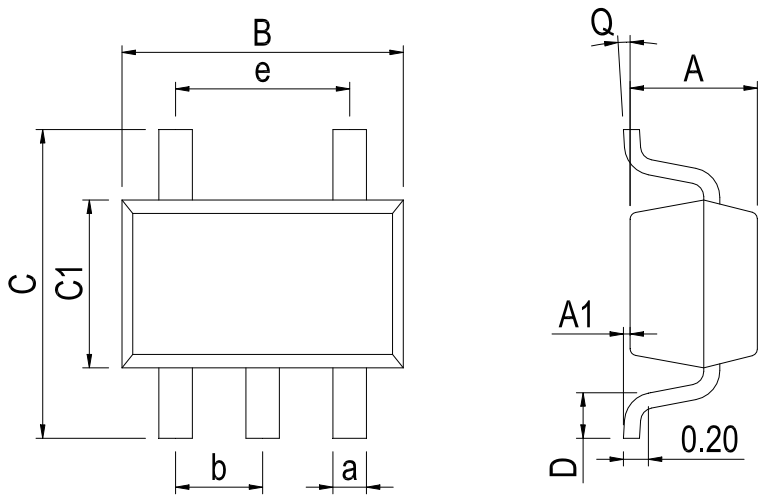
Physical Dimensions

DFN-8 3*3



Dimensions In Millimeters(DFN-8 3*3)								
Symbol:	**A**	**A1**	**B**	**B1**	**E**	**F**	**a**	**b**
Min:	0.85	0.00	2.90	2.90	0.20	0.30	0.20	0.65 BSC
Max:	0.95	0.05	3.10	3.10	0.25	0.50	0.34	

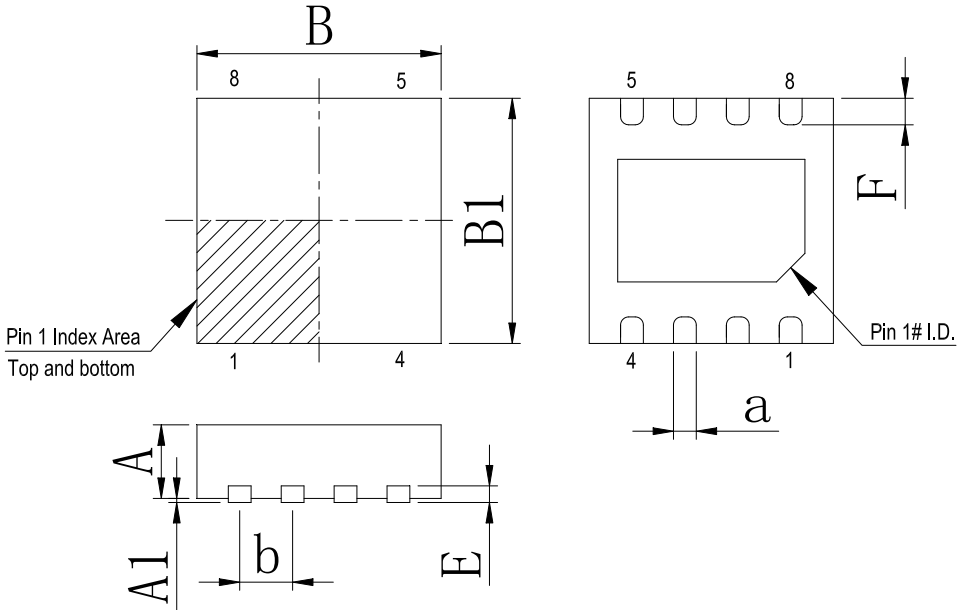
SOT-23-5



Dimensions In Millimeters(SOT-23-5)										
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**	**e**
Min:	1.00	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.95 BSC	1.90 BSC
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.50		

Physical Dimensions

DFN-8 2*2



Dimensions In Millimeters(DFN-8 2*2)								
Symbol:	**A**	**A1**	**B**	**B1**	**E**	**F**	**a**	**b**
Min:	0.85	0	1.90	1.90	0.15	0.25	0.18	0.50TYP
Max:	0.95	0.05	2.10	2.10	0.25	0.45	0.30	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2021-7	New	1-19
V1.1	2025-11	Document Reformatting	1-18
V1.2	2025-11	Update important statements、Update SOP-16 Dimension drawing	14、19

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