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TPVT4557YUG

SIM Card Interface Level Translator

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Features

- Supports clock speed up to 10 MHz clock
- Support SIM card supply voltages with range of 1.62 V to 3.6 V
- Host micro-controller operating voltage range: 1.08 V to 1.98 V
- Automatic enable and disable through VCCB
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Restriction of Hazardous Substances (RoHS) compliant and (Dark Green compliant)
- Packaging: QFN1418-10L

Applications

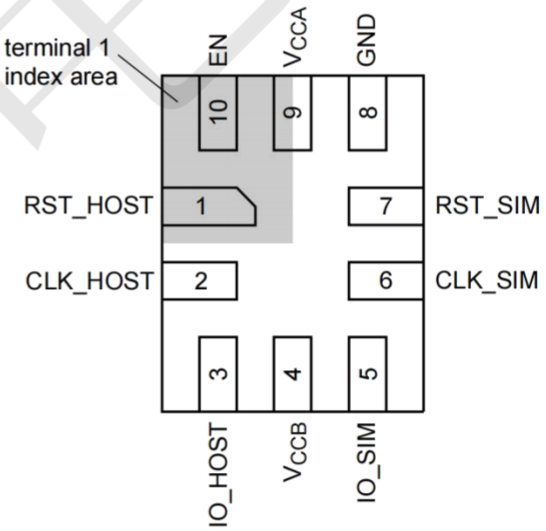
- SIM card terminals
- Mobile, Smart phones and Wireless modems

General Description

The device is built for interfacing a SIM card with a single low-voltage 1.0V to 1.8 V host side interface. The contains three 1.62 V to 3.6 V level translators to convert the data, RST and CLK signals between a SIM card and a host micro-controller. The is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.Incorporates shutdown feature for the SIM card signals according. Automatic level translation of I/O, RST and CLK between SIM card and host side interface with capacitance isolation.

Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on VCCB or any of the card side pins. External ESD diodes are not required.

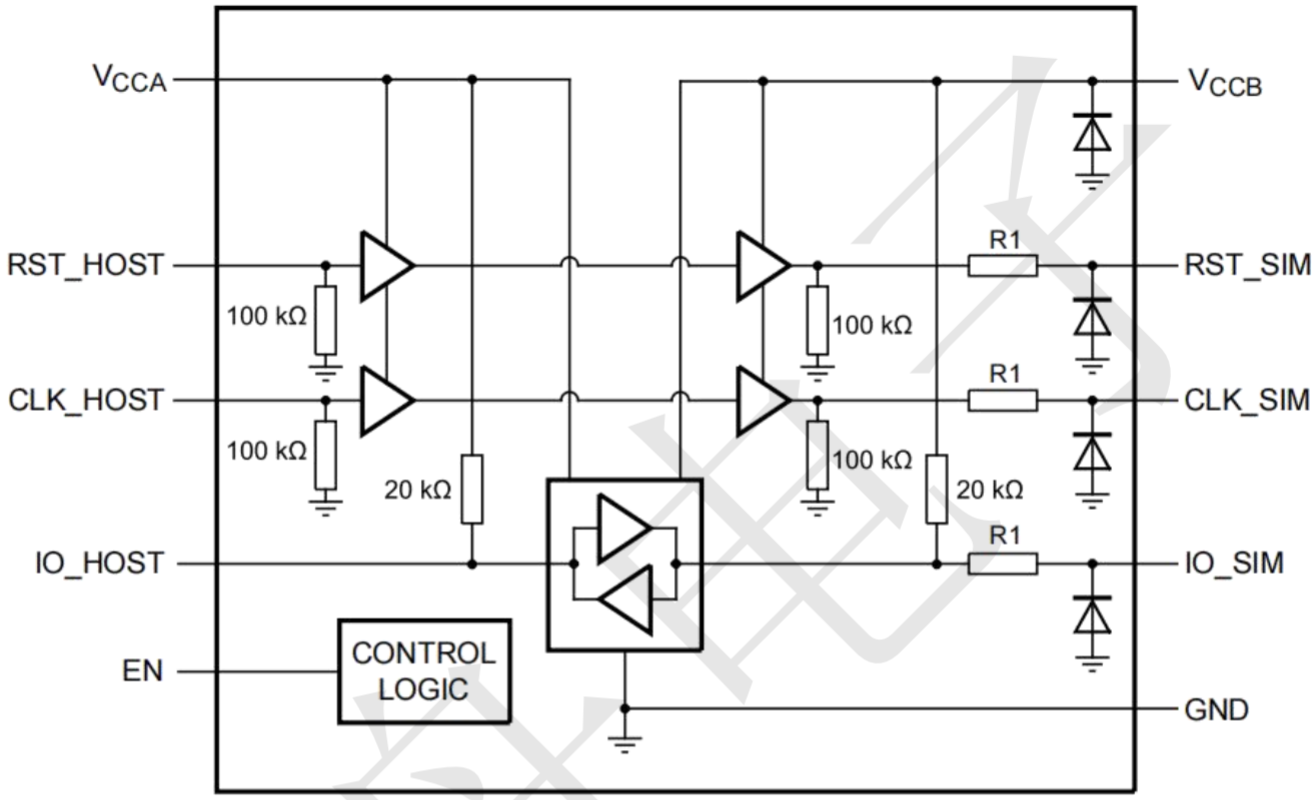
PIN CONFIGURATIONS (TOP VIEW)



PIN DESCRIPTION

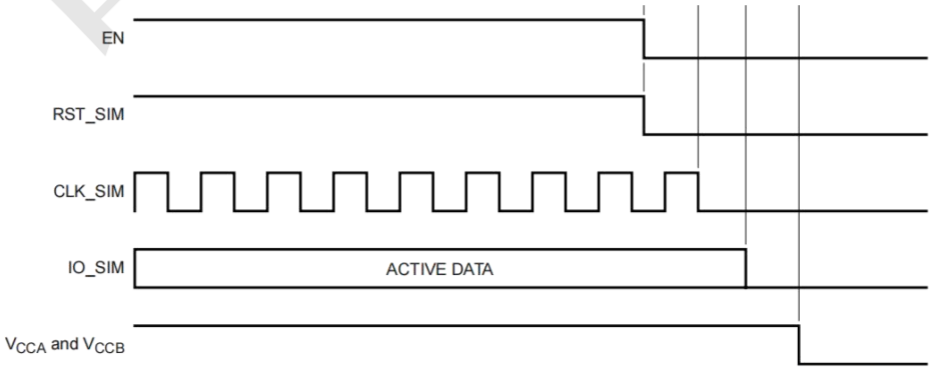
PIN NO.	PIN NAME	DESCRIPTION
1	RST_HOST	Reset input from host controller
2	CLK_HOST	Clock input from host controller
3	IO_HOST	Host controller bidirectional data input/output. The host output must be on an open-drain driver
4	VCCB	SIM card supply voltage. When VCCB is below the VCCB disable, the device is disabled.
5	IO_SIM	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver
6	CLK_SIM	Clock output pin for the SIM card
7	RST_SIM	Reset output pin for the SIM card
8	GND	Ground for the SIM card and host controller.
9	VCCA	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST).
10	EN	Host controller driven enable pin. This pin should be HIGH (VCCA) for normal operation, and LOW to help avoid race conditions specifically during the shutdown sequence.

Functional Diagram



Shutdown Sequence

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data. When the enable, EN, is asserted LOW, the shutdown sequence is initiated by powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM and IO_SIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds. It is important that EN is pulled LOW before VCCA and VCCB supplies go LOW to ensure that the shutdown sequence is properly initiated.



Shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and V_{CCA}/V_{CCB} SIM card translator

Electrical Characteristics 1

(Ta=25oC, VVCCA =1.0V~1.8V,VVCCB =1.62V~3.6V, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
VCCA	Host Side Supply		1.0	--	1.98	V
VCCB	SIM Side Supply		1.6	--	3.6	V
V_{VCCA_UVLO}	VCCA Under Voltage Lockout	Rising, 100mV hysteresis	0.6	0.7	0.8	V
V_{VCCB_UVLO}	VCCB Under Voltage Lockout	Rising. 100mV hysteresis	1.3	1.4	1.5	V
I_{SD_VCCA}	Shutdown Current EN=0V	VCCA=1.2V	--	0.5	1	uA
I_{SD_VCCB}		VCCB=1.8V	--	0.5	1	uA
I_{Q_VCCA}	Quiescent Current EN=VCCA	VCCA=1.2V, CLK_HOST=0V	--	0.5	1	uA
I_{Q_VCCB}		VCCB=1.8V, CLK_HOST=0V	--	0.5	1	uA
I_{ACT_VCCA}	Active Current EN=VCCA	VCCA=1.2V, CLK_HOST=1MHz CL= 30pF	--	5	10	uA
I_{ACT_VCCB}		VCCB=1.8V, CLK_HOST=1MHz CL= 30pF	--	250	300	uA
Logic I/O pin (EN)						
V_{IH}	High-Level Input Voltage	EN pin	0.7*VCCA	--	--	V
V_{IL}	Low-Level Input Voltage	EN pin	--	--	0.3*VCCA	V
Level Translator (Host Side)						
V_{IH}	High Level input voltage	IO_HOST, RST_HOST, CLK_HOST	0.7*VCCA	--	--	V
V_{IL}	Low Level input Voltage	IO_HOST, RST_HOST, CLK_HOST	--	--	0.3*VCCA	V
V_{OH}	High Level output voltage	IO_HOST, IOH_IO=20uA	0.8*VCCA	--	--	V
V_{OL}	Low Level output voltage	IO_HOST, IOL_IO=20uA	--	--	0.2*VCCA	V
R_{PUA}	Pull up resistance	IO_HOST connected to VCCA	6	8	10	kΩ

Electrical Characteristics 2

(Ta=25oC, VVCCA =1.0V~1.8V,VVCCB =1.62V~3.6V, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Level Translator (SIM Card Side)						
V_{IH}	High Level input voltage	IO_SIM	0.7*VCCB	--	--	V
V_{IL}	Low Level input Voltage	IO_SIM	--	--	0.3*VCCB	V
V_{OH}	High Level output voitage	CLK_SIM, RST_SIM, IOH=20uA	0.8*VCCB	--	--	V
		IO_SIM, IOH=20uA	0.8*VCCB	--	--	V
V_{OL}	Low Level output voltage	CLK_SIM, RST_SIM, IOL =-1mA	--	--	0.125* VCCB	V
		IO_SIM, IOL =-1mA	--	--	0.125* VCCB	V
R_{PUB}	Pull up resistance	IO_SIM connected to VCCB	12	20	30	kΩ
Rs	Series resistance	IO_SIM, RST_SIM, CLK_SIM	40	55	100	Ω
R_{PD}	Pull down resistance	IO_SIM, RST_SIM, CLK_SIM when EN is driven low	--	4	--	kΩ
Dynamic Characteristics (CL=30pE in Host side, CL=30Pf in SIM side, VCCA=1.8V, VCCB=3.0V)						
t_{PD}	Propagation delay	From Host side to SIM side	--	10	20	ns
t_{PD}	Propagation delay	From SIM side to HOST side	--	10	20	ns
t_{r_B}	RST_SIM Rising time	From 10% to 90% of VCCB=3.0V	--	8	15	ns
	CLK_SIM Rising time	From 10% to 90% of VCCB=3.0V	--	8	15	ns
	IO_SIM Rising time	From 10% to 90% of VCCB=3.0V	--	8	15	ns
t_{r_B}	RST SIM falling time	From 90 %to 10% of VCCB=3.0V	--	8	15	ns
	CLK_SIM falling time	From 90 %to 10% of VCCB=3.0V	--	8	15	ns
	IO_SIM falling time	From 90 %to 10% of VCCB=3.0V	--	8	15	ns

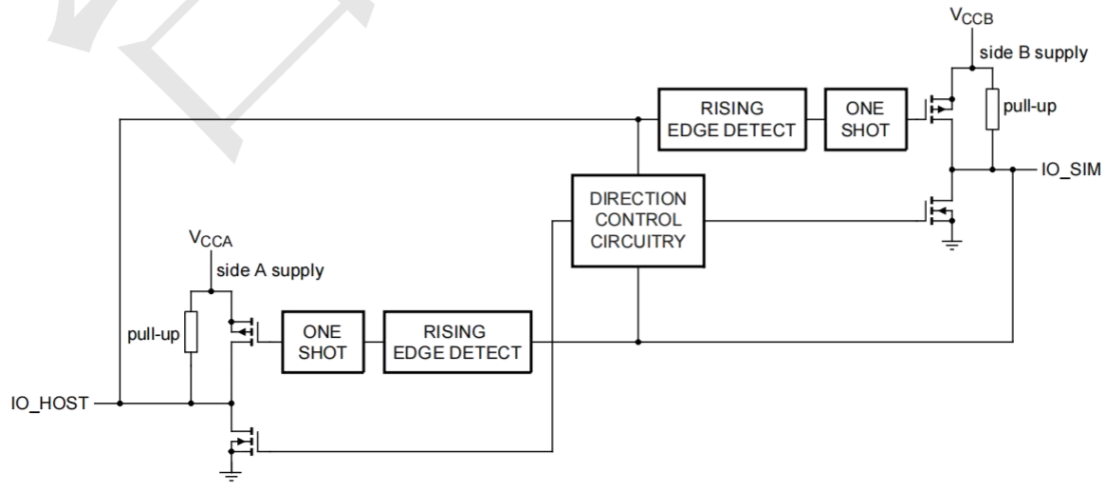
Electrical Characteristics 3

(Ta=25oC, VVCCA =1.0V~1.8V,VVCCB =1.62V~3.6V, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{r_A}	IO_HOST rising time	From 10% to 90% of VCCA=1.8V	--	8	15	ns
t_{r_A}	IO_HOST falling time	From 90 %to 10% of VCCA=1.8V	--	8	15	ns
t_{EN}	Enable timing	From EN High to RST_High	--	--	100	ns
t_{RST_DIS}	RST_SIM Disable time	From EN Low to RST_SIM low	--	200	--	ns
t_{CLK_DIS}	CLK_SIM Disable time	From EN low to CLK_SIM low	--	15	--	us
t_{IO_DIS}	IO_SIM Disable time	From EN low to IO_SIM low	--	--	--	us
f_{CLK}	CLK_HOST frequency		--	--	10	MHZ

Level Translator Stage

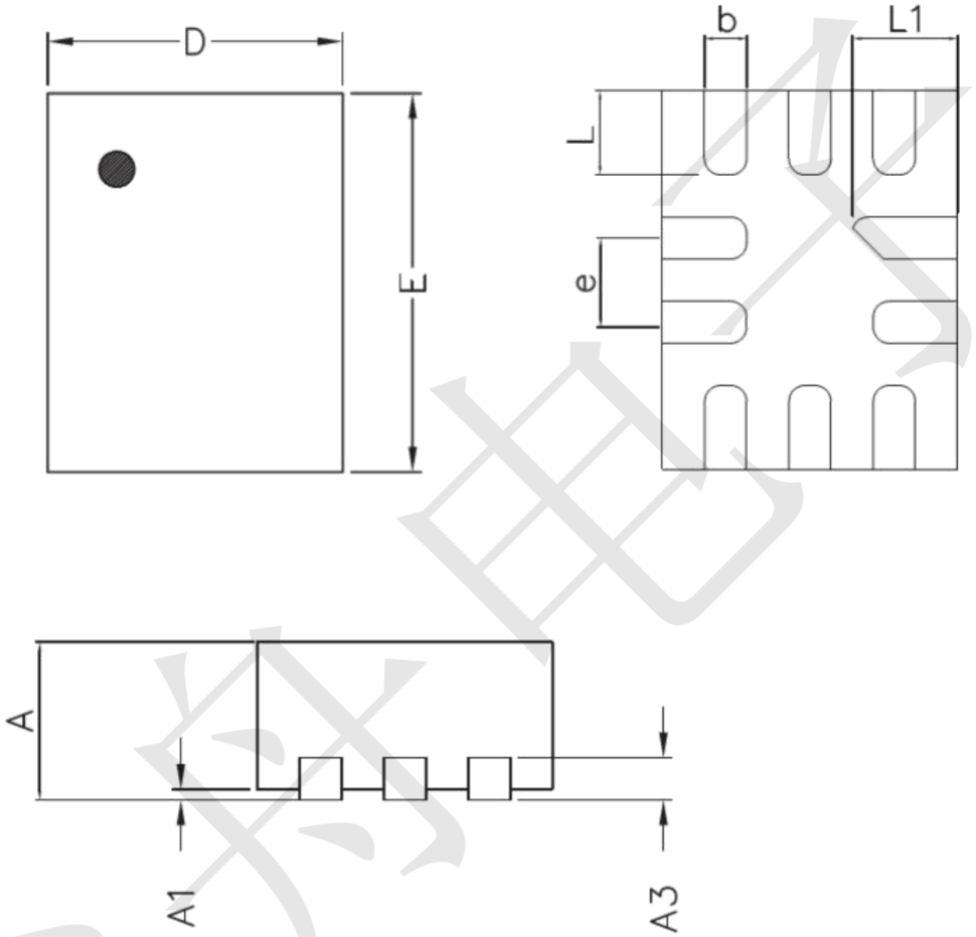
The architecture of the device I/O channel is shown below. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host. As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW. The channels RST and CLK just contain single direction drivers without the holding mechanism of the I/O channel, as these are just driven from the host to the card side.



Automatic direction control level translator for HIGH-level direction change interfaces

Package informantion

QFN1418-10L (Unit: mm)



Symbol	Dimension in Millimeters	
	Min.	Max.
A	0.450	0.550
A1	0.000	0.050
A3	0.152 Ref.	
D	1.350	1.450
E	1.750	1.850
b	0.150	0.250
e	0.400 Typ.	
L	0.350	0.450
L1	0.450	0.550