TPI3WVR646GEEX

High Performance MIPI,C-PHY Switch

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Features

- Wide VCC Supply Range: 1.65V~5.5V
- Low Quiescent Current: 35uA Typical
- Channel-to-Channel Cross-talk: -30dB Typical
- Insertion loss: -1dB@1GHz, -2dB @1.5GHz, -3dB@5.1GHz
- Power-off Truly Isolated and Off-Isolation: -25dB Typical
- Pin-to-Pin FSA646
- Small Packaging: CSP-36(WLCSP-36(2.4x2.4))

General Description

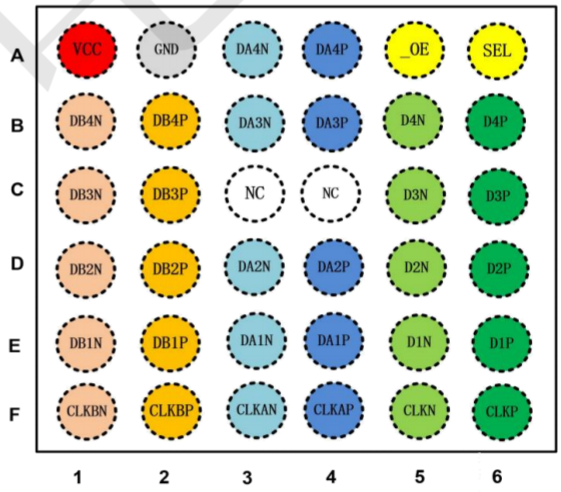
The is a high performance four-data lane MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The is has wide bandwidth and maintains good signal integrity,which makes it ideal is designed for the MIPI specification and allows connection to a CSI or DSI module. 36-Ball Wafer Level Chip Scale Package (WLCSP) 2.4mm x 2.4mm with Pb-free and Halogen-free,makes it ideal for mobile device.

Applications

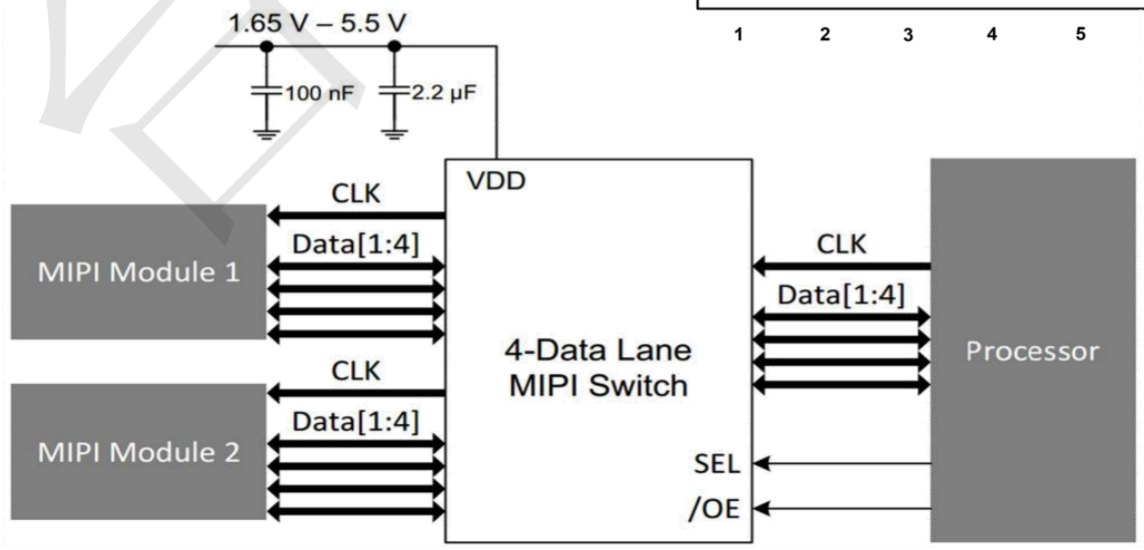
- Tablets and Notebooks
- Multi-Camera and Displays
- 4G/5G Smart Phone
- Telecom Signal Switching
- Mobile and AI Device

PIN CONFIGURATIONS

Top Through View



Functional Diagram



PIN DESCRIPTION

Pin #	Name	Type	Description
A1	VCC	PWR	1.5~5V Positive Supply
A2	GND	GND	Primary Ground Connection. Must be Connected to System Ground
A3	DA4N	I/O	A Side Data Path 4 Negative
A4	DA4P	I/O	A Side Data Path 4 Positive
A5	_OE	I	Chip Enable, Low Active
A6	SEL	I	Channel Selection. When Low, A side selected; When High, B side selected
B1	DB4N	I/O	B Side Data Path 4 Negative
B2	DB4P	I/O	B Side Data Path 4 Positive
B3	DA3N	I/O	A Side Data Path 3 Negative
B4	DA3P	I/O	A Side Data Path 3 Positive
B5	D4N	I/O	Common Side Data Path 4 Negative
B6	D4P	I/O	Common Side Data Path 4 Positive
C1	DB3N	I/O	B Side Data Path 3 Negative
C2	DB3P	I/O	B Side Data Path 3 Positive
C3	NC	O	Not Connected
C4	NC	O	Not Connected
C5	D3N	I/O	Common Side Data Path 3 Negative
C6	D3P	I/O	ommon Side Data Path 3 Positive
D1	DB2N	I/O	B Side Data Path 2 Negative
D2	DB2P	I/O	B Side Data Path 2 Positive
D3	DA2N	I/O	A Side Data Path 2 Negative
D4	DA2P	I/O	A Side Data Path 2 Positive
D5	D2N	I/O	Common Side Data Path 2 Negative
D6	D2P	I/O	Common Side Data Path 2 Positive
E1	DB1N	I/O	B Side Data Path 1 Negative
E2	DB1P	I/O	B Side Data Path 1 Positive
E3	DA1N	I/O	A Side Data Path 1 Negative
E4	DA1P	I/O	A Side Data Path 1 Positive
E5	D1N	I/O	Common Side Data Path 1 Negative
E6	D1P	I/O	Common Side Data Path 1 Positive
F1	CLKBN	I/O	B Side Clock Path Negative
F2	CLKBP	I/O	B Side Clock Path Positive
F3	CLKAN	I/O	A Side Clock Path Negative
F4	CLKAP	I/O	A Side Clock Path Positive
F5	CLKN	I/O	Common Side Clock Path Negative
F6	CLKP	I/O	Common Side Clock Path Positive

Absolute Maximum Ratings

(over operating free-air temperature range (unless otherwise noted) (1)

		Range	Unit
Power Supply Voltage	VCC	-0.5 ~ 6.0	V
Control Pins	_OE, SEL	-0.5 ~ VCC	V
DC Switch I/O Voltage	V_{SW}	-0.3 ~ VCC	V
DC I/O Current	I_{IK}	-50 ~ 50	mA
Storage Temperature Range	T_{STG}	-55 ~ 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001-2012	VCC	±2	kV
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV
ESD MM, JESD22-A115	VCC	±200	V
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV

(1) Stresses beyond those listed in Table-2 Absolute Maximum Ratings may cause permanent damage to the device. They are stress ratings only, which do not imply functional operation of the device at these or any other conditions. Beyond those indicated under Recommended Operating Conditions, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommend operating ratings

		Range	Unit
Power Supply Voltage	VCC	1.65 ~ 5.5	V
Control Pins	_OE, SEL	0 ~ VCC	V
Signal Pins	HS Mode	0 ~ 0.3	V
	LP Mode	0 ~ 1.3	V
Operating Temperature	T_A	-40 ~ 85	°C

(1) If _OE is left undriven, it will be pulled up to VCC by internal resistor; If SEL is left undriven, it will be pulled down to Ground by internal resistor.

Electrical Characteristics (Ta=25°C, VCC=1.8V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
VCC Quiescent Current	I_Q	SEL=0 or VCC, _OE=0	--	30	--	uA
Power-down Current	I_{PD}	SEL=0 or VCC, _OE=VCC	--	--	1.0	uA
DC Characteristics						
Input logic high	V_{IH}	VCC=1.8~4.5V	1.6	--	--	V
Input logic low	V_{IL}	VCC=1.8~4.5V	--	--	0.4	V
_OE Internal pull-up resistor	R_{UP}		--	2.0	--	MΩ
SEL Internal pull-down resistor	R_{DN}		--	2.0	--	MΩ
On-Resistance for LP MIPI	R_{ON_LP}	V_{IS}= 1.2V I_{ON}=8mA	--	4.8	10	Ω
On-Resistance for HS MIPI	R_{ON_HS}	V_{IS}= 0.2V I_{ON}=8mA	--	4.3	9.0	Ω
R_{ON} Flatness for LP MIPI	R_{FLAT_LP}	V_{IS}= 0 to 1.2V I_{ON}=8mA	--	0.9	--	Ω
R_{ON} Flatness for HS MIPI	R_{FLAT_LP}	V_{IS}= 0 to 0.2V I_{ON}=8mA	--	0.2	--	Ω
R_{ON} Matching Between Channels	R_{MATCH}	V_{IS}= 0 to 1.2V I_{ON}=8mA	--	0.1	--	Ω
Switch Off Leakage Current	I_{OFF}	_OE=VCC Dn, Dp =VCC DAn, DBn, DAp, DBp=0 CLKn, CLKp=0 CLKAn, CLKBn, CLKAp,CLKBp=VCC	-0.5	--	0.5	uA
AC Characteristics						
Enable Time _OE to Output	t_{EN}	R_L=50Ω C_L=0pF V_{IS}= 0.6V	--	80	150	uS
Disable Time _OE to Output	t_{DIS}	R_L=50Ω C_L=0pF V_{IS}= 0.6V	--	40	250	nS
Turn-On Time SEL to Output	t_{ON}	R_L=50Ω C_L=0pF V_{IS}= 0.6V	--	400	1200	nS
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω C_L=0pF V_{IS}= 0.6V	--	130	800	nS

Electrical Characteristics (Ta=25°C, VCC=1.8V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AC Characteristics						
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω C_L=0pF V_{IS}= 0.6V	--	130	800	nS
Break-Before-Make Time	t_{BBM}	R_L=50Ω C_L=0pF V_{IS}= 0.6V	--	250	500	nS
Propagation Delay	t_{PD}	R_L=50Ω C_L=0pF V_{IS}= 0.6V	--	0.25	--	nS
HS Mode Skew of Opposite Transitions of the Same Output	$t_{SK(P)}$	R_L=50Ω C_L=0pF V_{IS}= 0.3V	--	6.0	--	pS
HS Mode Skew of Channel-to-Channel Single-Ended Skew	$t_{SK(O)}$	R_L=50Ω C_L=0pF V_{IS}= 0.3V	--	6.0	--	pS
Off Isolation	Off	R_L = 50Ω f = 1.2GHz V_{IS}=0.2V_{PP}	--	-25	--	dB
Crosstalk (Channel-to-Channel)	X_{TALK}	R_L = 50Ω f = 1.2GHz V_{IS}=0.2V_{PP}	--	-30	--	dB
-3dB Bandwidth (Insertion Loss)	BW_{-3dB}	R_L=50Ω C_L=0pF Signal 0dBm	--	5.1	--	GHz
Capacitance						
Switch On Capacitance	C_{ON}	V_{Bias} = 0.2V, f = 1250MHz	--	1.5	--	pF
Switch Off Capacitance	C_{OFF}	V_{Bias} = 0.2V, f = 1250MHz	--	1.0	--	pF

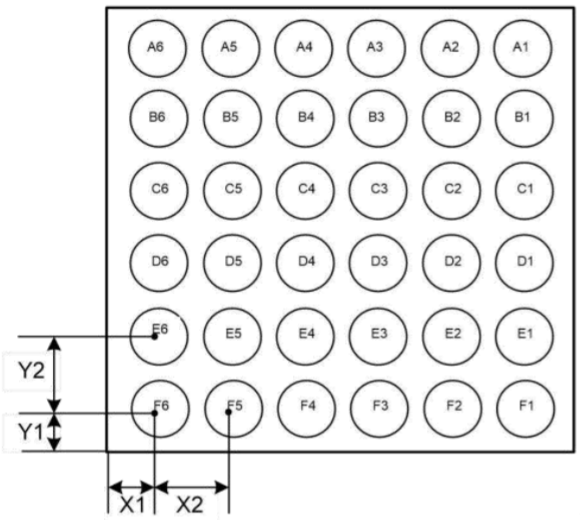
Note:

(1)Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

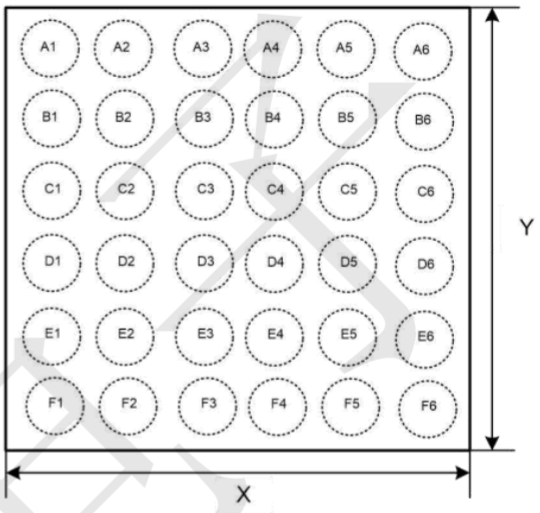
(2)Crosstalk is inversely proportional to source impedance.

Package information

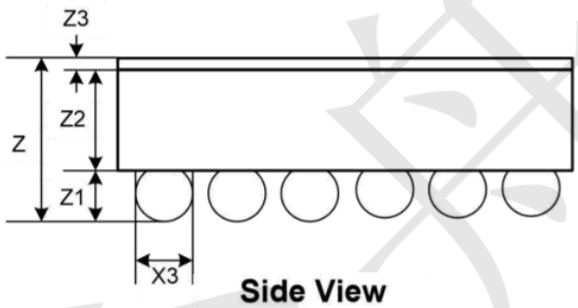
CSP-36(WLCSP-36(2.4x2.4))



Bottom-Up View



Top-Through View



Side View

Symbol	Dimensions In Millimeter		
	Min.	Typ.	Max.
X	2.37	2.40	2.43
Y	2.37	2.40	2.43
X1		0.16	
X2		0.40	
X3	0.175	0.205	0.235
Y1		0.16	
Y2		0.40	
Z	0.550	0.600	0.650
Z1	0.145	0.170	0.195
Z2	0.340	0.365	0.390
Z3	0.395	0.040	0.045