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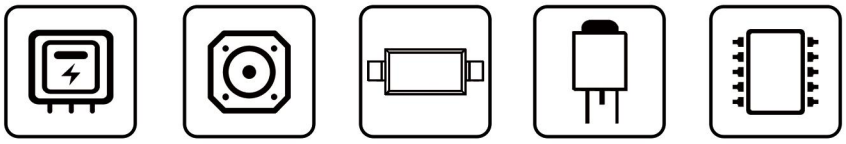
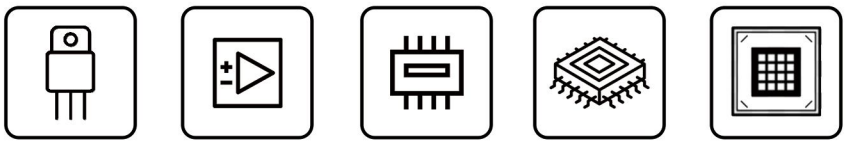




BISS0001-TD

產品規格說明書

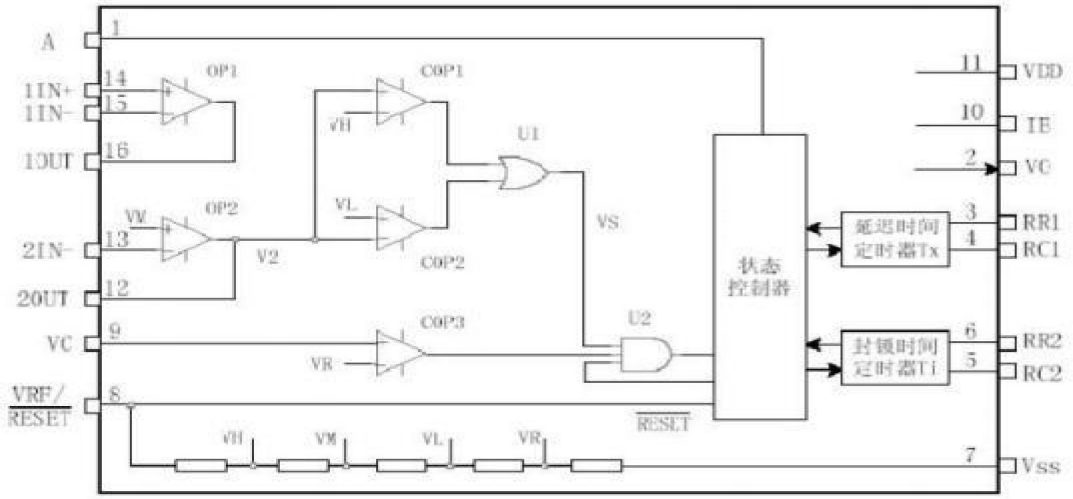
Features

- Low power CMOS technology
- CMOS high input impedance operational amplifiers
- Bi-directional level detector/Excellent noise immunity
- Internal delay time timer and blocking time timer
- Use 16 pin DIP and SOP packages

General Description

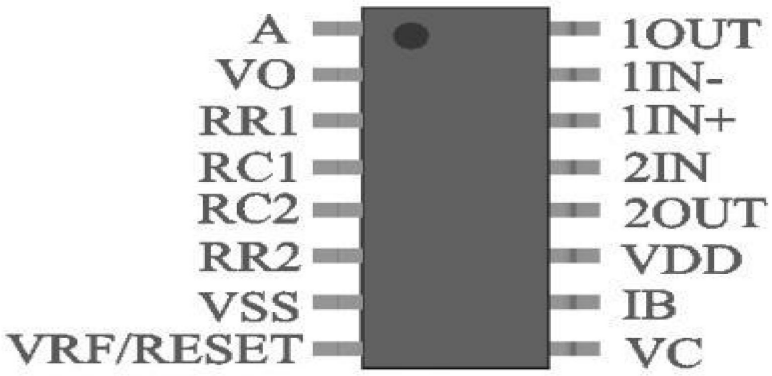
The **BISS0001-TD** is a sensor signal processing integrated circuits with higher performance. It is accompanied by pyroelectric infrared sensor and a small amount of external components passive pyroelectric infrared switch.It can automatically and quickly turn all kinds of incandescent lamp,fluorescent lamp,a buzzer,automatic door,electric fan,drying machines and other automatic device,particularly suitable for enterprises,hotels,shopping malls,warehouse and families aisles, corridors and other sensitive areas,or for automatic lighting,lighting and alarm system security zone.

Block Diagram



Package and pin assignment

BISS0001-TDprovides DIP 16 and SOP 16 dual in-line package.



Serial umber	Name	Functional Description
1	A	Select repeatable or non-repeatable trigger.When A=1.Allow duplicate trigger;or A=0;not allowed to repeat the trigger
2	VO	output pin
3	RR1	RR1 TX output resistor to adjust the delay time ends.(adjust the time lights on to off) TX≈50000×R1×C1
4	RC1	RC1 output capacitor to adjust the delay time TX end.(adjust the time lights on to off)
5	RC2	RC2 trigger lockout time TI capacitance adjustment end.(adjust the time lights off) Ti≈40×R2×C2
6	RR2	RR2 trigger lockout time TI's resistance adjustment end.(adjust the time lights off)
7	VSS	Negative power supply
8	VRF	reference voltage and the reset input.Typically connected toVDD,when connected to can make the timer reset.
9	VC	VC trigger is prohibited.Trigger when Vc<Vr.When allowed to trigger Vc>Vr.(Vr=0.2VDD)
10	IB	operational amplifier bias current settings
11	VDD	Positive power supply
12	2OUT	The second stage operational amplifier output
13	2IN-	The second stage operational amplifier inverting input
14	1IN+	The first stage operational amplifier inverting input
15	1IN-	The first stage operational amplifier inverting input
16	1OUT	The first stage operational amplifier output

Absolute Maximum Ratings

Vdd=5.0V Ta=25° C

Symbol	Parameters	Test Conditions	Parameter range	Unit
VDD	Supply Voltage	———	0.3———7.0	V
VI/VO	Input/output voltage	———	VSS-0.3———VDD+0.3	V
IOUT	Output Current	VDD=5.0V	10	mA
Topr	Operating Temperature	———	20———70	C
Tstr	Storage temperature	———	-40———+125	C

Electrical Characteristics

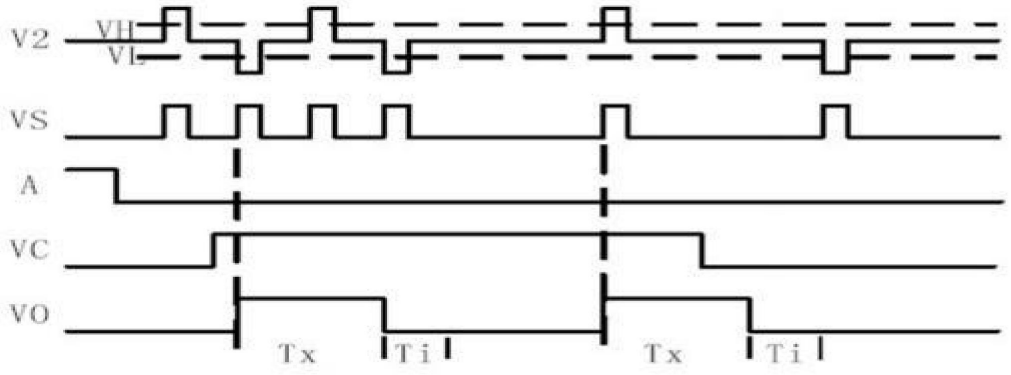
Vdd=5.0V Ta=25° C

Symbol	Parameters	Test Conditions		Min	Max	Uint
VDD	Operating Voltage Range	———		3	6	V
I	Current	No load	VDD=3V		50	uA
			VDD=5V		100	
VOS	Input offset voltage	VDD=5V			30	mV
IOS	Input Offset Current	VDD=5V			50	nA
AVO	Open-loop voltage gain	VDD=5V,RL=1.5M Ω		60		dB
CMRR	CMRR	VDD=5V,RL=1.5M Ω		60		dB
VYH	Opamp output high	VDD=5V		4.25		V
VYL	Opamp output low				0.75	V
VRH	Opamp input high	VRF=VDD=5V		1.1		V
VRL	Opamp input low				0.9	V
VOH	Opamp input high	VDD=5V，IOH=0.5 mA		4		V
VOL	Opamp input high	VDD=5V，IOL=0.1 mA			0.4	V
VAH	A input high	VDD=5V		3.5		V
VAL	A input low	VDD=5V			1.5	V

Functional Description

BISS0001-TDis mixed analog-digital ASIC constituted.by operational amplifiers, voltage comparators,state controller,delay timer,blockade time timer etc.

Unrepeatable trigger work
following figure unrepeatable trigger waveform to illustrate their work.



First, according to actual needs, The signal amplification by the using of the operational amplifier OP1 composition sensor signal preprocessing circuit. The second stage of amplificatio by to the operational amplifier OP2. while the voltage elevated after as VM≈0.5VDD, the output signal V2 to the comparator COP1 and COP2 composed of two-way amplitude to detect valid trigger signal Vs. Because VH≈0.7VDD, VL≈0.3VDD, so when VDD=5V, you can effectively suppress noise±1V, System reliability had be improved.

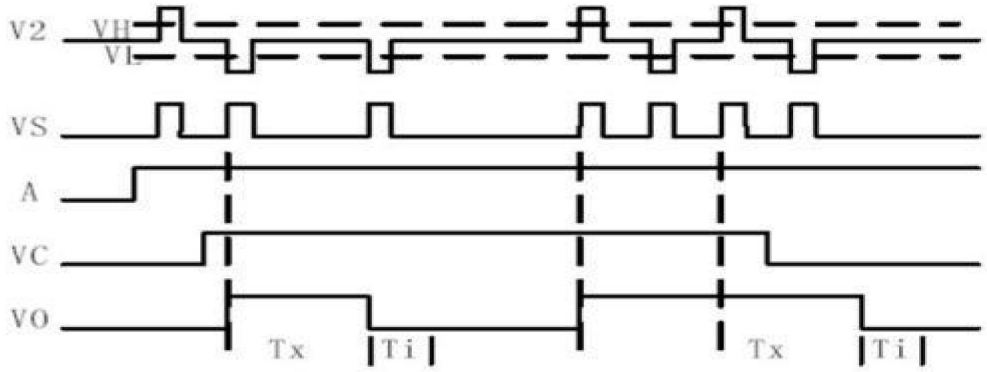
COP3 is a condition of the comparator. When Vc<VR(=0.2VDD), the COP3 output is low to seal the gate U2, forbid window signal downward transfer; and when Vc>VR, COP3 outputs high level, enter to delay period.

When the A terminal is connected with the"0"level, any change in TX time V2 will be ignored until the end of time, Tx, the so-called unrepeatable trigger work mode. When Tx the end of time, the down-regulation of Vo is low, at the same time start blocking time timer and enter the blocked period Ti. In Ti time, any change of V2 cannot make Vo jump into an active state, which can effectively

suppress interference generated during load switching.

Repeated trigger work mode

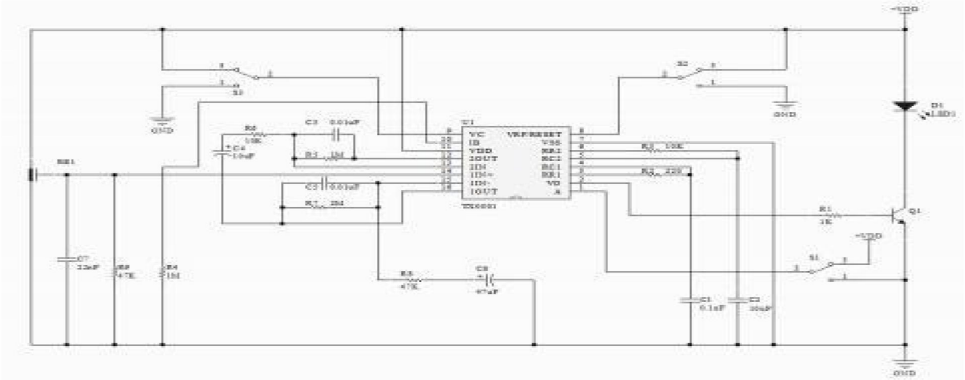
As shown in the following figure can be triggered repeatedly working modewaveforms,to illustrate its working process.



In Vc=0,A=0 period,Vs can not trigger Vo to the active state.In Vc=1,A=1,Vs can triggered Vo to the active state repeatedly and can make Vo keep valid state in the Tx period.

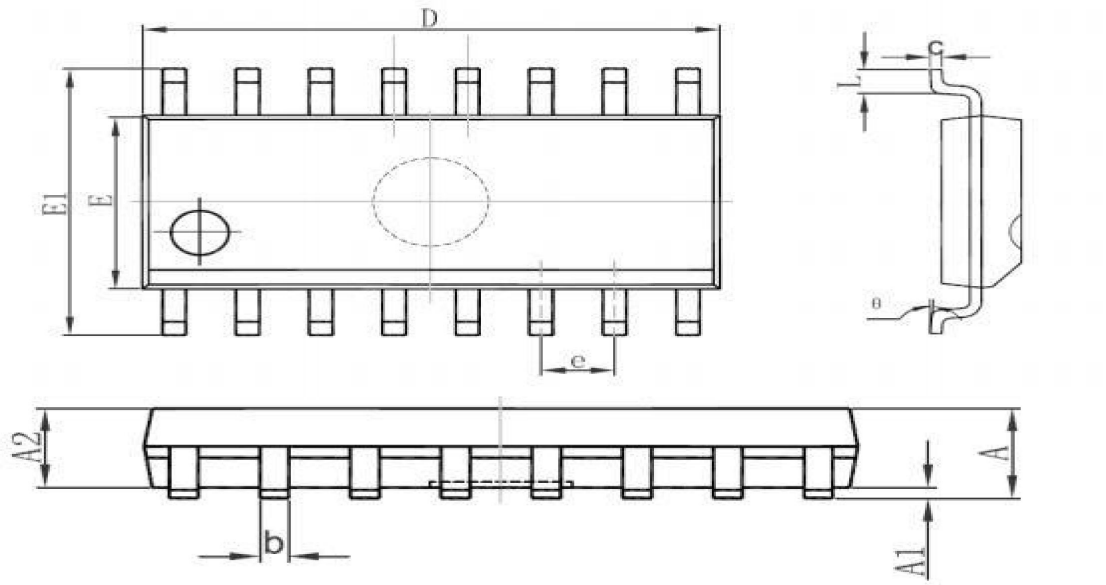
Within Tx time,jump on the long Vs changes,Vo continue to next a Tx cycle form the moment of Vs changes. If Vs keep"1"state,Vo keep active;If Vs keep"0",then in the period after the Tx,Vo restored to the inactive state;any change of Vs cannot make Vo to the active state in the lockout time Ti.

Application Circuits



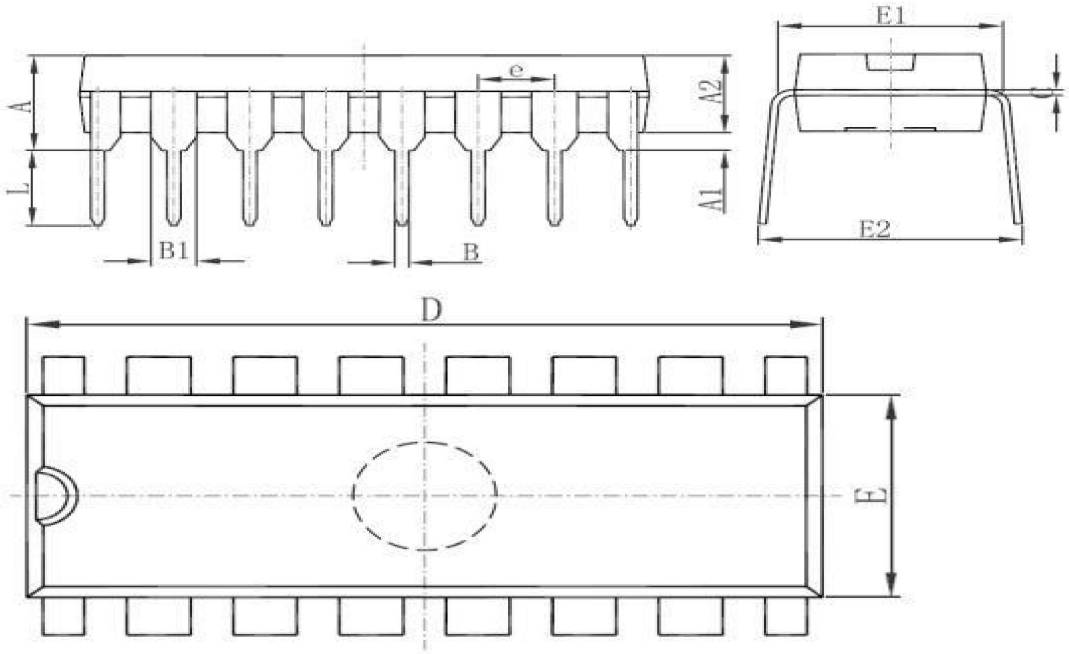
Package Information

SOP16 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP16 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354