钍地半导体
Tudi Semiconductor

Product Specification

TUDI-ADM1232

Microprocessor Supervisory Circuit

网址 www.sztdbdt.com

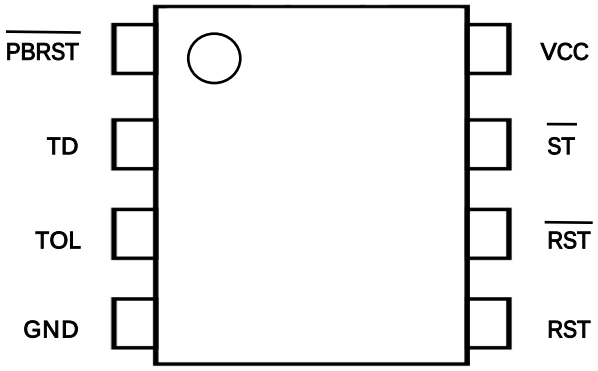
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Adjustable precision voltage monitor with 4.5 V and 4.75 V options
- Adjustable strobe monitor with 150 ms, 600 ms, or 1.2 sec options
- No external components
- Specified from 40°C to +85°C



Pin Diagram

Applications

- Microprocessor
- systems Portable
- equipment
- Computers
- Intelligent
- instruments
- Automotive systems

Description

ADM1232 is a microprocessor supervisory circuit which can monitor the following:

- Microprocessor power supply voltage
- Whether the processor locked up
- External interrupts

ADM1232 comes in two packages: SOP8 and DIP8

Pin description

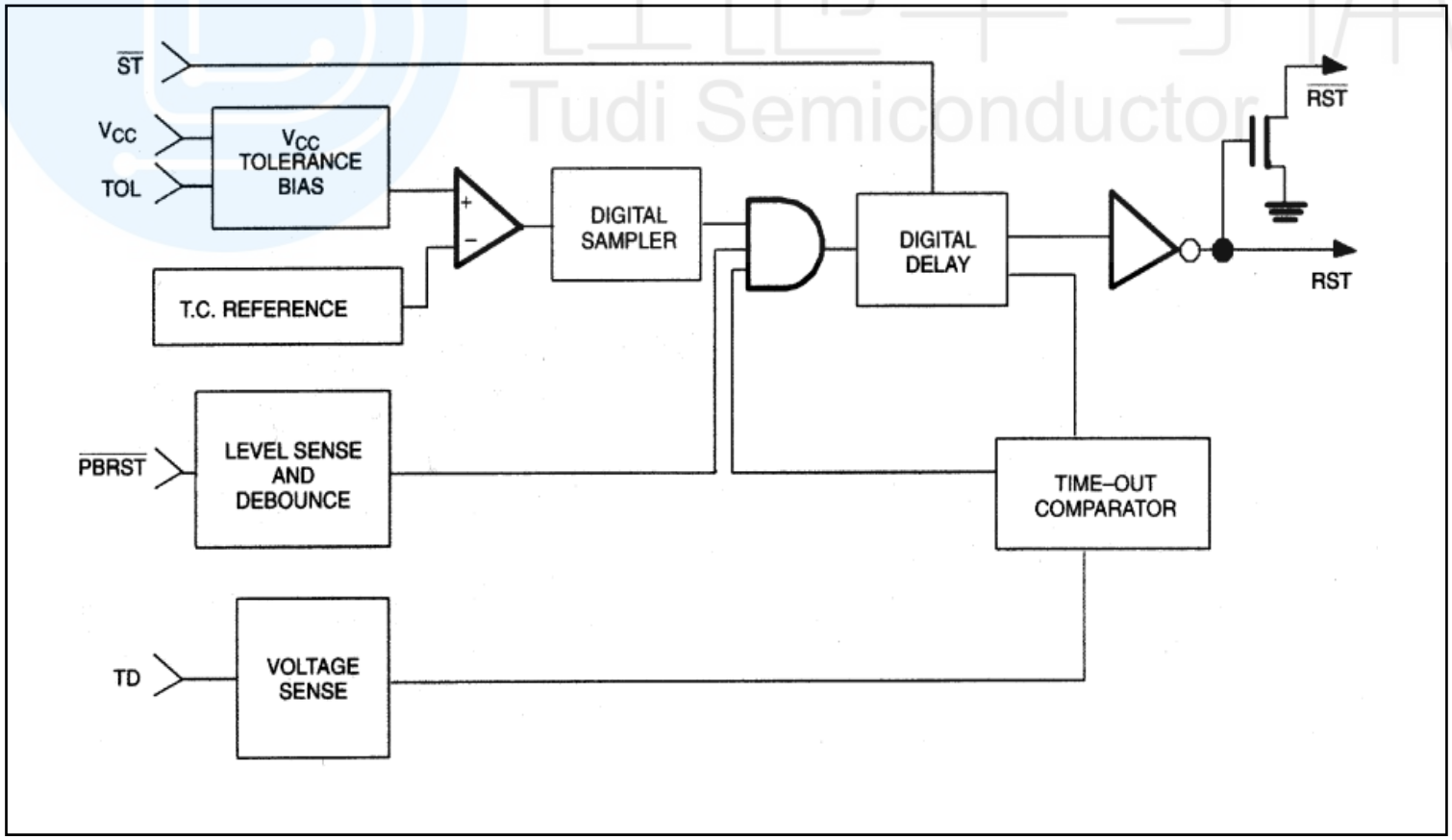
1	PBRST	Pushbutton Reset Input
2	TD	Time Delay Set
3	TOL	Selects 5%or 10%Vcc Detect
4	GND	Ground
5	RST	Reset Output(Active High)
6	RST	Reset Output(Active Low,opendrain)
7	ST	Strobe Input
8	Vcc	+5 Volt Power

Parameter limit

Voltage on Vcc Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to Vcc+0.5V
Operating Temperature	0℃ to 70℃
Operating Temperature (Industrial Version)	- 40°C to 85°C
Storage Temperature	-55℃ to+125℃
Soldering Temperature	260℃ for 10 seconds

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Micro-detector block diagram



Operation - Power monitoring
The 1232 detects out-of-tolerance power supply conditions and warns a processor-basedsystem of impending power failure.When Vcc falls below a preset level as defined by TOL,the Vcccomparator outputs the signals RST and $\overline{RST}$ .When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as Vcc falls below 4.75 volts.When TOL is connected to Vcc,the RST and $\overline{RST}$ signals become active as Vcc falls below 4.5 volts.The RST and $\overline{RST}$ are excellent control signals for amicroprocessor,as processing is stopped at the last possible moments of valid Vcc.On power-up,RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize
Operation - Button reset
The 1232 provides an input pin for direct connection to a pushbutton(Figure 1) Thepushbutton reset input requires an active low signal.Internally,this input is debounced and timed suchthat RST and $\overline{RST}$ signals of at least 250 ms minimum are generated.The 250 ms delay starts as thepushbutton reset input is released from low level.
Operation - Watchdog timer
The watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is notstimulated for a predetermined time period.The time period is set by the TD input to be typically 150 mswith TD connected to ground,600 ms with TD left unconnected, and 1.2 seconds with TD connected toVcc.The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactiveIf a high-to-low transition occurs on the $\overline{ST}$ input pin prior to timeout,the watchdog timer is reset andbegins to timeout again If the watchdog timer is allowed to timeout,then the RST and $\overline{RST}$ signals aredriven to the active state for 250 ms minimum.The $\overline{ST}$ input can be derived from microprocessor addresssignals, data signals,and/or control signals.When the microprocessor is functioning normally, thesesignals would,as a matter of routine,cause the watchdog to be reset prior to timeout.To guarantee thatthe watchdog timer does not timeout,a high-to-low transition must occur at or less than the minimumshown in Table 1.A typical circuit example is shown in Figure 2.

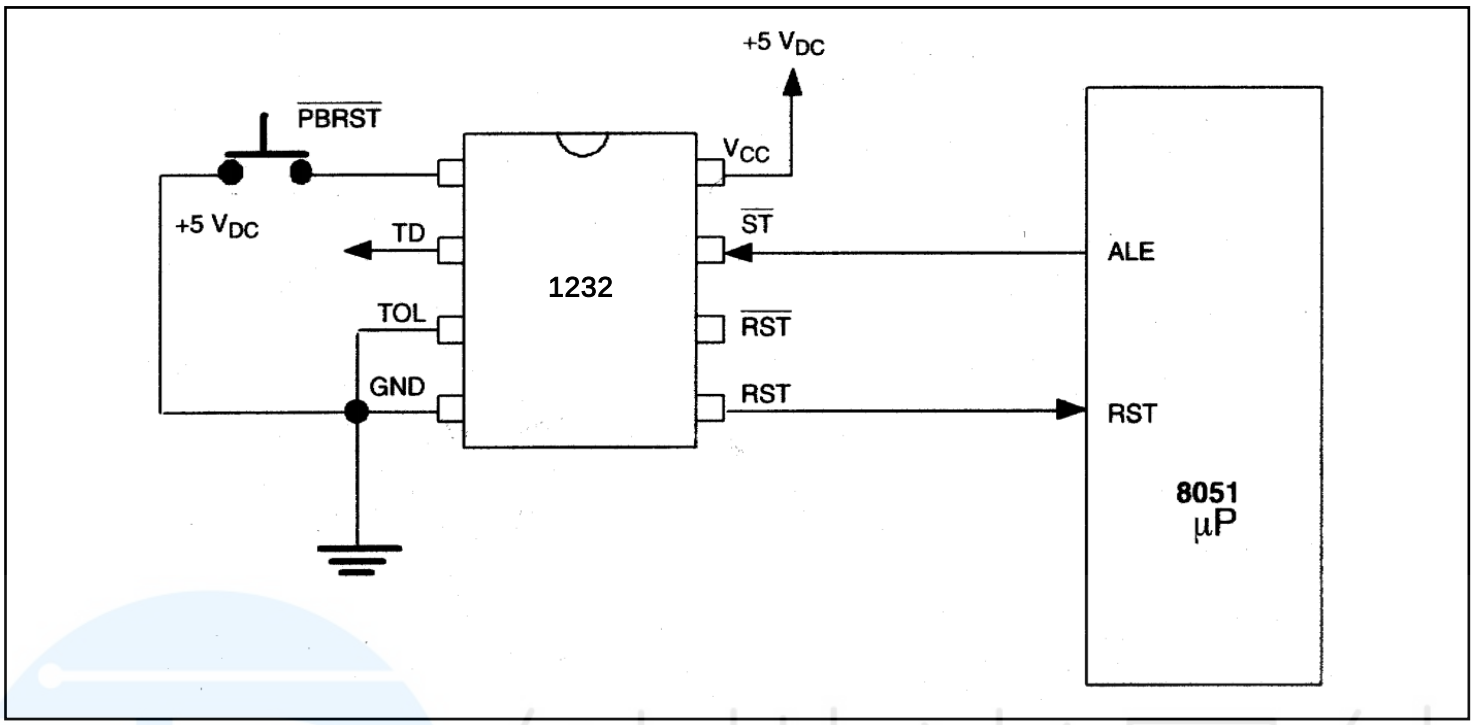


Figure 1 Button reset

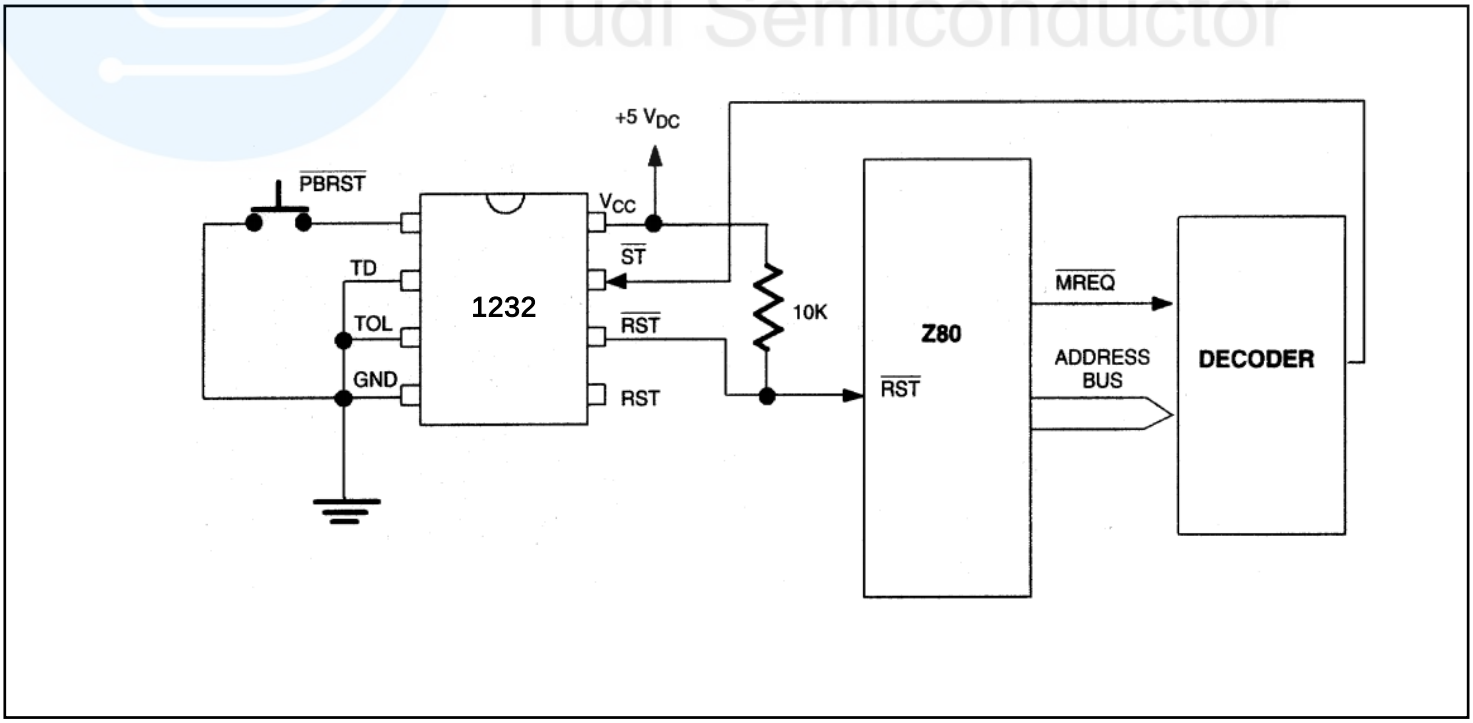


Figure 2 Watchdog timer

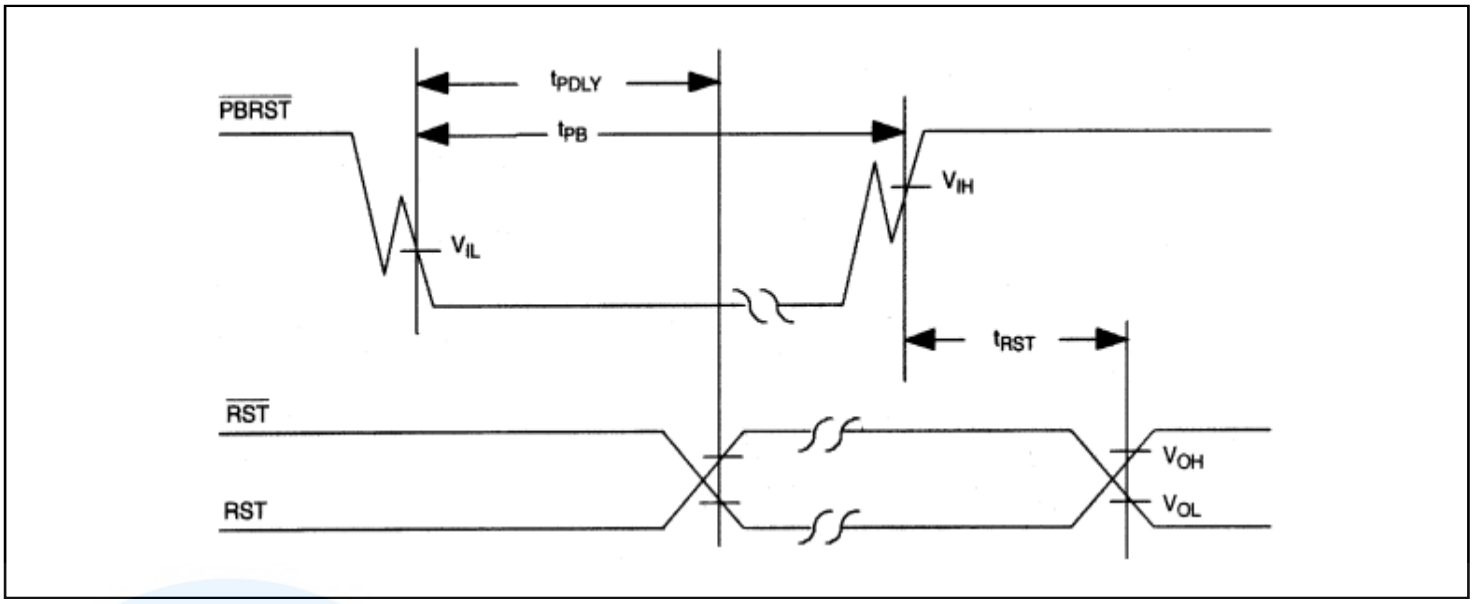


Figure 3 Timing diagram: button reset

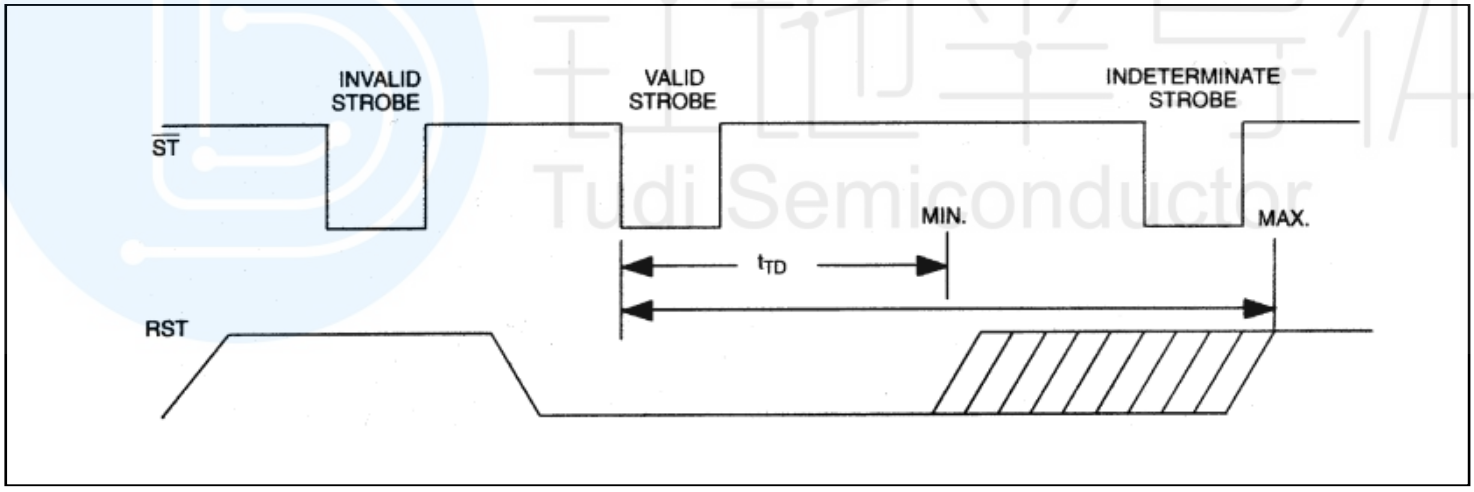


Figure 4 Timing diagram: pulse input

TD	Time-out		
	MIN	TYP	MAX
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
Vcc	500 ms	1200 ms	2000 ms

Table 1 Watchdog timeout

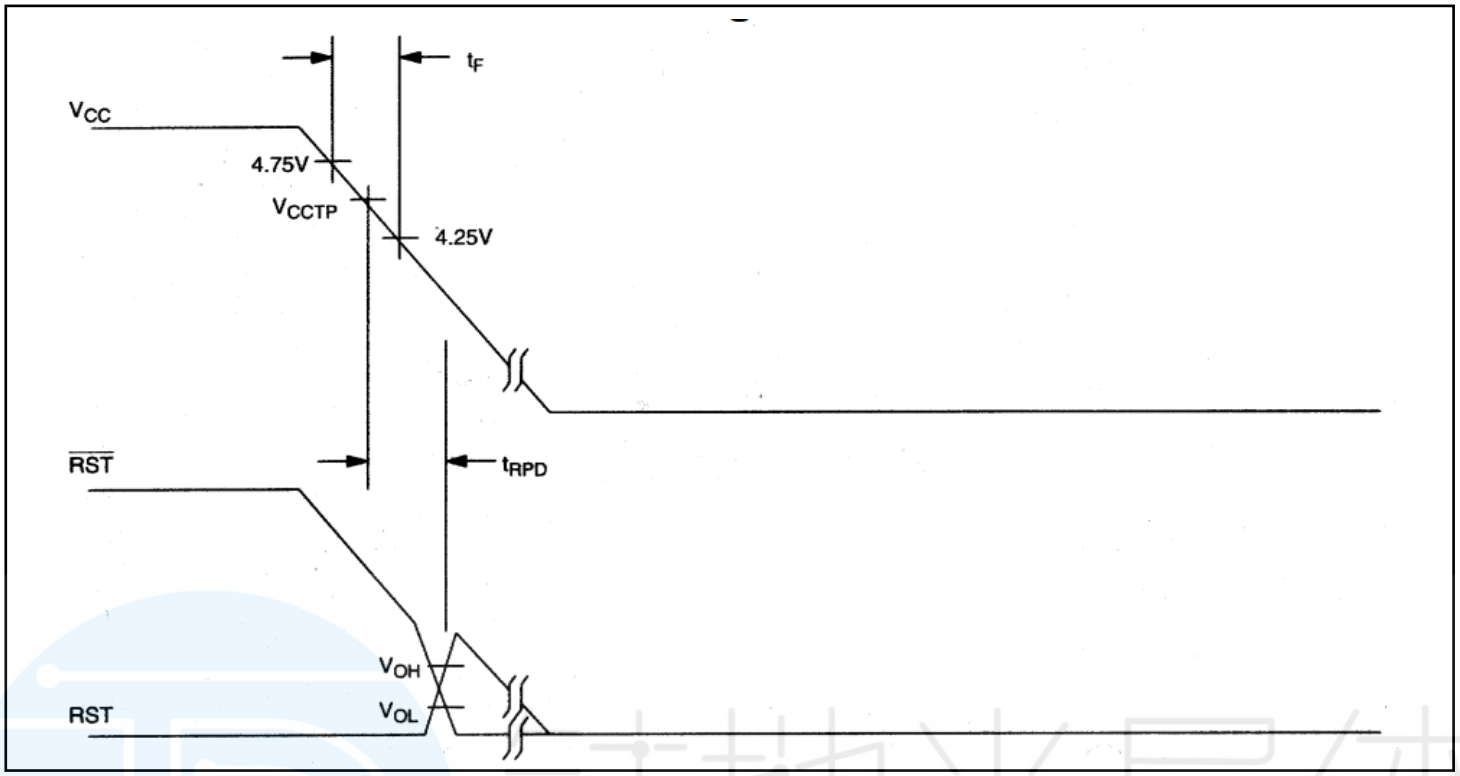


Figure 5 Timing diagram: power off

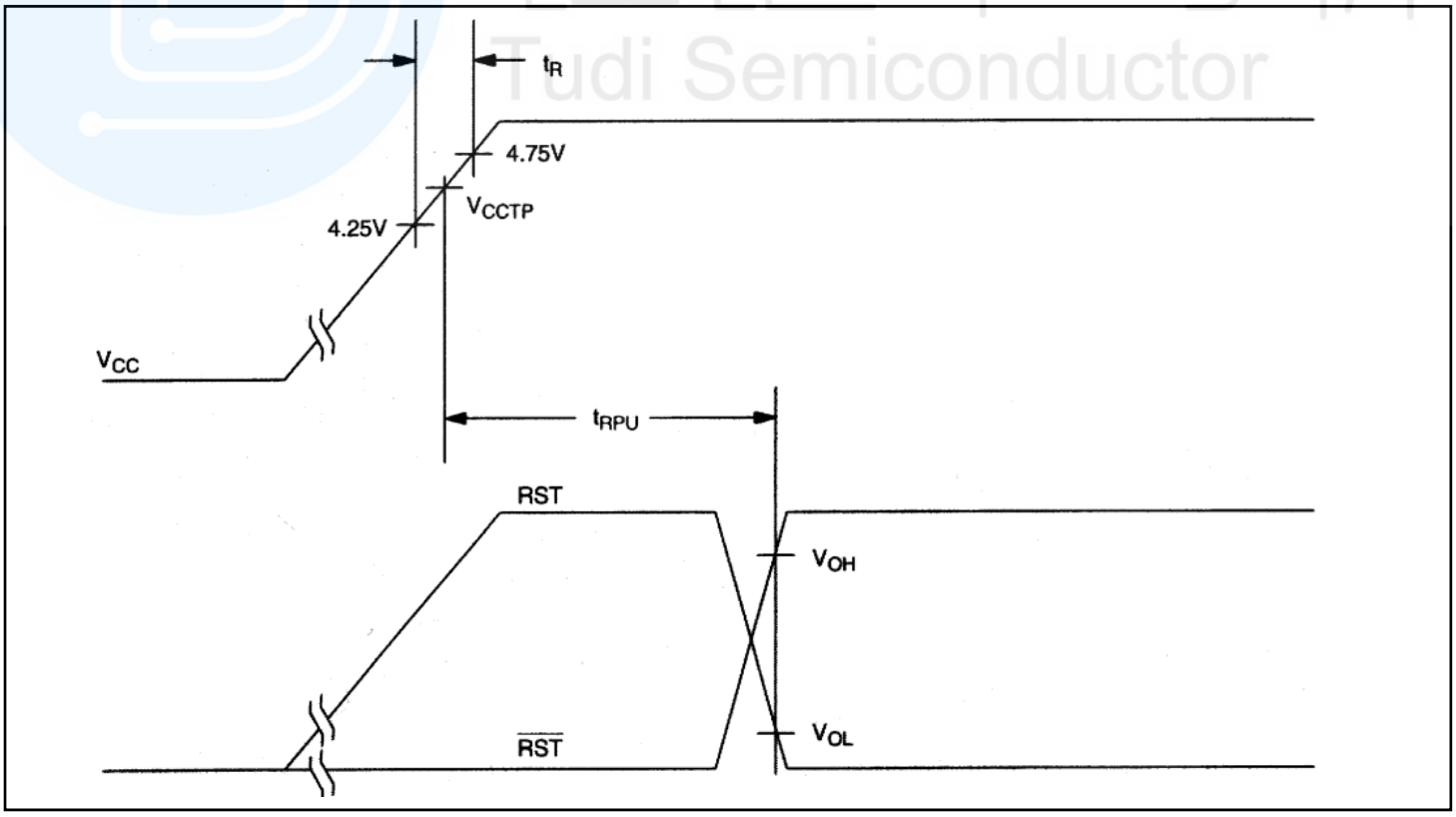


Figure 6 Timing diagram: power up

Recommended DC operating conditions (0℃ to 70℃)						
Parameter	Symbols	Min	Typ	Max	Units	Notes
Supply Voltage	Vcc	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	VH	2.0		Vcc+0.3	V	I
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V	-0.3		+0.8	V	I
Direct current electrical characteristics (0℃ to 70℃;Vcc=4.5 to 5.5V)						
Parameter	Symbols	Min	Typ	Max	Units	Notes
Input Leakage	IL	-1.0		+1.0	μA	3
Output Current @2.4V	IoH	-8	-10		mA	5
Output Current @0.4V	IoL	10			mA	
Low Level @RST	VoL			0.4	V	1
Output Voltage @-500 uA	VoH	Vcc-0.5V	Vcc-0.1V		V	17
Output Current(CMOS)	Icc1			50	μA	2
Operating Current(TTL)	Icc2		200	500	μA	8
Vcc Trip Point (TOL=GND)	VcCTP	4.50	4.62	4.74	V	1
Vcc Trip Point (TOL=Vcc)	VcCTP	4.25	4.37	4.49	V	1
Capacitance (tA=25℃)						
Parameter	Symbols	Min	Typ	Max	Units	Notes
Input Capacitance	CIN			5	pF	
Output Capacitance	CoUT			7	pF	
AC electrical characteristics (0℃ to 70℃;Vcc=5V±10%)						
Parameter	Symbols	Min	Typ	Max	Units	Notes
$\overline{PBRST}$=VI	tpB	20			ms	
RESET Active Time	tRST	250	610	1000	ms	
$\overline{ST}$ Pulse Width	tsT	20			ns	69
Vcc Fail Detect to RST and $\overline{RST}$	tRPD		50	175	μs	
Vcc Slew Rate 4.75V to 4.25V	tp	300			μs	
Vcc Detect to RST and $\overline{RST}$ Inactive	tRPU	250	610	1000	ms	4
Vcc Slew Rate 4.25V to 4.75V	tr	0			ns	
$\overline{PBRST}$ Stable Low to $\overline{RST}$ and RST	tpDLY			20	ms	

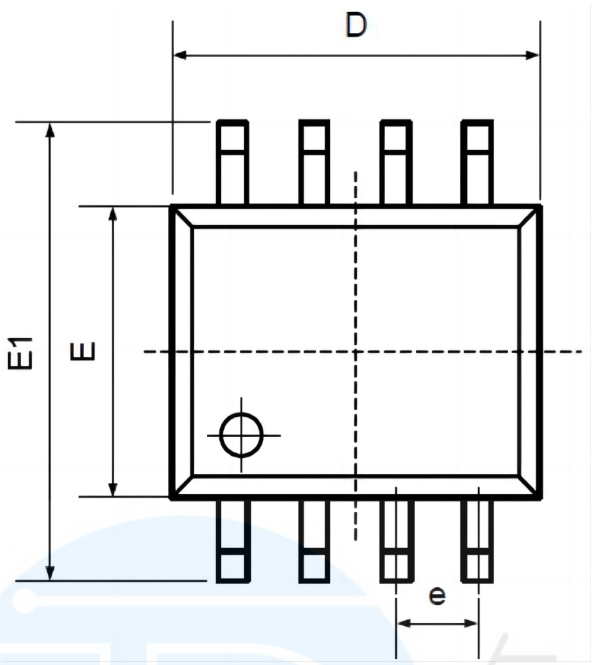
Notes:

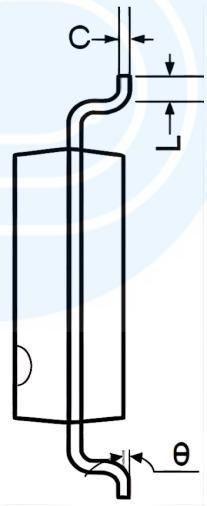
1. All voltages referenced to ground.
2. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ within 0.5V of supply rails.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40k typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open-drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.
8. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ at TTL levels.
9. Watchdog can not be disabled. It must be strobed to avoid resets.

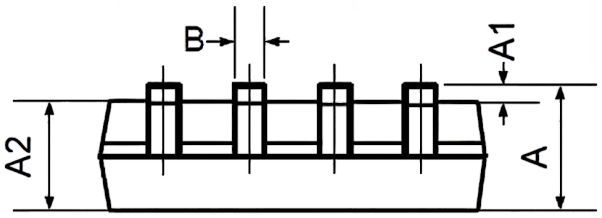
Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
ADM1232ANZ-TUDI	DIP8	Tube,50,A box of 2000	ADM1232ANZ	- 40°C to 85°C
ADM1232ARNZ-REEL-TUDI	SOP8	Tape,Reel,2500	ADM1232ARNZ	

Package SOP8

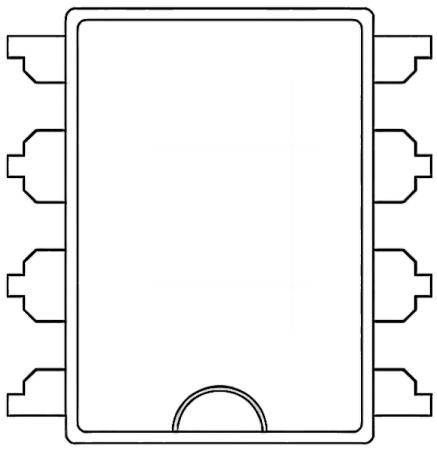


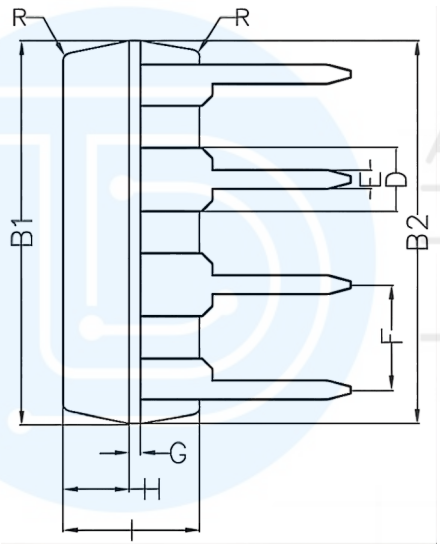


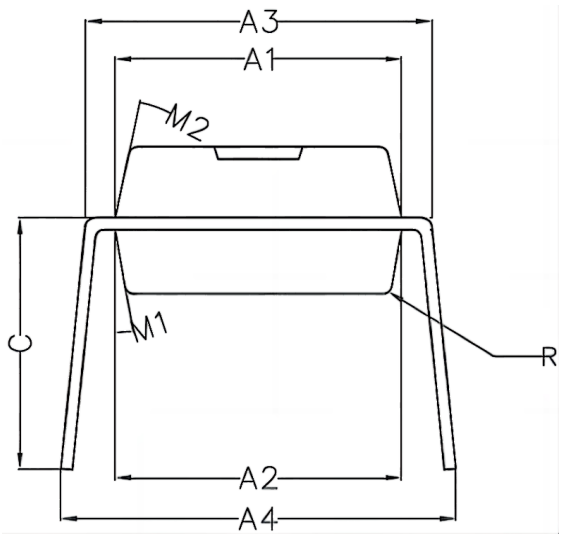


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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