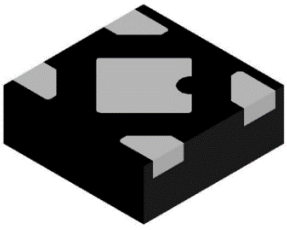
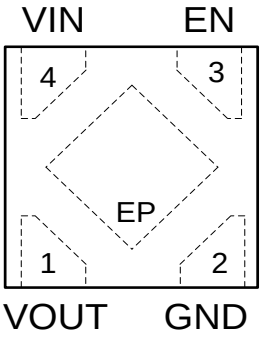
WL28631D

Ultra-Low Noise, High PSRR LDO, 400mA Linear Regulator for RF and Analog Circuits

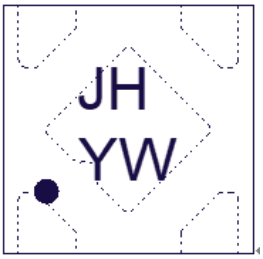
http://www.omnivision-group.com



DFN1X1-4L



Pin Configuration (Top View)



Marking

J: Device Code

H : Voltage Code

Y : Year Code

W: Week Codes

Marking of the WL28631D18-4/TR (Top View)

Descriptions

The WL28631D is a linear regulator capable of supplying 400mA output current. Designed to meet the requirements of RF and analog circuits, the WL28631D device provides low noise, high PSRR, low quiescent current and very good load /line transients.

The device is designed to work with a 1μF input and 1μF output ceramic capacitor (no separate noise bypass capacitor is required). Operation

The WL28631D regulators are available in standard DFN1x1-4L Package. Standard products are Pb-free and Halogen-free.

Features

- Input Voltage Range :2.2V~5.5V
- Output Voltage Range :1.8V~3.3V
- Output current :400mA
- PSRR :Typ.100dB at 10mA，f =1KHz
  :Typ. 45dB at 10mA , f =1MHz
- Low Dropout :Typ. 180mV at 400mA
- Quiescent current :Typ. 21μA
- Low Output Voltage Noise :Typ. 4.8 μV_{RMS}
- Output Voltage Tolerance :±2%,-40℃<T_A<85℃
- UVLO Threshold :Max. 1.7V (Falling)
- Recommend capacitor :1uF
- Stable with 1μF Ceramic Input and Output capacitor
- No Noise Bypass Capacitor Required
- Thermal-Overload Protection

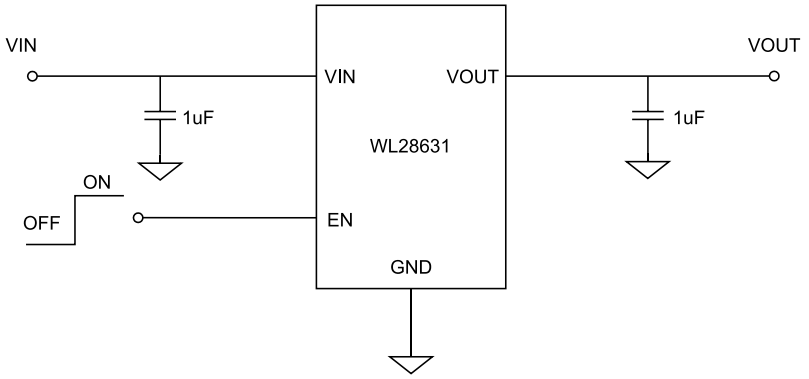
Applications

- Cell phones , radiophone, digital cameras
- Bluetooth, wireless handsets
- Hifi products
- Others portable electronics device

Order Information

For detail order information, please see page 13

Typical Application

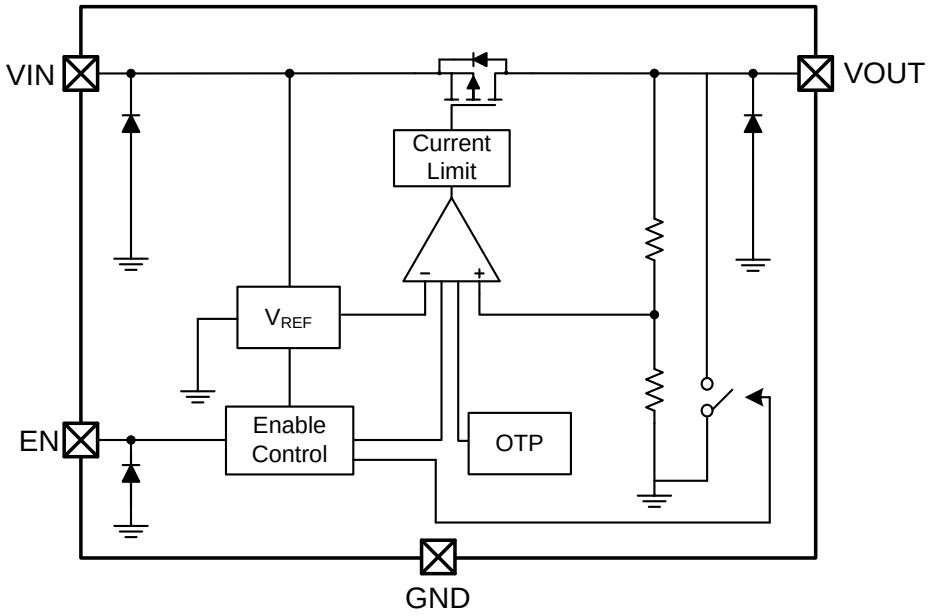


Note : A 1-uF or larger capacitor is required for stability both in the input and output side. The effective capacitance needs to take the DC-Bias characteristic, tolerance and temperature into consideration. The input and output capacitor must be located a distance of not more than 1 cm .

PIN Functions

PIN	Symbol	Description
1	VOUT	Regulated output voltage. 1μF capacitor should be connected at this input.
2	GND	Common ground connection.
3	EN	Driving the pin high turns on the regulator. Driving the pin low makes the regulator operate in the shutdown mode. The EN pin must not be left floating and needs to be connected to V_{IN} if not used.
4	VIN	Input voltage supply pin. 1μF capacitor should be connected at this input.
EP		Expose pad can be tied to ground plane for better power dissipation.

Block Diagram



Absolute Maximum Ratings

Parameter	Value	Unit
Power Dissipation, PD@TA=25℃	Internally Limited	mW
V_{IN} Range	-0.3～6.0	V
V_{EN} Range	−0.3 to V_{IN} + 0.3	V
V_{OUT} Range	−0.3 to V_{IN} + 0.3	V
I_{OUT}	Internally limited	
Lead Temperature Range	260	°C
Moisture Sensitivity Level	Level-1	
Storage Temperature Range	-55 ~ 150	°C
Operating Junction Temperature Range	150	°C
Thermal Resistance, $R_{\theta JA}$(Junction-to-Ambient Thermal Resistance)[1][2][3]	153	°C/W
Thermal Resistance, $R_{\theta JB}$(Junction-to-Board)[1][2][3]	117	°C/W
ESD Capability, Human Body Model, ESD_{HBM}	±2000	V
ESD Capability, Charge Device Model, ESD_{CDM}	±500	V

[1] Thermal resistance data is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

[2] Single component mounted on 2oz, 1.5*1.5 inch^2 FR4 PCB with 1.0*1.0 inch^2 Cu area.

[3] The test results are for reference only, if you need to compare with other company's products, it is recommended to do the comparison test under the same conditions to have the reference significance.

Recommend Operating Ratings

Parameter	Value	Unit
Operating Input Voltage Range [4]	2.2～5.5	V
Operating Output Voltage Range	1.8～3.3	V
Operating Enable Voltage Range[5]	0～3.3	V
Operating Output Current Range	1～400	mA
Operating Temperature Range	-40～85	°C

[4] In order to achieve high performance of PSRR, it is recommended that the V_{IN} needs to be no smaller than (V_{OUT}+0.5V).

[5] Enable Voltage should smaller than Input Voltage.

Electronics Characteristics

V_{IN}=$V_{OUT(NOM)}$+1V, C_{IN}=C_{OUT}=1uF, V_{EN} = 1.2 V. Typical values are at Ta = +25°C ,unless otherwise noted

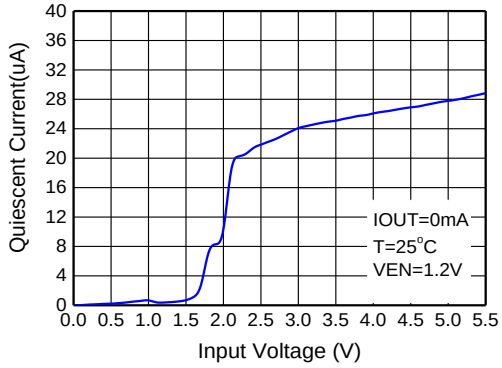
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating Input Voltage	V_{IN}			2.2		5.5	V
Output Voltage Accuracy	V_{OUT_acc}	V_{IN} = $V_{OUT(NOM)}$ + 1 V I_{OUT}=1mA, T_A=25℃		-1		+1	%
		V_{IN} = $V_{OUT(NOM)}$ + 1 V I_{OUT}=1mA, -40℃<T_A<85℃		-2*		+2*	%
Output Current Limit	I_{LIM}	V_{OUT} = 90% VOUT(NOM)		420	650		mA
Dropout Voltage	V_{DROP}	V_{OUT}=2.2$V_{(NOM)}$, I_{OUT}=400mA			220	340	mV
		V_{OUT}=2.8$V_{(NOM)}$, I_{OUT}=400mA			180	285	
		V_{OUT}=3.3$V_{(NOM)}$, I_{OUT}=400mA			165	242	
Line Regulation	$\triangle V_{LINE}$	V_{IN}=V_{OUT}+1V~5.5V ,I_{OUT}=1mA			0.1	5	mV
Load Regulation	$\triangle V_{Load}$	I_{OUT}=1~100mA			4.5	11	mV
Quiescent Current	I_Q	I_{OUT}=0mA			21	30	μA
Short Current*	I_{SHORT}	V_{OUT} short to GND			150		mA
Shut-down Current	I_{SHDN}	VEN =0 V, VIN = 5.5 V				1	μA
Power Supply Rejection Rate*	PSRR	I_{OUT} =10mA	f=100Hz f=1KHz f=100KHz f=1MHz		90 100 62 45		dB
EN logic high voltage	V_{ENH}	V_{IN}=5.5V, I_{OUT}=1mA		0.825			V
EN logic low voltage	V_{ENL}	V_{IN}=2.2V				0.4	V
EN Input Current	I_{EN}	V_{EN} = 5.5V				1	μA
Turn−On Time	T_{ON}	C_{OUT} = 1μF, From assertion of VEN to V_{OUT} = 90% V_{OUT} (NOM)	V_{OUT}=1.8V		0.52	1.1	mS
			V_{OUT}=2.2V		0.58	1.2	
			V_{OUT}=2.8V		0.68	1.4	
			V_{OUT}=3.3V		0.73	1.7	
Output Voltage Noise*	e_{NO}	10Hz to 100KHz,	V_{OUT}=1.8V I_{OUT} =200mA		4.8		μVRMS
Thermal shutdown threshold*	T_{SDH}	Temperature rising			150		°C
	T_{SDL}	Temperature falling			120		°C

Under voltage lock out threshold	V_{UVLO}	Falling，I_{OUT} = 1mA			1.7	V
Active Output Discharge Resistance	R_{LOW}	V_{IN}=4V, V_{EN}=0V，V_{OUT}=2.8V	200	390	550	Ω
Line Transient*	$Tran_{LINE}$	V_{IN} = ($V_{OUT(NOM)}$ + 2 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 us, I_{OUT} = 1 mA	−1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 2 V) in 30 us, I_{OUT} = 1 mA			+1	
Load Transient*	$Tran_{LOAD}$	I_{OUT} = 1 mA to 200 mA in 10 us	−10			mV
		I_{OUT} = 200 mA to 1 mA in 10 us			+10	

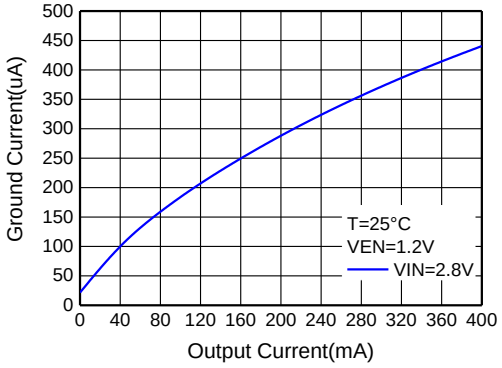
* Guaranteed by Design

Typical characteristics

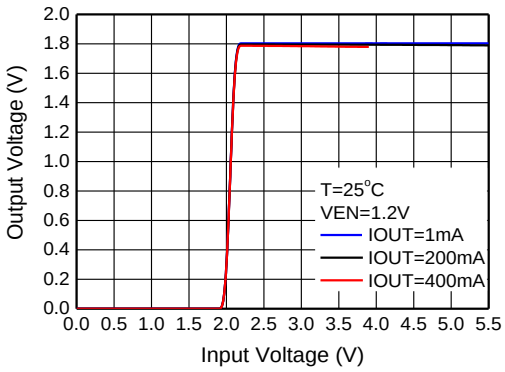
At VOUT=1.8 V, VIN=VOUT+1 V, IOUT=1 mA, CIN=1 μF, COUT=1 μF, VEN=1.2 V and Ta=+25°C, unless otherwise noted.



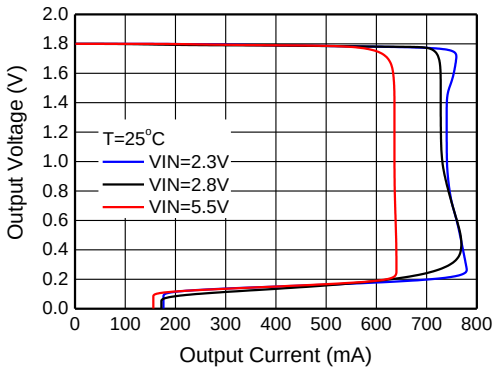
Quiescent current vs. Supply voltage



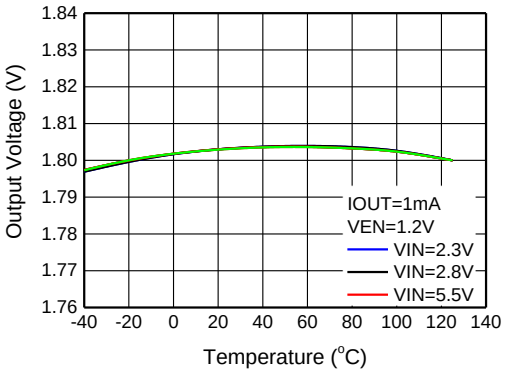
Ground Current vs. Load Current



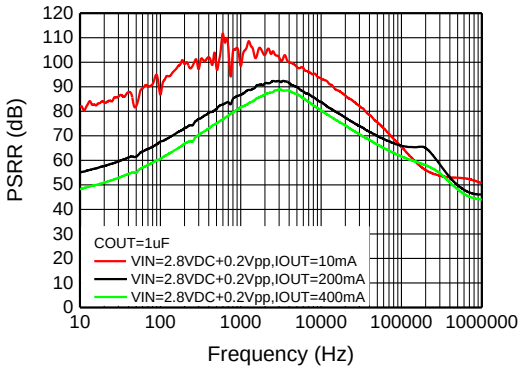
Output voltage vs. Supply voltage



Output voltage vs. Output current[6]



Output Voltage vs. Temperature

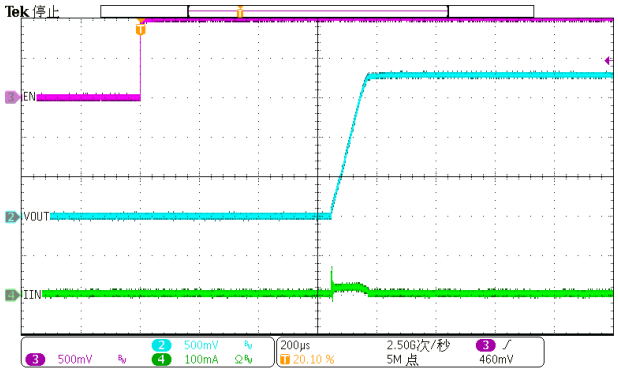


PSRR

[6] For the overload condition, the output current is limited since the LDO operates in the OCL mode. With the load increase in the process, the output voltage reduces while the output current is always around ICL. If V_{OUT} is lower than 0.2 V, the LDO enters the short mode and the output current equals to the short current I_{SHORT}.

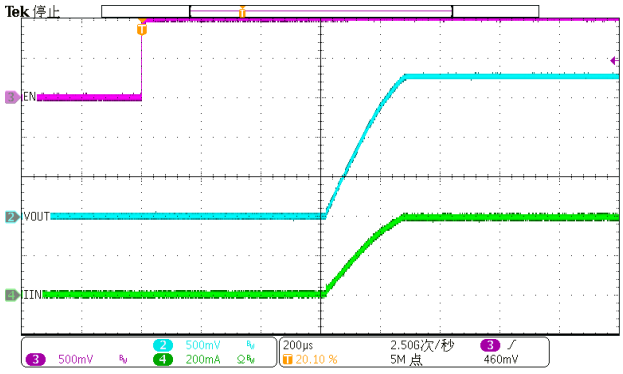
Typical characteristics

At VOUT=1.8 V, VIN=VOUT+1 V, IOUT=1 mA, CIN=1 μF, COUT=1 μF, VEN=1.2 V and Ta=+25°C, unless otherwise noted.



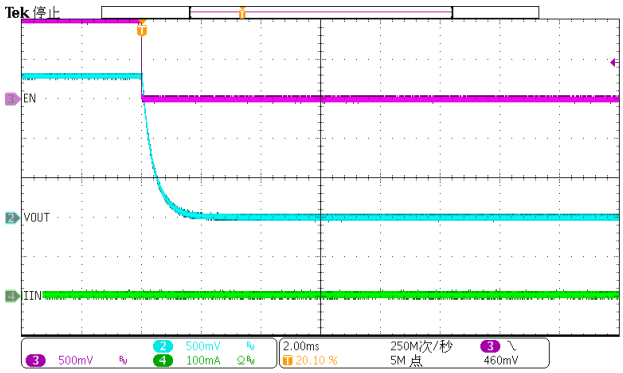
Soft-Start From EN

IOUT=0mA



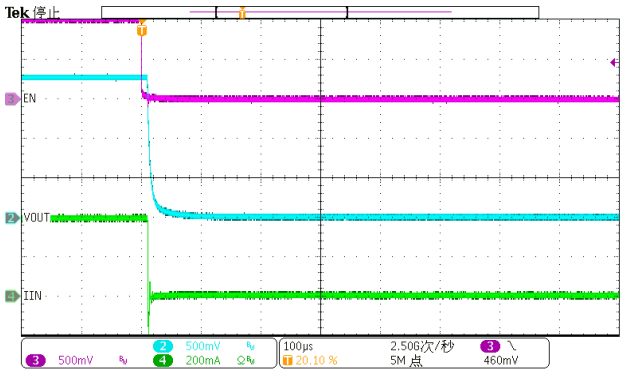
Soft-Start From EN

IOUT=400mA



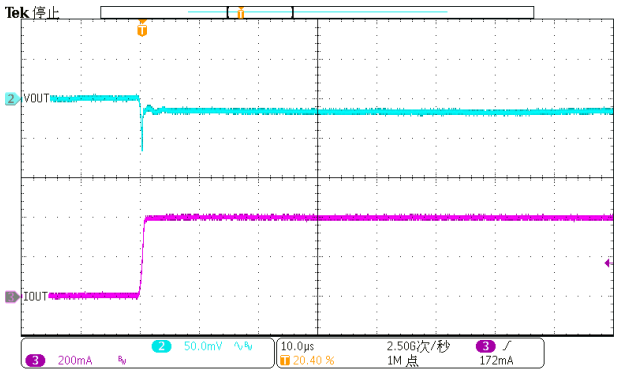
EN Shutdown

IOUT=0mA



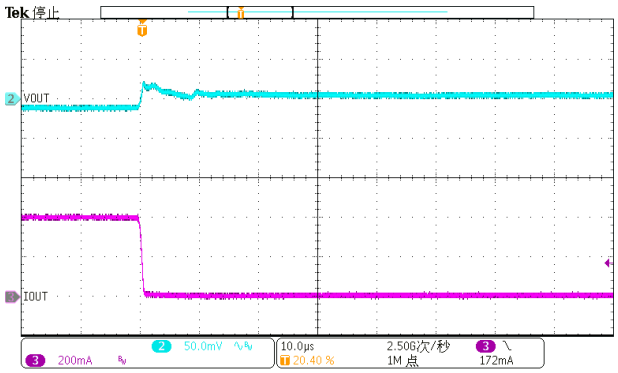
EN Shutdown

IOUT=400mA



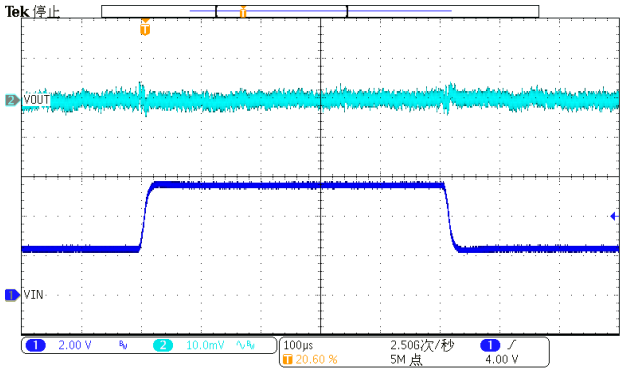
Load Transient Response

IOUT=1mA~400mA, rising time = 1uS



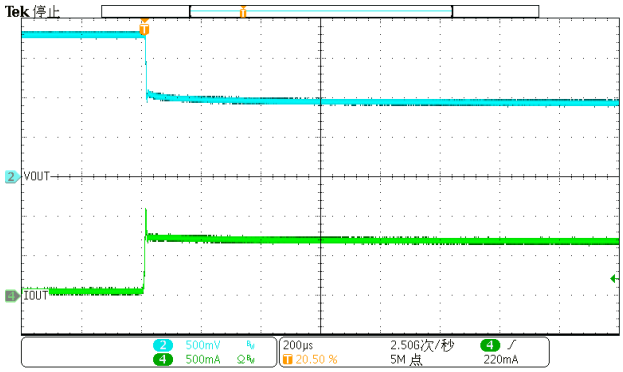
Load Transient Response

IOUT=400mA~1mA, Falling time = 1uS



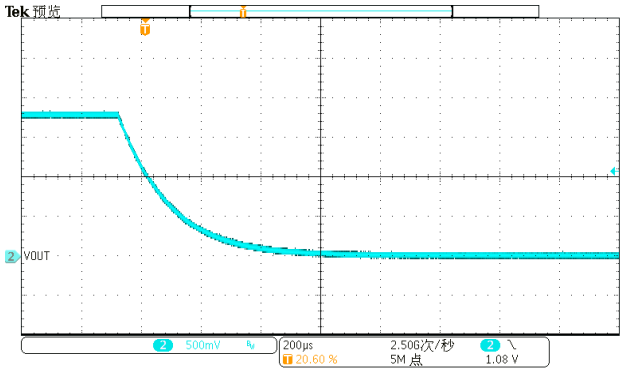
Line Transient Response

VIN=2.8V~5.5V,Rising time/Falling time = 10uS



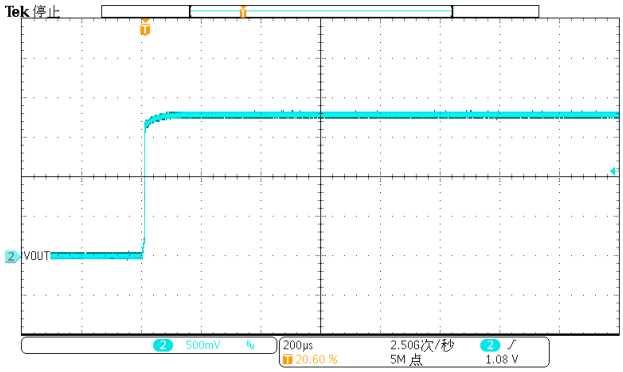
Vout OC Protection

IOUT = 100mA to OCP



Vout TSD Protection,

VIN=2.8V,IOUT=1mA,Thermal Shutdown Threshold



Vout TSD Protection,

VIN=2.8V,IOUT=1mA,Thermal Shutdown hysteresis

Function Description

Overview

The WL28631D series are general purpose high performance 400mA low dropout liner regulator. This series supports output voltages as low as 1.8V and as high as 3.3V.

The WL28631D series has 45 dB PSRR at 1MHz and 400mA load. The regulator features low noise of 4.8 uVRMS at 1.8V output voltage. The regulator also has very good line transient and load transient performance.

Input capacitor (CIN)

The input capacitor needs to be placed as close as possible to the device. It needs to be no smaller than 1uF.

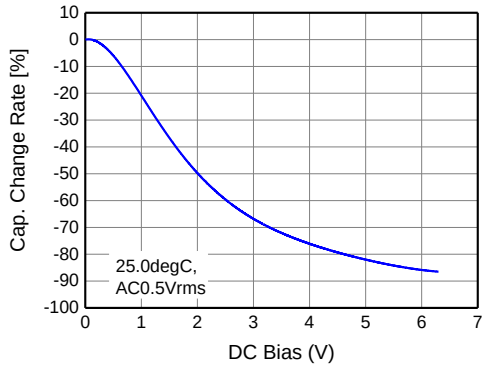
Usually, there is a certain amount of parasitic inductance on the power line, which can cause the chip to become less stable. Input capacitance of sufficient tolerance can weaken the influence of parasitic parameters on the chip at the input, which is beneficial to the stability. Also, this capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage. So, X7R, X5R MLCCs with good temperature characteristics are recommended.

Output capacitor (COUT)

The output capacitor needs to be placed as close as possible to the device.

Output capacitance is very important for system stability, and it is recommended to use MLCCs with high temperature characteristics and high DC voltage characteristics. Selecting capacitors with larger ESR can improve system stability, and selecting capacitors with smaller ESR can improve load transient and PSRR performance. Special attention should be paid to small package capacitors (e.g. 0201), whose capacitance value decreases sharply with the rise of DC voltage

Example: a 0201package MLCC effective value DC voltage charateristics.



Enable Operation

The LDO use EN (Enable pin) to enable and disable voltage converter function. When the voltage applied to the EN is greater than the EN Logic High Voltage, the converter will turn on the main power MOS to output the rated output voltage. When the voltage applied to EN is less than EN Logic Low Voltage, the converter will turn off the main power MOS tube, the auto discharge transistor is active so the output voltage is pulled to GND through 390 (typ.) resistor.

EN Logic High Voltage is not less than 0.825V and EN Logic Low Voltage is not greater than 0.4V. The EN is CMOS logic and cannot be left floating.

Output current limit

Output current is internally limited to a 650 mA typ.

For the overload condition, the output current is limited since the LDO operates in the OCL mode. With the load increase in the process, the output voltage reduces while the output current is always around ICL. If V_{OUT} is lower than 0.2 V, the LDO enters the short mode and the output current equals to the short current I_{SHORT}.

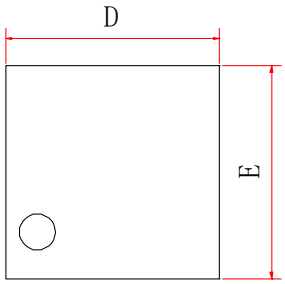
If the load is reduced below ICL, the chip will automatically exit OCL mode.

Over Temperature Protection

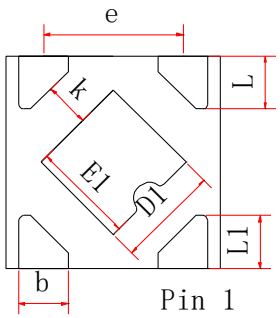
The chip will shut down when the temperature of the converter exceeds the OTP temperature. When the temperature drops below the OTP threshold, the LDO restores the output voltage. While the chip has an over-temperature protection function, do not allow the chip to operate in an over-temperature condition for a long period of time. This behavior may reduce the life of the chip and lower the reliability of the product.

PACKAGE OUTLINE DIMENSIONS

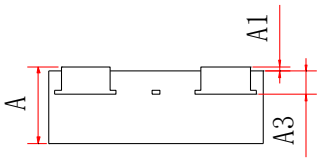
DFN1x1-4L



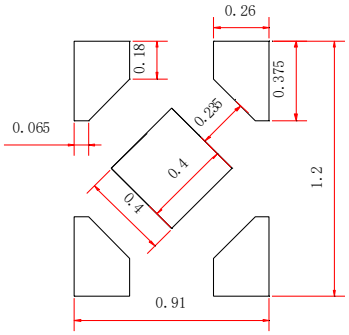
TOP VIEW



BOTTOM VIEW



SIDE VIEW

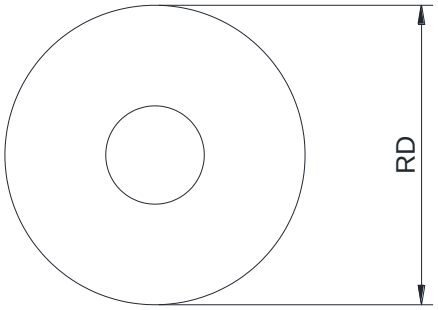


RECOMMENDED LAND PATTERN(unit:mm)

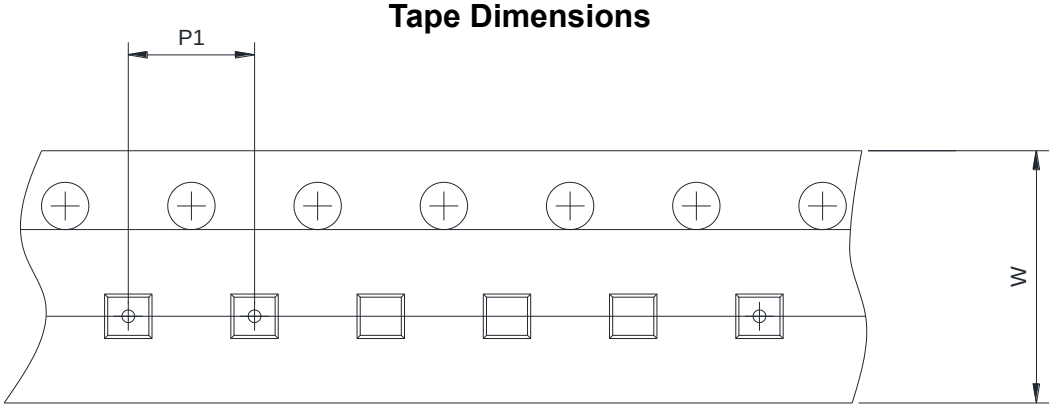
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.32	0.36	0.40
A1	-0.004	-	0.046
A3	0.110 REF		
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D1	0.43	0.48	0.53
E1	0.43	0.48	0.53
K	0.15	-	-
b	0.18	0.23	0.28
e	0.65 TYP.		
L	0.20	0.25	0.30
L1	0.20	0.25	0.30

TAPE AND REEL INFORMATION

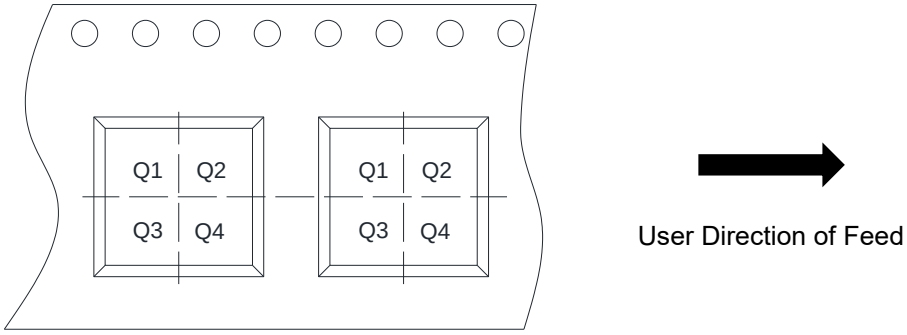
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☑ 2mm	☐ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

ORDER INFORMATION

Ordering No.	Vout (V)	Package	Operating Temperature	Marking	Shipping
WL28631D18-4/TR	1.8	DFN1x1-4L	-40~+85°C	JH YW	Tape and Reel, 10000
WL28631D22-4/TR	2.2	DFN1x1-4L	-40~+85°C	JJ YW	Tape and Reel, 10000
WL28631D25-4/TR	2.5	DFN1x1-4L	-40~+85°C	JK YW	Tape and Reel, 10000
WL28631D28-4/TR	2.8	DFN1x1-4L	-40~+85°C	JL YW	Tape and Reel, 10000
WL28631D285-4/TR	2.85	DFN1x1-4L	-40~+85°C	JV YW	Tape and Reel, 10000
WL28631D30-4/TR	3.0	DFN1x1-4L	-40~+85°C	JM YW	Tape and Reel, 10000
WL28631D29-4/TR	2.9	DFN1x1-4L	-40~+85°C	Jg YW	Tape and Reel, 10000
WL28631D33-4/TR	3.3	DFN1x1-4L	-40~+85°C	JN YW	Tape and Reel, 10000