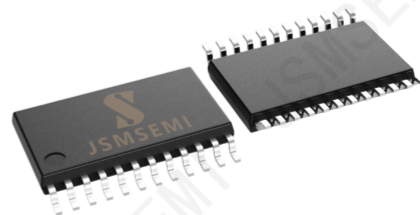


General Description

The 74HC/HCT4067 is a single-pole 16-throw analog switch (SP16T) suitable for use in analog or digital 16:1 multiplexer/demultiplexer applications. The switch features four digital select inputs (S0, S1, S2 and S3), sixteen independent inputs/outputs (Yn), a common input/output (Z) and a digital enable input (E). When E is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .



Features:

- Input levels S0, S1, S2, S3 and $\bar{E}$ inputs:
For 74HC4067: CMOS level
For 74HCT4067: TTL level
- Low ON resistance:
 - 80 Ω (typical) at $V_{CC} = 4.5\text{ V}$
 - 70 Ω (typical) at $V_{CC} = 6.0\text{ V}$
 - 60 Ω (typical) at $V_{CC} = 9.0\text{ V}$
- Typical “break before make” built-in
- Specified from -40°C to $+125^{\circ}\text{C}$
- Packaging information: SOP24/TSSOP24

Applications:

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

2、Block Diagram And Pin Description

2.1、Block Diagram

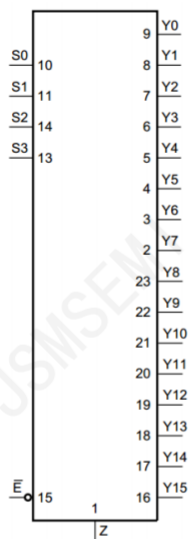


Figure 1. Logic symbol

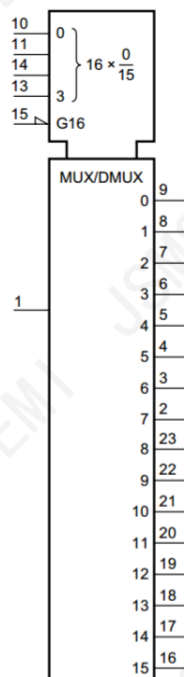


Figure 2. IEC logic symbol

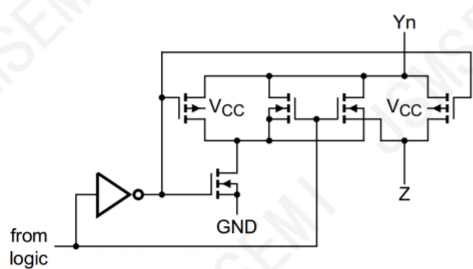


Figure 3. Schematic diagram (one switch)

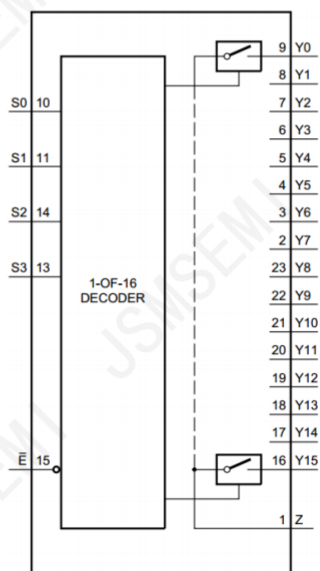


Figure 4. Functional diagram

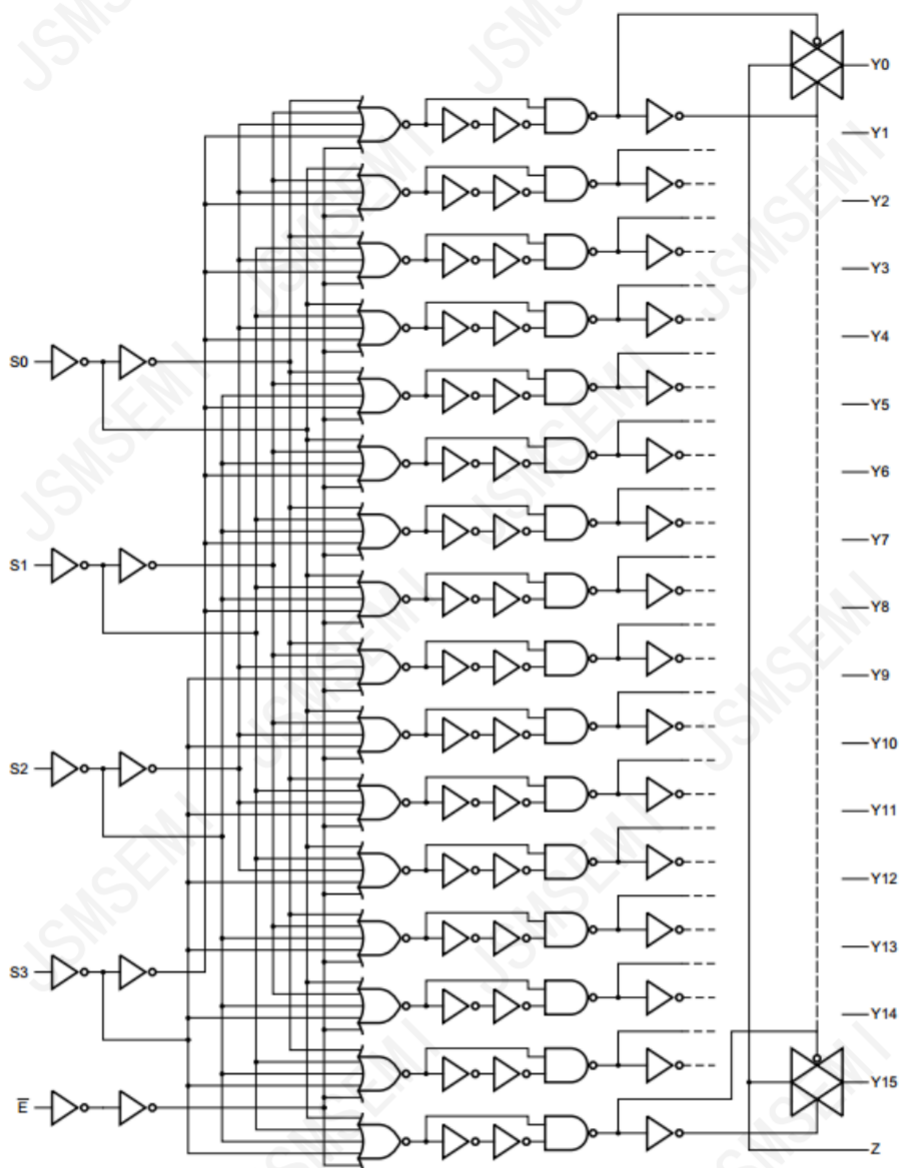
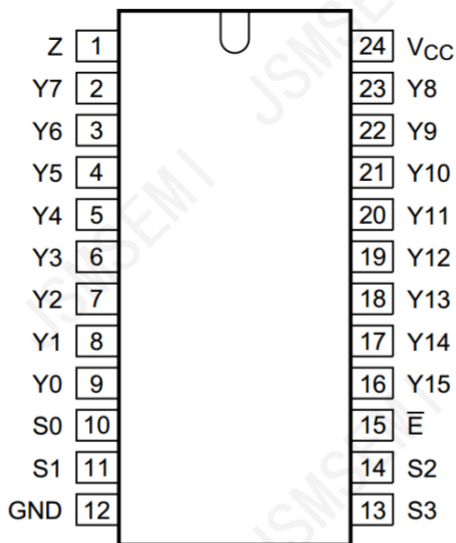


Figure 5. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	Z	common input or output
2	Y7	independent input or output
3	Y6	independent input or output
4	Y5	independent input or output
5	Y4	independent input or output
6	Y3	independent input or output
7	Y2	independent input or output
8	Y1	independent input or output
9	Y0	independent input or output
10	S0	address input 0
11	S1	address input 0
12	GND	ground (0 V)
13	S3	address input 0
14	S2	address input 0
15	$\bar{E}$	enable input (active LOW)
16	Y15	independent input or output
17	Y14	independent input or output
18	Y13	independent input or output
19	Y12	independent input or output
20	Y11	independent input or output
21	Y10	independent input or output
22	Y9	independent input or output
23	Y8	independent input or output
24	V _{CC}	supply voltage

2.4、Function Table

Input					Channel ON
$\bar{E}$	S3	S2	S1	S0	
L	L	L	L	L	Y0 to Z
L	L	L	L	H	Y1 to Z
L	L	L	H	L	Y2 to Z
L	L	L	H	H	Y3 to Z
L	L	H	L	L	Y4 to Z
L	L	H	L	H	Y5 to Z
L	L	H	H	L	Y6 to Z
L	L	H	H	H	Y7 to Z
L	H	L	L	L	Y8 to Z
L	H	L	L	H	Y9 to Z
L	H	L	H	L	Y10 to Z
L	H	L	H	H	Y11 to Z
L	H	H	L	L	Y12 to Z
L	H	H	L	H	Y13 to Z
L	H	H	H	L	Y14 to Z
L	H	H	H	H	Y15 to Z
H	X	X	X	X	-

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	- [1]	-0.5	+11.0	V
input clamping current	I_{IK}	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
switch clamping current	I_{SK}	$V_{SW} < -0.5\text{ V}$ or $V_{SW} > V_{CC} + 0.5\text{ V}$	-	± 20	mA
switch current	I_{SW}	$V_{SW} = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	± 25	mA
supply current	I_{CC}	-	-	+50	mA
ground current	I_{GND}	-	-50	-	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	- [2]	-	500	mW
power dissipation	P	per switch	-	100	mW
Soldering temperature	T_L	10s	260		°C

Note:

[1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows into terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or GND.

[2] For SOP24 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.

For TSSOP24 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
74HC4067						
supply voltage	V _{CC}	-	3.0	5.0	9.0	V
input voltage	V _I	-	0	-	V _{CC}	V
switch voltage	V _{SW}	-	0	-	V _{CC}	V
ambient temperature	T _{amb}	in free air	-40	-	+125	°C
input transition rise and fall rate	Δt/ΔV	V _{CC} = 4.5 V	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	ns/V
		V _{CC} = 9.0 V	-	-	31	ns/V
74HCT4067						
supply voltage	V _{CC}	-	4.5	5.0	5.5	V
input voltage	V _I	-	0	-	V _{CC}	V
switch voltage	V _{SW}	-	0	-	V _{CC}	V
ambient temperature	T _{amb}	in free air	-40	-	+125	°C
input transition rise and fall rate	Δt/ΔV	V _{CC} = 4.5 V	-	1.67	139	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	$V_{is}=V_{CC}$ to GND; $I_{SW}=1000\text{ }\mu\text{A}$	$V_{CC}=4.5\text{ V}$	-	110	180	Ω
			$V_{CC}=6.0\text{ V}$	-	95	160	Ω
			$V_{CC}=9.0\text{ V}$	-	75	130	Ω
ON resistance (rail)	$R_{ON(rail)}$	$V_{is}=\text{GND or }V_{CC}$ $I_{SW}=1000\text{ }\mu\text{A}$	$V_{CC}=4.5\text{ V}$	-	90	160	Ω
			$V_{CC}=6.0\text{ V}$	-	80	140	Ω
			$V_{CC}=9.0\text{ V}$	-	70	120	Ω
ON resistance mismatch between channels	ΔR_{ON}	$V_{is}=V_{CC}$ to GND	$V_{CC}=4.5\text{ V}$	-	9	-	Ω
			$V_{CC}=6.0\text{ V}$	-	8	-	Ω
			$V_{CC}=9.0\text{ V}$	-	6	-	Ω
74HC4067							
HIGH-level input voltage	V_{IH}	$V_{CC}=4.5\text{ V}$		3.15	2.4	-	V
		$V_{CC}=6.0\text{ V}$		4.2	3.2	-	V
		$V_{CC}=9.0\text{ V}$		6.3	4.7	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=4.5\text{ V}$		-	2.1	1.35	V
		$V_{CC}=6.0\text{ V}$		-	2.8	1.80	V
		$V_{CC}=9.0\text{ V}$		-	4.3	2.70	V
input leakage current	I_I	$V_I=V_{CC}$ or GND	$V_{CC}=6.0\text{ V}$	-	-	± 0.1	μA
			$V_{CC}=9.0\text{ V}$	-	-	± 0.2	μA
OFF-state leakage current	$I_{S(OFF)}$	$V_{CC}=9.0\text{ V};$ $V_I=V_{IH}$ or $V_{IL};$ $ V_{SW} =V_{CC}-\text{GND};$ see Figure 8	per channel	-	-	± 0.1	μA
			all channels	-	-	± 0.8	μA
ON-state leakage current	$I_{S(ON)}$	$V_{CC}=9.0\text{ V}; V_I=V_{IH}$ or $V_{IL};$ $ V_{SW} =V_{CC}-\text{GND};$ see Figure 9		-	-	± 0.8	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $V_{is}=\text{GND or }V_{CC};$ $V_{os}=V_{CC}$ or GND	$V_{CC}=6.0\text{ V}$	-	-	8.0	μA
			$V_{CC}=9.0\text{ V}$	-	-	16.0	μA
input capacitance	C_I	-		-	3.5	-	pF
74HCT4067							
HIGH-level input voltage	V_{IH}	$V_{CC}=4.5\text{ V to }5.5\text{ V}$		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=4.5\text{ V to }5.5\text{ V}$		-	1.2	0.8	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=5.5\text{ V}$		-	-	± 0.1	μA

OFF-state leakage current	$I_{S(OFF)}$	$V_{CC}=5.5\text{ V};$ $V_I=V_{IH}\text{ or }V_{IL};$ $ V_{SW} =V_{CC}-GND;$ see Figure 8	per channel	-	-	± 0.1	μA
			all channels	-	-	± 0.8	μA
ON-state leakage current	$I_{S(ON)}$	$V_{CC}=5.5\text{ V};$ $V_I=V_{IH}\text{ or }V_{IL}; V_{SW} =$ $V_{CC}-GND;$ see Figure 9	-	-	-	± 0.8	μA
supply current	I_{CC}	$V_I=V_{CC}\text{ or }GND;$ $V_{is}=GND\text{ or }V_{CC};$ $V_{os}=V_{CC}\text{ or }GND;$ $V_{CC}=4.5\text{ V to }5.5\text{ V}$	-	-	-	8.0	μA
additional supply current	ΔI_{CC}	per input pin; $V_I=V_{CC}-2.1\text{ V};$ other inputs at $V_{CC}\text{ or }GND;$ $V_{CC}=4.5\text{ V to }5.5\text{ V}$	pin $\bar{E}$	-	60	216	μA
			pin Sn	-	50	180	μA
input capacitance	C_I	-	-	3.5	-	-	pF

Note:

[1] $V_I=V_{IH}\text{ or }V_{IL};$ for test circuit see Figure 6.

[2] V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

[3] V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}\sim 85^{\circ}\text{C}$, voltages are reference to GND (ground=0V), unless otherwise specified, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	$V_{is} = V_{CC}$ to GND; $I_{SW} = 1000\text{ uA}$	$V_{CC} = 4.5\text{ V}$	-	-	225	Ω
			$V_{CC} = 6.0\text{ V}$	-	-	200	Ω
			$V_{CC} = 9.0\text{ V}$	-	-	165	Ω
ON resistance (rail)	$R_{ON(rail)}$	$V_{is} = \text{GND or } V_{CC}$ $I_{SW} = 1000\text{ uA}$	$V_{CC} = 4.5\text{ V}$	-	-	200	Ω
			$V_{CC} = 6.0\text{ V}$	-	-	175	Ω
			$V_{CC} = 9.0\text{ V}$	-	-	150	Ω
74HC4067							
HIGH-level input voltage	V_{IH}	$V_{CC} = 4.5\text{ V}$		3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$		4.2	-	-	V
		$V_{CC} = 9.0\text{ V}$		6.3	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC} = 4.5\text{ V}$		-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$		-	-	1.80	V
		$V_{CC} = 9.0\text{ V}$		-	-	2.70	V
input leakage	I_I	$V_I = V_{CC}$ or GND	$V_{CC} = 6.0\text{ V}$	-	-	± 1.0	μA

current			V _{CC} = 9.0 V	-	-	±2.0	uA
OFF-state leakage current	I _{S(OFF)}	V _{CC} = 9.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Figure 8	per channel	-	-	±1.0	uA
			all channels	-	-	±8.0	uA
ON-state leakage current	I _{S(ON)}	V _{CC} = 9.0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Figure 9		-	-	±8.0	uA
supply current	I _{CC}	V _I = V _{CC} or GND; V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND	V _{CC} = 6.0 V	-	-	80.0	uA
			V _{CC} = 9.0 V	-	-	160.0	uA
74HCT4067							
HIGH-level input voltage	V _{IH}	V _{CC} = 4.5 V to 5.5 V		2.0	-	-	V
LOW-level input voltage	V _{IL}	V _{CC} = 4.5 V to 5.5 V		-	-	0.8	V
input leakage current	I _I	V _I = V _{CC} or GND; V _{CC} = 5.5 V		-	-	±1.0	uA
OFF-state leakage current	I _{S(OFF)}	V _{CC} = 5.5V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - GND; see Figure 8	per channel	-	-	±1.0	uA
			all channels	-	-	±8.0	uA
ON-state leakage current	I _{S(ON)}	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} -GND; see Figure 9		-	-	±8.0	uA
supply current	I _{CC}	V _I = V _{CC} or GND; V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND; V _{CC} = 4.5 V to 5.5V		-	-	80.0	uA
additional supply current	ΔI _{CC}	per input; V _I = V _{CC} - 2.1V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	pin $\bar{E}$	-	-	270	uA
			pin Sn	-	-	225	uA

Note:

[1] $V_I = V_{IH} \text{ or } V_{IL}$; for test circuit see Figure 6.

[2] V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

[3] V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

3.3.3、DC Characteristics 3

($T_{amb} = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$, voltages are reference to GND (ground=0V), unless otherwise specified, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ON resistance (peak)	$R_{\text{ON(peak)}}$	$V_{\text{is}} = V_{\text{CC}}$ to GND; $I_{\text{SW}} = 1000 \text{ uA}$	$V_{\text{CC}} = 4.5 \text{ V}$	-	-	270	Ω
			$V_{\text{CC}} = 6.0 \text{ V}$	-	-	240	Ω
			$V_{\text{CC}} = 9.0 \text{ V}$	-	-	195	Ω
ON resistance (rail)	$R_{\text{ON(rail)}}$	$V_{\text{is}} = \text{GND or } V_{\text{CC}}$ $I_{\text{SW}} = 1000 \text{ uA}$	$V_{\text{CC}} = 4.5 \text{ V}$	-	-	240	Ω
			$V_{\text{CC}} = 6.0 \text{ V}$	-	-	210	Ω
			$V_{\text{CC}} = 9.0 \text{ V}$	-	-	180	Ω
74HC4067							
HIGH-level input voltage	V_{IH}	$V_{\text{CC}} = 4.5 \text{ V}$		3.15	-	-	V
		$V_{\text{CC}} = 6.0 \text{ V}$		4.2	-	-	V
		$V_{\text{CC}} = 9.0 \text{ V}$		6.3	-	-	V
LOW-level input voltage	V_{IL}	$V_{\text{CC}} = 4.5 \text{ V}$		-	-	1.35	V
		$V_{\text{CC}} = 6.0 \text{ V}$		-	-	1.80	V
		$V_{\text{CC}} = 9.0 \text{ V}$		-	-	2.70	V
input leakage current	I_{I}	$V_{\text{I}} = V_{\text{CC}}$ or GND	$V_{\text{CC}} = 6.0 \text{ V}$	-	-	± 1.0	uA
			$V_{\text{CC}} = 9.0 \text{ V}$	-	-	± 2.0	uA
OFF-state leakage current	$I_{\text{S(OFF)}}$	$V_{\text{CC}} = 9.0 \text{ V};$ $V_{\text{I}} = V_{\text{IH}}$ or $V_{\text{IL}};$ $ V_{\text{SW}} = V_{\text{CC}} - \text{GND};$ see Figure 8	per channel	-	-	± 1.0	uA
			all channels	-	-	± 8.0	uA
ON-state leakage current	$I_{\text{S(ON)}}$	$V_{\text{CC}} = 9.0 \text{ V}; V_{\text{I}} = V_{\text{IH}}$ or $V_{\text{IL}};$ $ V_{\text{SW}} = V_{\text{CC}} - \text{GND};$ see Figure 9		-	-	± 8.0	uA
supply current	I_{CC}	$V_{\text{I}} = V_{\text{CC}}$ or GND; $V_{\text{is}} = \text{GND or } V_{\text{CC}};$ $V_{\text{os}} = V_{\text{CC}}$ or GND	$V_{\text{CC}} = 6.0 \text{ V}$	-	-	160.0	uA
			$V_{\text{CC}} = 9.0 \text{ V}$	-	-	320.0	uA
74HCT4067							
HIGH-level input voltage	V_{IH}	$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$		2.0	-	-	V
LOW-level input voltage	V_{IL}	$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$		-	-	0.8	V
input leakage current	I_{I}	$V_{\text{I}} = V_{\text{CC}}$ or GND; $V_{\text{CC}} = 5.5 \text{ V}$		-	-	± 1.0	uA
OFF-state leakage current	$I_{\text{S(OFF)}}$	$V_{\text{CC}} = 5.5\text{V};$ $V_{\text{I}} = V_{\text{IH}}$ or $V_{\text{IL}};$	per channel	-	-	± 1.0	uA

		$ V_{SW} =V_{CC}-GND$; see Figure 8	all channels	-	-	± 8.0	μA
ON-state leakage current	$I_{S(ON)}$	$V_{CC}=5.5V$; $V_I=V_{IH}$ or V_{IL} ; $ V_{SW} =V_{CC}-GND$; see Figure 9		-	-	± 8.0	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND ; $V_{is}=GND$ or V_{CC} ; $V_{os}=V_{CC}$ or GND ; $V_{CC}=4.5V$ to $5.5V$		-	-	160.0	μA
additional supply current	ΔI_{CC}	per input; $V_I=V_{CC}-2.1V$; other inputs at V_{CC} or GND ; $V_{CC}=4.5V$ to $5.5V$	pin $\bar{E}$	-	-	294	μA
			pin S_n	-	-	245	μA

Note:

[1] $V_I=V_{IH}$ or V_{IL} ; for test circuit see Figure 6.

[2] V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.

[3] V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

3.3.4、AC Characteristics 1

($T_{amb}=25^\circ C$, $GND=0V$; $t_r=t_f=6ns$; $C_L=50pF$; unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
74HC4067						
propagation delay	t_{pd}	Y_n to Z ; see Figure 10 ^{[1][2]}	$V_{CC}=4.5V$	-	9	15 ns
			$V_{CC}=6.0V$	-	7	13 ns
			$V_{CC}=9.0V$	-	5	9 ns
		Z to Y_n ; see Figure 10 ^{[1][2]}	$V_{CC}=4.5V$	-	6	12 ns
			$V_{CC}=6.0V$	-	5	10 ns
			$V_{CC}=9.0V$	-	4	8 ns
turn-off time	t_{off}	$\bar{E}$ to Y_n ; see Figure 11 ^[3]	$V_{CC}=4.5V$	-	27	50 ns
			$V_{CC}=5.0V$; $C_L=15pF$	-	27	- ns
			$V_{CC}=6.0V$	-	22	43 ns
			$V_{CC}=9.0V$	-	20	38 ns
		S_n to Y_n ; see Figure 11 ^[3]	$V_{CC}=4.5V$	-	30	50 ns
			$V_{CC}=5.0V$; $C_L=15pF$	-	29	- ns
			$V_{CC}=6.0V$	-	24	43 ns
			$V_{CC}=9.0V$	-	21	38 ns
		$\bar{E}$ to Z ;	$V_{CC}=4.5V$	-	31	55 ns
			$V_{CC}=6.0V$	-	25	47 ns

		see Figure 11 ^[3]	V _{CC} = 9.0 V	-	24	42	ns		
		Sn to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	34	58	ns		
			V _{CC} = 6.0 V	-	27	47	ns		
			V _{CC} = 9.0 V	-	25	45	ns		
turn-on time	t _{on}	$\bar{E}$ to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	29	55	ns		
			V _{CC} = 5.0 V; C _L = 15 pF	-	26	-	ns		
			V _{CC} = 6.0 V	-	23	47	ns		
			V _{CC} = 9.0 V	-	17	42	ns		
		Sn to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	32	60	ns		
			V _{CC} = 5.0 V; C _L = 15 pF	-	29	-	ns		
			V _{CC} = 6.0 V	-	26	51	ns		
			V _{CC} = 9.0 V	-	18	45	ns		
		$\bar{E}$ to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	31	55	ns		
			V _{CC} = 6.0 V	-	25	47	ns		
			V _{CC} = 9.0 V	-	18	42	ns		
		Sn to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	34	60	ns		
			V _{CC} = 6.0 V	-	27	51	ns		
			V _{CC} = 9.0 V	-	19	45	ns		
		power dissipation capacitance	C _{PD}	per switch; V _I = GND to V _{CC} ^[4]		-	29	-	pF
		74HCT4067							
propagation delay	t _{pd}	Y _n to Z; see Figure 10 ^{[1][2]}	V _{CC} = 4.5 V	-	9	15	ns		
		Z to Y _n ; see Figure 10 ^{[1][2]}	V _{CC} = 4.5 V	-	6	12	ns		
turn-off time	t _{off}	$\bar{E}$ to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	26	55	ns		
			V _{CC} = 5.0 V; C _L = 15 pF	-	26	-	ns		
		Sn to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	31	55	ns		
			V _{CC} = 5.0 V; C _L = 15 pF	-	30	-	ns		
		$\bar{E}$ to Z;	V _{CC} = 4.5 V	-	30	60	ns		

		see Figure 11 ^[3]					
		Sn to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	35	60	ns
turn-on time	t _{on}	$\bar{E}$ to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	32	60	ns
			V _{CC} = 5.0 V; C _L = 15 pF	-	32	-	ns
		Sn to Y _n ; see Figure 10 ^[3]	V _{CC} = 4.5 V	-	35	60	ns
			V _{CC} = 5.0 V; C _L = 15 pF	-	33	-	ns
		$\bar{E}$ to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	38	65	ns
		Sn to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	38	65	ns
power dissipation capacitance	C _{PD}	per switch; V _I = GND to V _{CC} -1.5V ^[4]		-	29	-	pF

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3] t_{on} is the same as t_{pZH} and t_{pZL}.

[4] t_{off} is the same as t_{pHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\Sigma\{(C_L + C_{SW}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{SW} = switch capacitance in pF;

V_{CC} = supply voltage in V.

[5] For test circuit see Figure 12.

[6] V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

3.3.5、AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$; $GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit		
74HC4067								
propagation delay	t _{pd}	Y _n to Z; see Figure 10 ^{[1][2]}	V _{CC} = 4.5 V	-	-	19	ns	
			V _{CC} = 6.0 V	-	-	16	ns	
			V _{CC} = 9.0 V	-	-	11	ns	
		Z to Y _n ; see Figure 10 ^{[1][2]}	V _{CC} = 4.5 V	-	-	15	ns	
			V _{CC} = 6.0 V	-	-	13	ns	
			V _{CC} = 9.0 V	-	-	10	ns	
turn-off time	t _{off}	$\bar{E}$ to Y _n ; see Figure 10 ^[3]	V _{CC} = 4.5 V	-	-	63	ns	
			V _{CC} = 6.0 V	-	-	54	ns	
			V _{CC} = 9.0 V	-	-	48	ns	
		S _n to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	63	ns	
			V _{CC} = 6.0 V	-	-	54	ns	
			V _{CC} = 9.0 V	-	-	48	ns	
		$\bar{E}$ to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	69	ns	
			V _{CC} = 6.0 V	-	-	59	ns	
			V _{CC} = 9.0 V	-	-	53	ns	
		S _n to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	73	ns	
			V _{CC} = 6.0 V	-	-	62	ns	
			V _{CC} = 9.0 V	-	-	56	ns	
turn-on time	t _{on}	$\bar{E}$ to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	69	ns	
			V _{CC} = 6.0 V	-	-	59	ns	
			V _{CC} = 9.0 V	-	-	53	ns	
		S _n to Y _n ; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	75	ns	
			V _{CC} = 6.0 V	-	-	64	ns	
			V _{CC} = 9.0 V	-	-	56	ns	
		$\bar{E}$ to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	69	ns	
			V _{CC} = 6.0 V	-	-	59	ns	
			V _{CC} = 9.0 V	-	-	53	ns	
		S _n to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	75	ns	
			V _{CC} = 6.0 V	-	-	64	ns	
			V _{CC} = 9.0 V	-	-	56	ns	
		74HCT4067						

propagation delay	t_{pd}	Yn to Z; see Figure 10 ^{[1][2]}	$V_{CC} = 4.5 \text{ V}$	-	-	19	ns
		Z to Yn; see Figure 10 ^{[1][2]}	$V_{CC} = 4.5 \text{ V}$	-	-	15	ns
turn-off time	t_{off}	$\bar{E}$ to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	69	ns
		Sn to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	69	ns
		$\bar{E}$ to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	75	ns
		Sn to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	75	ns
turn-on time	t_{on}	$\bar{E}$ to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	75	ns
		Sn to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	75	ns
		$\bar{E}$ to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	81	ns
		Sn to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	81	ns

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3] t_{on} is the same as t_{PZH} and t_{PZL} .

[4] t_{off} is the same as t_{PHZ} and t_{PLZ} .

[5] For test circuit see Figure 12.

[6] V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

3.3.6、AC Characteristics 3

($T_{amb} = -40^{\circ}\text{C} \sim +125^{\circ}\text{C}$; $GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
74HC4067							
propagation delay	t_{pd}	Yn to Z; see Figure 10 ^{[1][2]}	V _{CC} = 4.5 V	-	-	22	ns
			V _{CC} = 6.0 V	-	-	19	ns
			V _{CC} = 9.0 V	-	-	14	ns
		Z to Yn; see Figure 10 ^{[1][2]}	V _{CC} = 4.5 V	-	-	18	ns
			V _{CC} = 6.0 V	-	-	15	ns
			V _{CC} = 9.0 V	-	-	12	ns
turn-off time	t_{off}	$\bar{E}$ to Yn; see Figure 10 ^[3]	V _{CC} = 4.5 V	-	-	75	ns
			V _{CC} = 6.0 V	-	-	64	ns
			V _{CC} = 9.0 V	-	-	57	ns
		Sn to Yn; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	75	ns
			V _{CC} = 6.0 V	-	-	64	ns
			V _{CC} = 9.0 V	-	-	57	ns
		$\bar{E}$ to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	83	ns
			V _{CC} = 6.0 V	-	-	71	ns
			V _{CC} = 9.0 V	-	-	63	ns
		Sn to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	87	ns
			V _{CC} = 6.0 V	-	-	74	ns
			V _{CC} = 9.0 V	-	-	68	ns
turn-on time	t_{on}	$\bar{E}$ to Yn; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	83	ns
			V _{CC} = 6.0 V	-	-	71	ns
			V _{CC} = 9.0 V	-	-	63	ns
		Sn to Yn; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	90	ns
			V _{CC} = 6.0 V	-	-	77	ns
			V _{CC} = 9.0 V	-	-	68	ns
		$\bar{E}$ to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	83	ns
			V _{CC} = 6.0 V	-	-	71	ns
			V _{CC} = 9.0 V	-	-	63	ns
		Sn to Z; see Figure 11 ^[3]	V _{CC} = 4.5 V	-	-	90	ns
			V _{CC} = 6.0 V	-	-	77	ns
			V _{CC} = 9.0 V	-	-	68	ns
74HCT4067							

propagation delay	t_{pd}	Yn to Z; see Figure 10 ^{[1][2]}	$V_{CC} = 4.5 \text{ V}$	-	-	22	ns
		Z to Yn; see Figure 10 ^{[1][2]}	$V_{CC} = 4.5 \text{ V}$	-	-	18	ns
turn-off time	t_{off}	$\bar{E}$ to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	83	ns
		Sn to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	83	ns
		$\bar{E}$ to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	90	ns
		Sn to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	90	ns
turn-on time	t_{on}	$\bar{E}$ to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	90	ns
		Sn to Yn; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	90	ns
		$\bar{E}$ to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	98	ns
		Sn to Z; see Figure 11 ^[3]	$V_{CC} = 4.5 \text{ V}$	-	-	98	ns

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

[3] t_{on} is the same as t_{PZH} and t_{PZL} .

[4] t_{off} is the same as t_{PHZ} and t_{PLZ} .

[5] For test circuit see Figure 12.

[6] V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

3.3.7、AC Characteristics 4

($T_{amb}=25^{\circ}\text{C}$; $\text{GND}=0\text{V}$; $C_L=50\text{pF}$; recommended conditions and typical values.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
total harmonic distortion	THD	$f_i = 1\text{ kHz};$ $C_L = 50\text{pF};$ $R_L = 10\text{ k}\Omega;$ see Figure 13	$V_{CC} = 4.5\text{ V};$ $V_{is(p-p)} = 4.0\text{ V}$	-	0.04	-	%
			$V_{CC} = 9.0\text{ V};$ $V_{is(p-p)} = 8.0\text{ V}$	-	0.02	-	%
		$f_i = 10\text{ kHz};$ $C_L = 50\text{pF};$ $R_L = 10\text{ k}\Omega;$ see Figure 13	$V_{CC} = 4.5\text{ V};$ $V_{is(p-p)} = 4.0\text{ V}$	-	0.12	-	%
			$V_{CC} = 9.0\text{ V};$ $V_{is(p-p)} = 8.0\text{ V}$	-	0.06	-	%
isolation (OFF-state)	α_{iso}	$R_L = 600\text{ }\Omega;$ $C_L = 50\text{pF};$ see Figure 14	$V_{CC} = 4.5\text{ V};$ [1]	-	-50	-	dB
			$V_{CC} = 9.0\text{ V};$ [1]	-	-50	-	dB
-3dB frequency response	$f_{(-3dB)}$	$R_L = 50\text{ }\Omega;$ $C_L = 10\text{pF};$ see Figure 15	$V_{CC} = 4.5\text{ V};$ [2]	-	90	-	MHz
			$V_{CC} = 9.0\text{ V};$ [2]	-	100	-	MHz
switch capacitance	C_{sw}	independent pins Y		-	5	-	pF
		common pin Z		-	45	-	pF

Note:

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

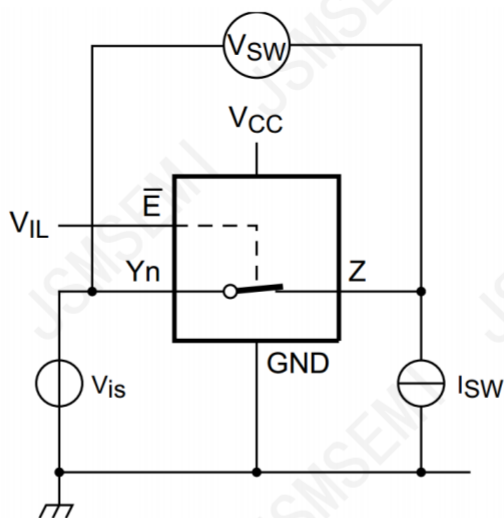
[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for $f_i = 1\text{ MHz}$ (0 dBm = 1 mW into 50 Ω). After set-up, f_i is increased to obtain a reading of -3dB at V_{os} .

[3] V_{is} is the input voltage at a Y_n or Z terminal, whichever is assigned as an input.

[4] V_{os} is the output voltage at a Y_n or Z terminal, whichever is assigned as an output.

4、Testing Circuit

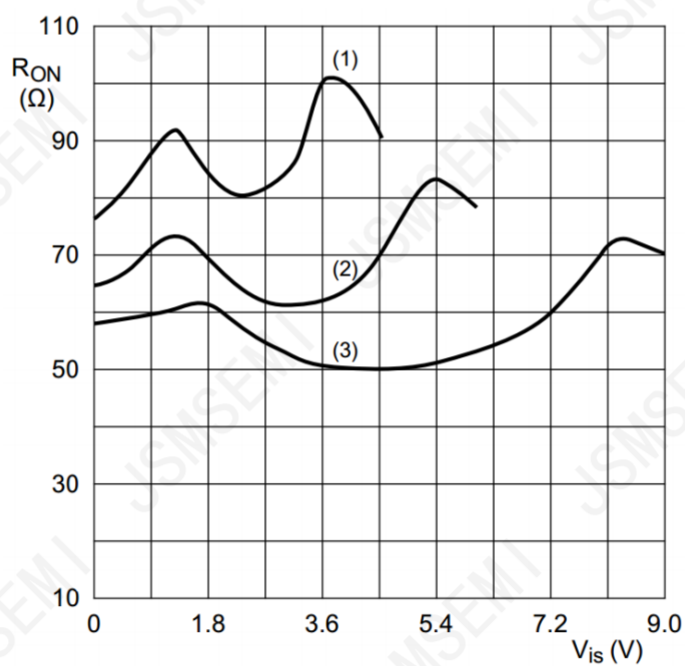
4.1、DC Testing Circuit 1



$$V_{is} = 0V \text{ to } V_{CC}$$

$$R_{ON} = V_{SW}/I_{SW}$$

Figure 6. Test circuit for measuring R_{ON}



$$V_{is} = 0V \text{ to } V_{CC}$$

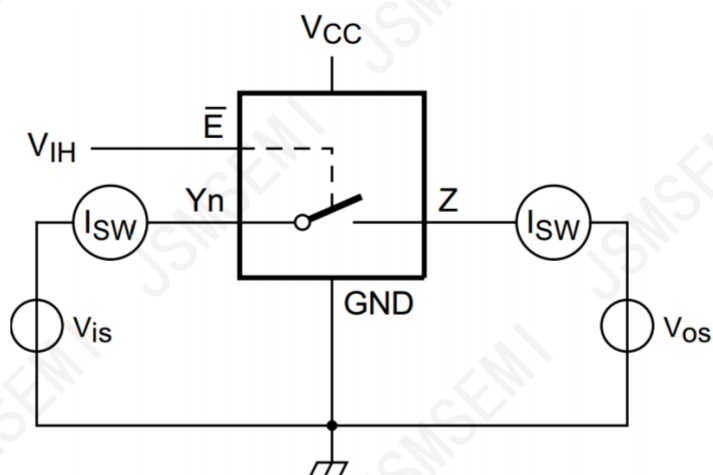
$$(1) V_{CC} = 4.5V$$

$$(2) V_{CC} = 6.0V$$

$$(3) V_{CC} = 9.0V$$

Figure 7. Typical R_{ON} as a function of input voltage V_{is}

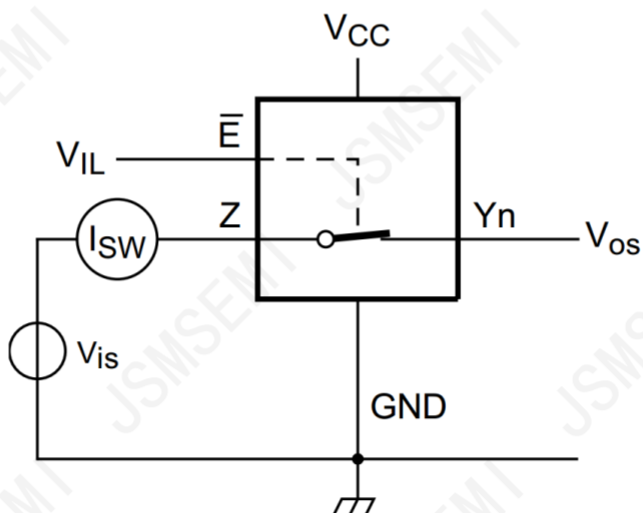
4.2、DC Testing Circuit 2



$V_{is} = V_{CC}$ and $V_{os} = GND$

$V_{is} = GND$ and $V_{os} = V_{CC}$

Figure 8. Test circuit for measuring OFF-state leakage current



$V_{is} = V_{CC}$ and $V_{os} = \text{open}$

$V_{is} = GND$ and $V_{os} = \text{open}$

Figure 9. Test circuit for measuring ON-state leakage current

4.3、AC Testing Waveforms

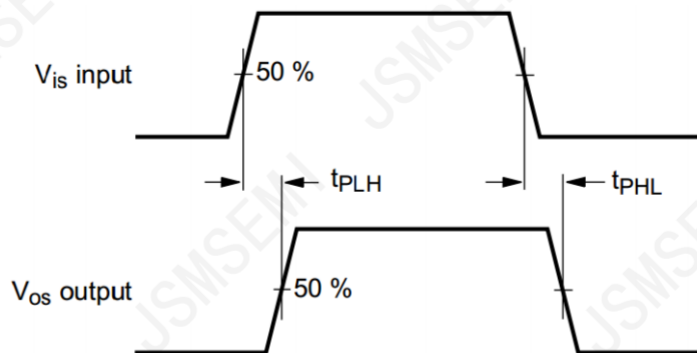


Figure 10. Input (V_{is}) to output (V_{os}) propagation delays

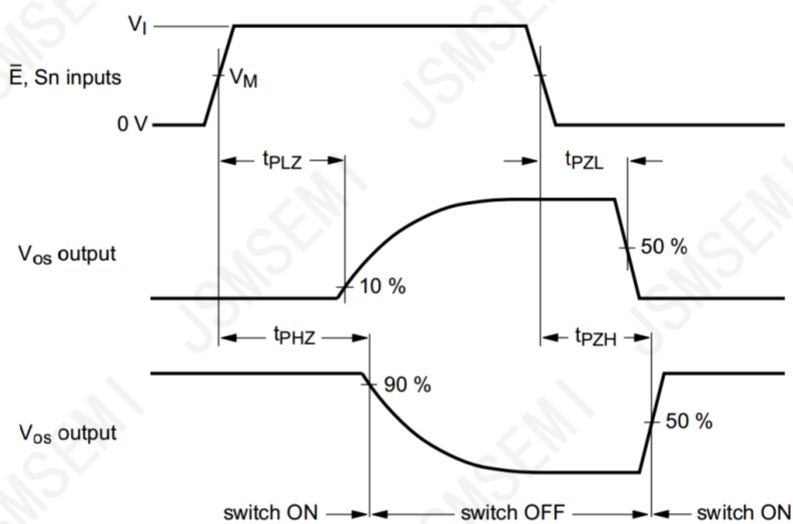


Figure 11. Turn-on and turn-off times

4.4、Measurement Points

Type	V_I	V_M
74HC4067	V_{CC}	$0.5V_{CC}$
74HCT4067	3.0V	1.3V

4.5、AC Testing Circuit 1

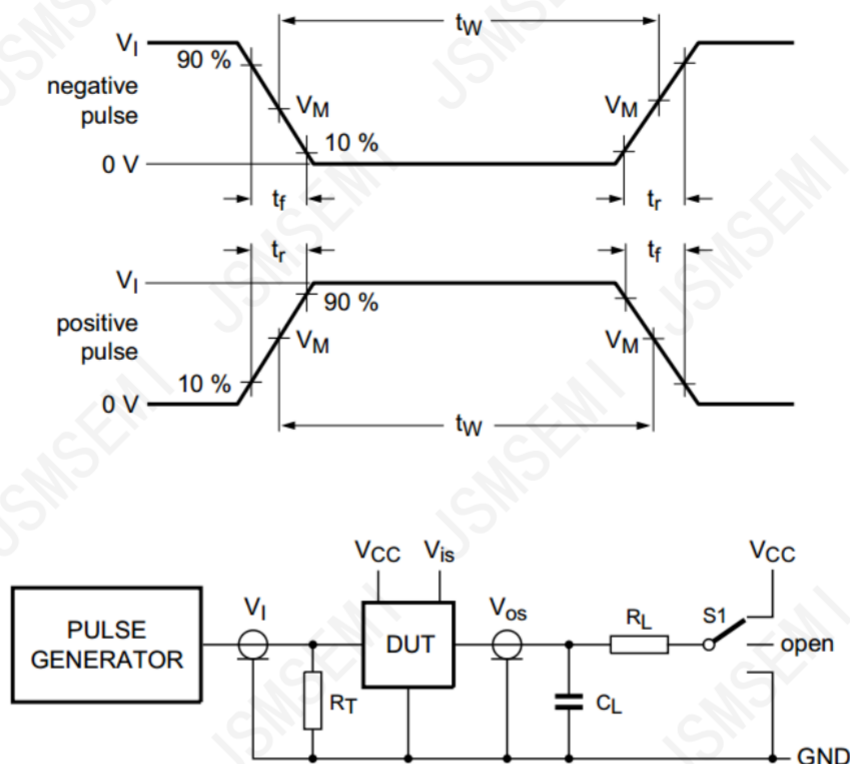


Figure 12. Test circuit for measuring switching times

Definitions for test circuit:

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

S1 = Test selection switch.

4.6、Test Data

Test	Input				Output		S1 position
	Control $\bar{E}$	Address Sn	Switch Yn (Z)	t_r, t_f	Switch Z (Yn)		
	$V_I^{[1]}$	$V_I^{[1]}$	V_{is}		C_L	R_L	
t_{PHL}, t_{PLH}	GND	GND or V_{CC}	GND to V_{CC}	6ns	50pF	-	open
t_{PHZ}, t_{PZH}	GND to V_{CC}	GND to V_{CC}	V_{CC}	6ns	50pF, 15pF	1k Ω	GND
t_{PLZ}, t_{PZL}	GND to V_{CC}	GND to V_{CC}	GND	6ns	50pF, 15pF	1k Ω	V_{CC}

Note:

[1] For 74HCT4067: maximum input voltage $V_I = 3.0$ V.

4.7、AC Testing Circuit 2

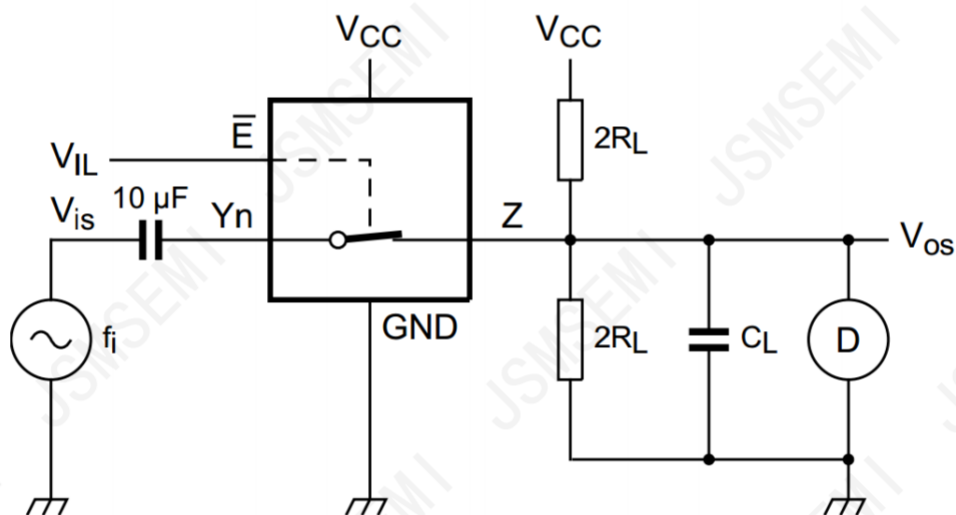
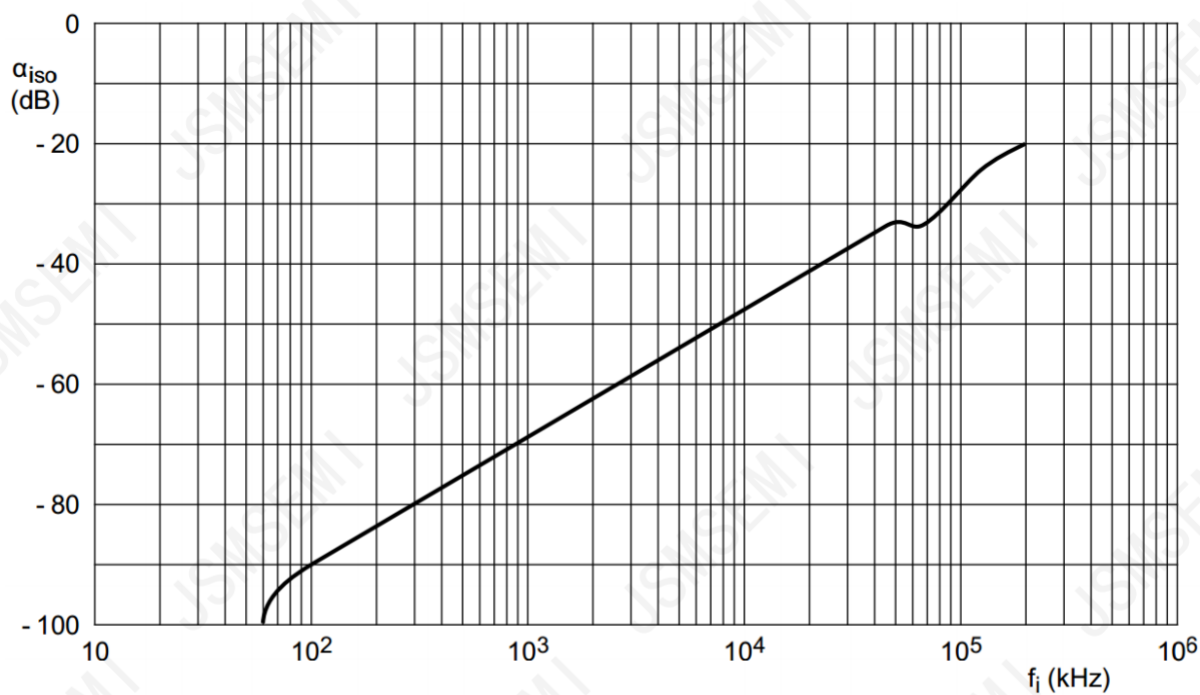
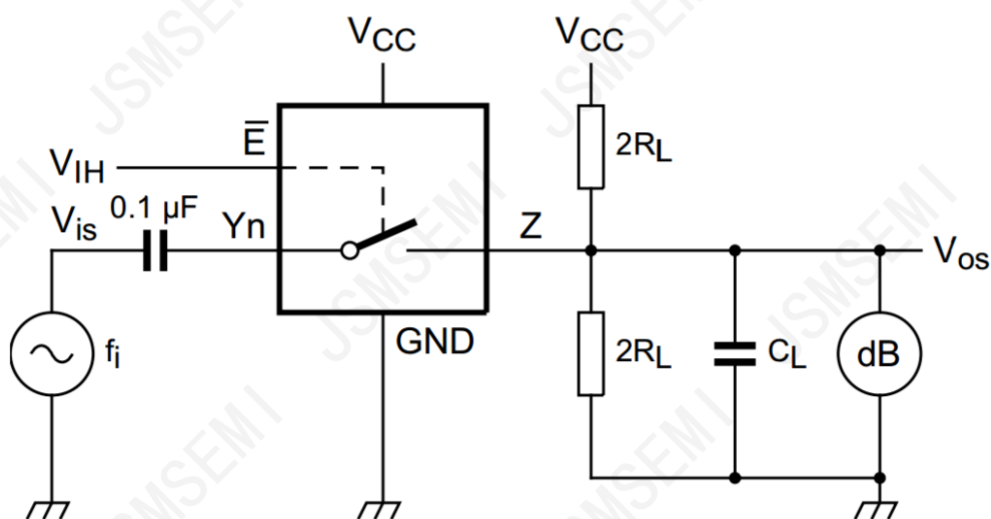


Figure 13. Test circuit for measuring total harmonic distortion



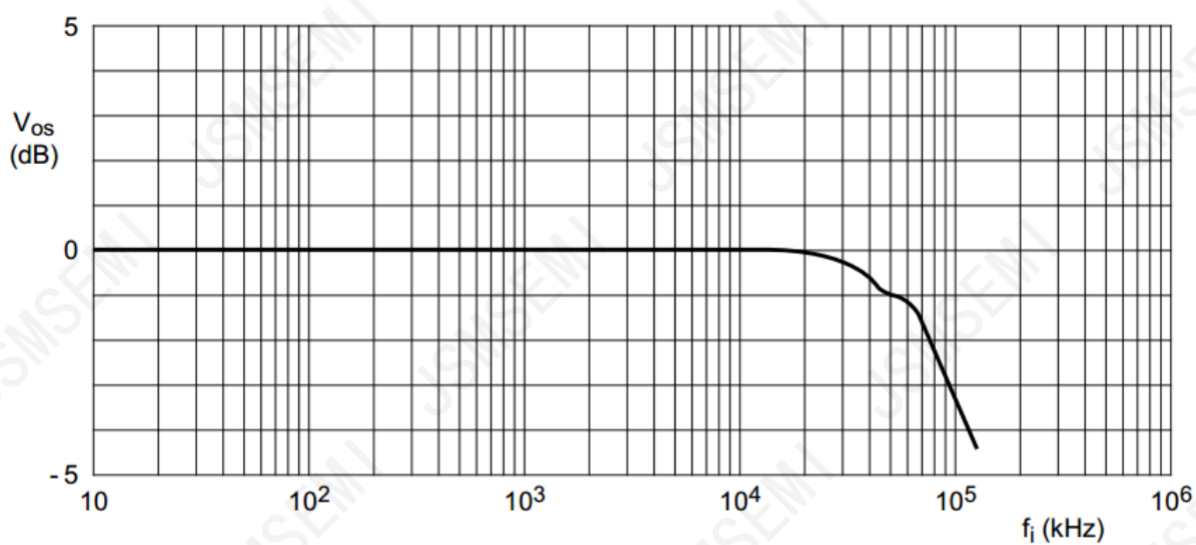
a. Isolation (OFF-state)



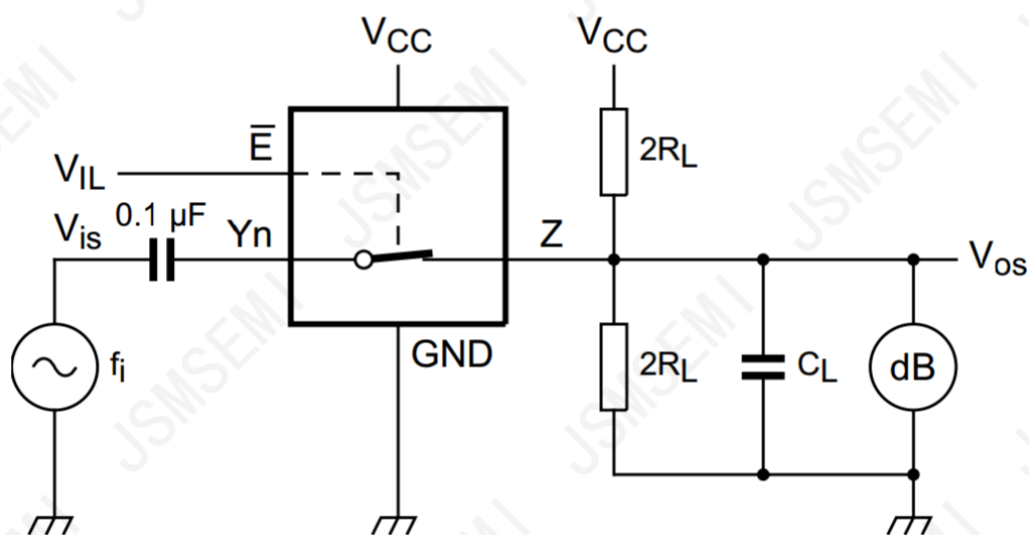
b. Test circuit

$V_{CC} = 4.5 \text{ V}$; $GND = 0 \text{ V}$; $R_L = 600 \Omega$; $R_{source} = 1 \text{ k}\Omega$.

Figure 14. Isolation (OFF-state) as a function of frequency



a. Typical -3 dB frequency response



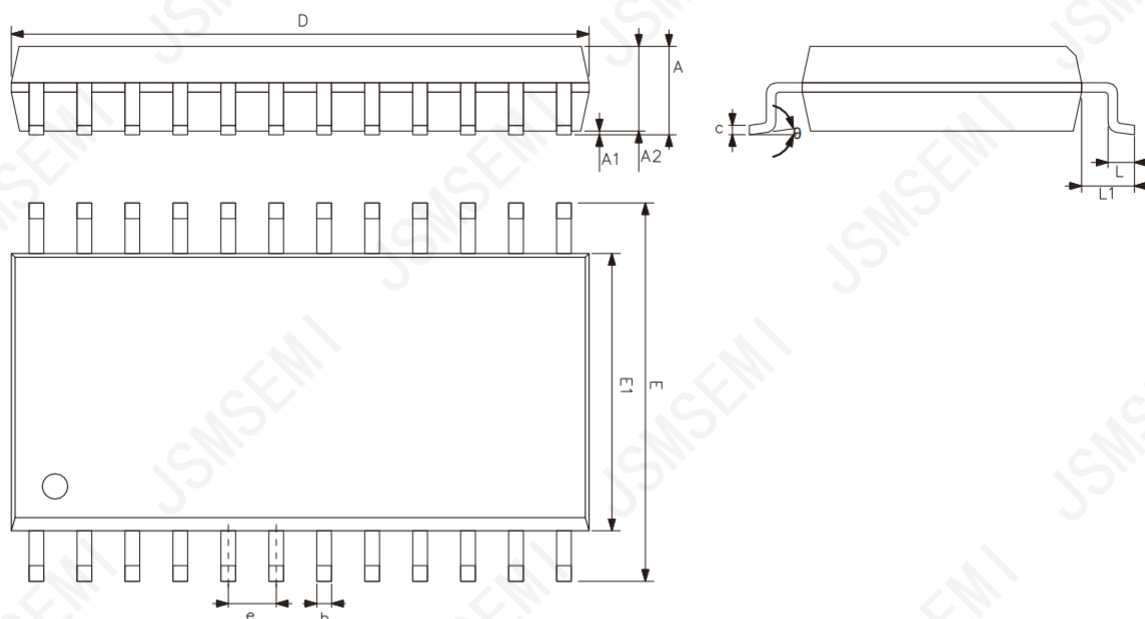
b. Test circuit

$V_{CC} = 4.5 \text{ V}$; $GND = 0 \text{ V}$; $R_L = 50 \Omega$; $R_{source} = 1 \text{ k}\Omega$.

Figure 15. -3 dB frequency response

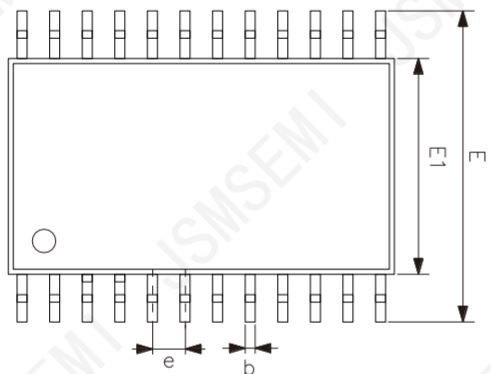
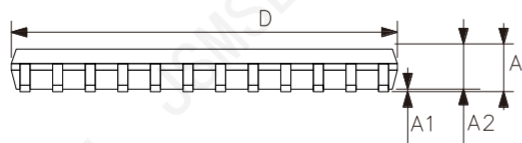
5、Package Information

5.1、SOP24



Symbol	Dimensions (mm)	
	Min.	Max.
A	2.35	2.65
A1	0.10	0.30
A2	2.13	2.44
b	0.39	0.47
c	0.25	0.30
D	15.19	15.55
E	10.10	10.57
E1	7.40	7.62
e	1.27	
L	0.41	1.00
L1	1.30	1.50
θ	0°	8°

5.2、TSSOP24



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.20	6.60
E1	4.30	4.50
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

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