4.1-A Brushed DC Motor Driver with Integrated Current Sense and Regulation

(compatible to DRV8251A (TI USA)

1. Feature

- N-channel H-bridge brushed DC motor driver
- 4.5V to 48V Operating Supply Voltage Range
- High Output Current Capability: 4.1-A Peak
- Low MOSFET $R_{DS(on)}$ Typical 0.50Ω(HS+LS)
- Low Power Sleep Mode
  - <2uA at VM=24V, T_J = 25°C
- PWM Control Interface
- Protection Features:
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Undervoltage Lockout (UVLO)

2. Applications

- POS Printers
- Printers
- Washer and Dryer
- Coffee machine
- Surgical Equipment
- Fitness Machine

3. General Description

The HT8251A device is an integrated motor driver with N-channel H-bridge, charge pump, current regulation, and protection circuitry. The charge pump improves efficiency by supporting N-channel MOSFET half bridges and 100% duty cycle driving.

An internal current mirror architecture on the IPROPI pin implements current sensing and regulation. This eliminates the need for a large power shunt resistor, saving board area and reducing system cost. The IPROPI current-sense output allows a microcontroller to detect motor stall or changes in load conditions.
The external voltage reference pin, VREF, determines the threshold of current regulation during start-up and stall events without interaction from a microcontroller.
A low-power sleep mode achieves ultra-low quiescent current draw by shutting down most of the internal circuitry. Internal protection features include supply undervoltage lockout, output overcurrent, and device overtemperature.

The HT8251A is available in a 8-pin eSOP8

4. Package

Part Number	Package	Body Size
HT8251AREZ	eSOP8	4.9mm x 6.0mm

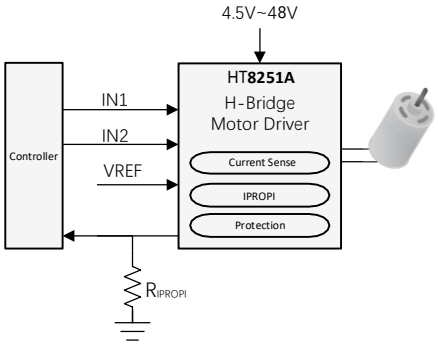
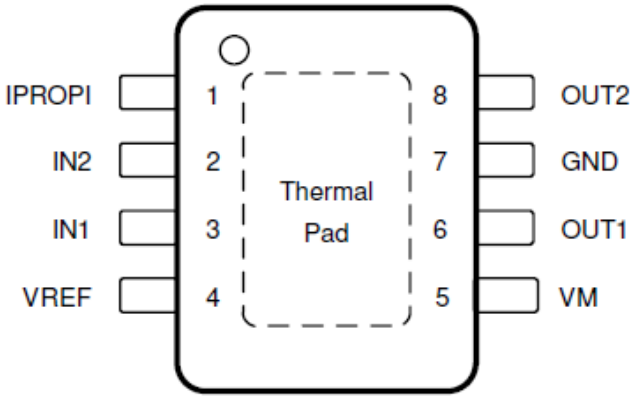


Fig.1 Block diagram of HT8251A

5. PIN Definition



8-Pin HSOP Top View

Fig.2 Pad definition of HT8251A

Table 1 Pad Functions

Pin	Name	I/O	Description
1	IPROPI	PWR	Analog current output proportional to load current
2	IN2	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns
3	IN1	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns
4	VREF	I	Analog input. Apply a voltage between 0 to 5 V. For information on current regulation
5	VM	PWR	4.5-V to 48-V power supply. Connect a 0.1-µF bypass capacitor to ground
6	OUT1	I	H-bridge output. Connect directly to the motor or other inductive load
7	GND	PWR	Device power ground. Connect to system ground.
8	OUT2	I	H-bridge output. Connect directly to the motor or other inductive load

Absolute Maximum Ratings

(If out of these ratings, the filter may be fail or damaged)

Table 2

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.3	50	V
Power supply transient voltage ramp	VM	0	2	V/μs
Logic pin voltage	INx	-0.3	7	V
Reference input pin voltage	VREF	-0.3	6	V
Output pin voltage	OUTx	-0.7	VM + 0.7	V
Current sense input pin voltage	ISEN	-0.5	1	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

6. Recommended Operating Conditions

Table 3

			MIN	TYP	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5		48	V
V_{VREF}	Reference voltage	VREF	0		5	V
V_{IN}	Logic input voltage	INx	0		5.5	V
f_{PWM}	PWM frequency	INx	0			200 kHz
I_{OUT}	Peak output current 4.5V≤V_{VM}<5.5V	OUTx			3.7	A
	Peak output current 5.5V≤V_{VM}				4.1	
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

7. Electrical Characteristics

Table 4

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
I_{VMQ}	VM sleep mode current	V_{VM} = 24 V, IN1 = IN2 = 0, T_J = 25°C			2	μA
I_{VM}	VM active mode current	V_{VM} = 24 V, IN1 = IN2 = 1		3	4	mA
t_{WAKE}	Turn on time	Control signal to active mode			250	μs
t_{SLEEP}	Turn off time	Control signal to sleep mode	0.8		1.5	ms
LOGIC-LEVEL INPUTS (INx)						
V_{IL}	Input logic low voltage				0.7	V
V_{IH}	Input logic high voltage		1.5			V
V_{HYS}	Input hysteresis			200		mV
I_{IL}	Input logic low current	V_{IN} = 0 V	-1		1	μA
I_{IH}	Input logic high current	V_{IN} = 3.3 V		33	100	μA
R_{PD}	Input pulldown resistance	To GND		100		kΩ
DRIVER OUTPUTS (OUTx)						
$R_{DS(on)\_HS}$	High-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		250		mΩ
$R_{DS(on)\_LS}$	Low-side MOSFET on resistance	V_{VM} = 24 V, I = 1 A, f_{PWM} = 25 kHz		250		mΩ
V_{SD}	Body diode forward voltage	I_{OUT} = 1 A		0.8		V
t_{RISE}	Output rise time	V_{VM} = 24 V, OUTx rising from 10% to 90%		220		ns
t_{FALL}	Output fall time	V_{VM} = 24 V, OUTx falling from 90% to 10%		220		ns
t_{PD}	Input to output propagation delay	INx to OUTx		0.7	1	μs
t_{DEAD}	Output dead time			200		ns
INTEGRATED CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A_{IPROPI}	Current mirror scaling factor			1500		uA/A
A_{ERR}	Current mirror total error	I_{OUT} = 1.5 A, V_{VM} ≥ 6.5 V, V_{IPROPI} ≤ 3.0 V	-5		5	%
t_{OFF}	Current regulation off time			25		μs
t_{BLANK}	Current regulation blanking time			2		μs
t_{DEG}	Current regulation deglitch time			0.7		μs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising	4.15	4.3	4.45	V
		Supply falling	4.05	4.2	4.35	V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		100		mV
t_{UVLO}	Supply undervoltage deglitch time			10		us
I_{OCP}	Overcurrent protection trip point	4.5V≤V_{VM}<5.5V	3.7			A
		5.5V≤V_{VM}	4.1			
t_{OCP}	Overcurrent protection deglitch time			2		μs
t_{RETRY}	Overcurrent protection retry time			3		ms
T_{TSD}	Thermal shutdown temperature			165		℃

8. Detailed Description

8.1 Overview

The HT8251A is an 8-pin device for driving brushed DC motors from a 4.5-V to 48-V supply rail. Two logic inputs control the H-bridge driver, which consists of four N-channel MOSFETs that have a typical RDS(on) of 500 mΩ (including one high-side and one low-side FET). A single power input, VM, serves as both device power and
the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation at frequencies between 0 to 200 kHz. The device enters a low-power sleep mode by bringing both inputs low.
The HT8251A also integrates current sense feedback to a microcontroller using current mirrors on the low-side power MOSFETs. The IPROPI pin sources a small current that is proportional to the current in the MOSFETs. This current can be converted to a proportional voltage using an external resistor (RIPROPI). This integrated current sensing scheme out-performs traditional external shunt resistor sensing by providing current information even during the off-time slow decay recirculating period and removing the need for an external power shunt resistor. The integrated current regulation feature allows the device to limit the output current with a fixed off-time PWM chopping scheme. The VREF pin configures the current regulation level during motor operation to limit the load current.
A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

8.2 Functional Block Diagram

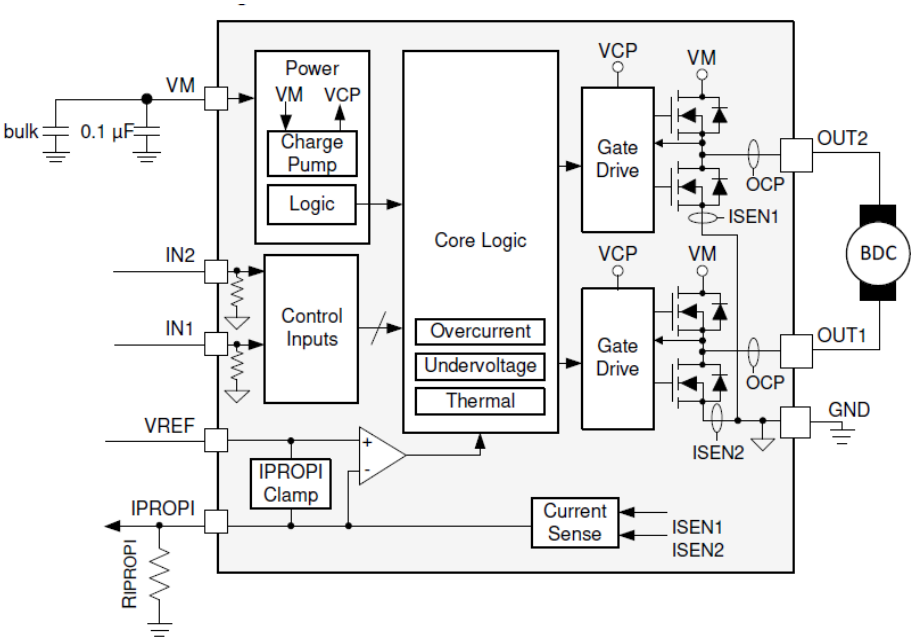


Figure 3. Function Block Diagram

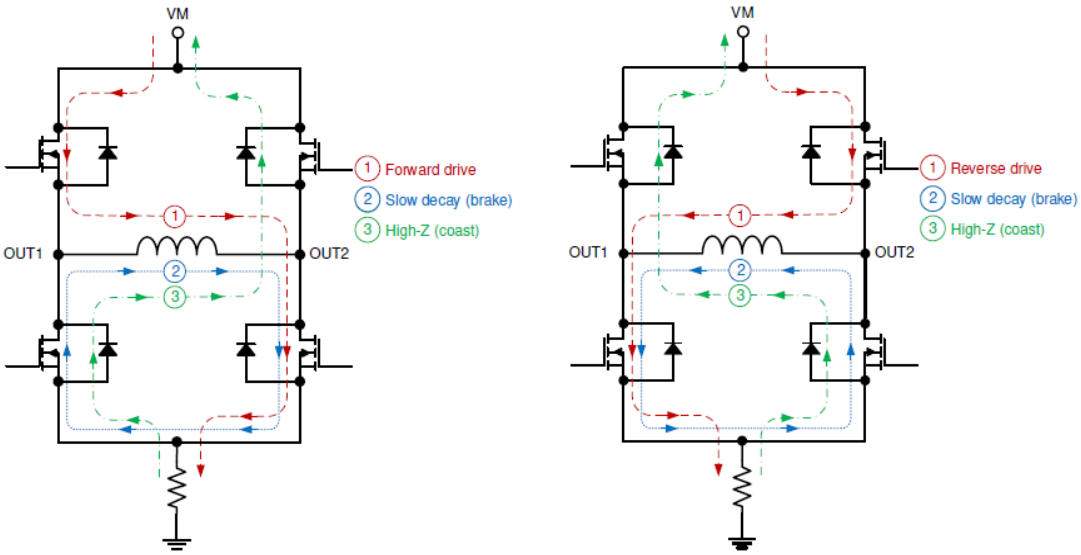
8.3 Bridge Control

The HT8251A output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in table 5.

Table 5 H-Bridge Logic

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)
0	1	L	H	Reverse (Current OUT2 → OUT1)
1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	L	L	Brake; low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 0 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. Figure 4 shows how the motor current flows through the H-bridge. The input pins can be powered before VM is applied.



FORWARD REVERSE

Figure 4. H-Bridge Current Paths

8.4 Current Sense and Regulation (IPROPI)

The HT8251A device integrates current sensing, regulation, and feedback as part of the IPROPI feature. These features allow the device to sense the output current without an external sense resistor or sense circuitry reducing system size, cost, and complexity. This also allows for the device to limit the output current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current through a current proportional output. The figure5 shows the IPROPI timings specified in the Electrical Characteristics table.

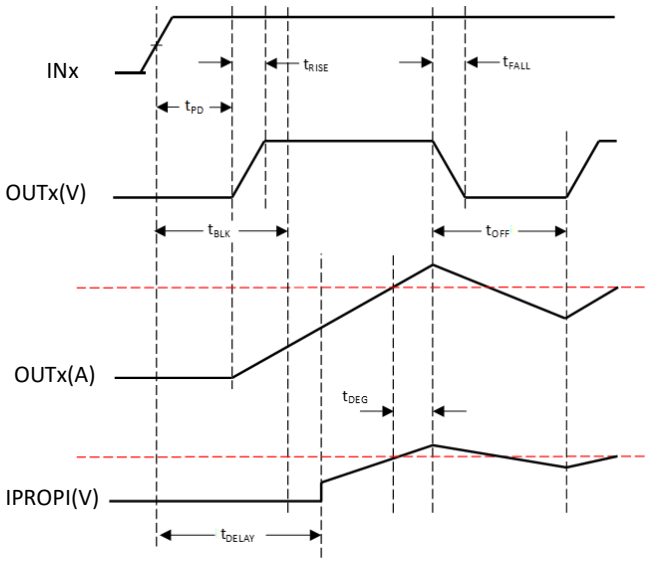


Figure 5. Detailed IPROPI Timing Diagram

8.5 Current Sensing

The IPROPI pin outputs an analog current proportional to the current flowing through the low-side power MOSFETs in the H-bridge scaled by AIPROPI. The IPROPI output current can be calculated by equation1 . The I_{LSx} in equation1 is only valid when the current flows from drain to source in the low-side MOSFET. If current flows from source to drain or through the body diode, the value of I_{LSx} for that channel is zero. For instance, if the bridge is in the brake, slow-decay state, then the current out of I_{PROPI} is only proportional to the current in one of the low-side MOSFETs.

$$I_{PROPI}\ (\mu A) = (I_{LS1} + I_{LS2})\ (A) \times A_{IPROPI}\ (\mu A/A) \qquad (1)$$

The A_{ERR} parameter in the Electrical Characteristics table is the error associated with the A_{IPROPI} gain. It indicates the combined effect of offset error added to the IOUT current and gain error.The motor current is measured by an internal current mirror architecture on the low-side FETs which removes the need for an external power sense resistor as shown in Figure 6. The current mirror architecture allows for the motor winding current to be sensed in both the drive and brake low-side slow-decay periods allowing for continuous current monitoring in typical bidirectional brushed DC motor applications. In coast mode, the current is freewheeling and cannot be sensed because it flows from source to drain. However, the current can be sampled by briefly re-enabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again.

After t_{OFF} elapses, the output is re-enabled according to the two inputs, I_{Nx}. The drive time (t_{DRIVE}) until reaching another ITRIP event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

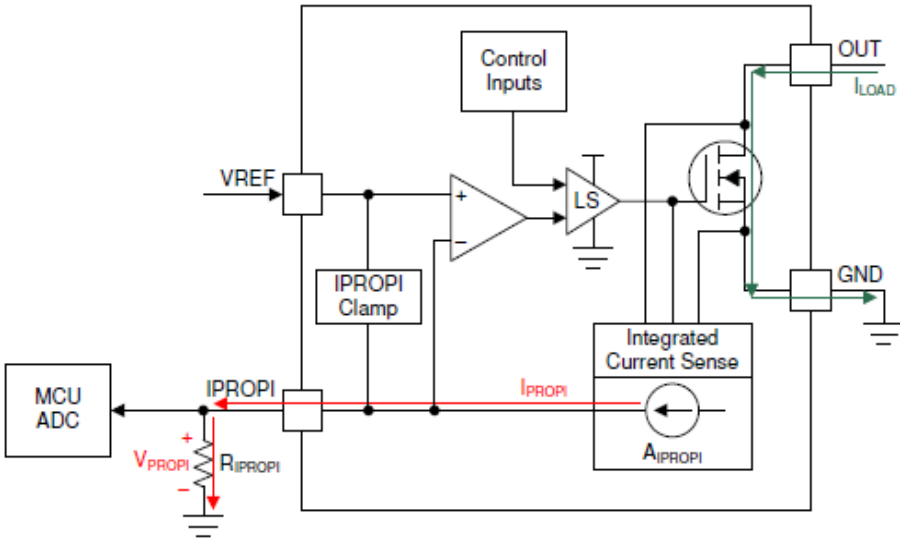


Figure 6. Integrated Current Sensing

The I_{PROPI} pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin with the I_{IPROPI} analog current output. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. Additionally, the HT8251A device implements an internal I_{PROPI} voltage clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events.

The corresponding IPROPI voltage to the output current can be calculated by equation 2.

$$V_{IPROPI}\ (V) = I_{PROPI}\ (A) \times R_{IPROPI}\ (\Omega) \qquad (2)$$

The IPROPI output bandwidth is limited by the sense delay time (t_{DELAY}) of the internal current sensing circuit. This time is the delay from the low-side MOSFET enable command (from the INx pins) to the IPROPI output being ready. If the device is alternating between drive and slow-decay (brake) in an H-bridge PWM pattern, then the low-side MOSFET sensing the current is continuously on and the sense delay time has no impact to the IPROPI output. If a command on the INx pins disables the low-side MOSFETs, the IPROPI output will disable with the input logic signal. Although the low-side MOSFETs may still conduct current as they disable according to the device slew rate (noted in the Electrical Characteristics table by t_{RISE} time), IPROPI will not represent the current in the low-side MOSFETs during this turnoff time.

8.6 Current Regulation

The HT8251A device integrates current regulation using a fixed off-time current chopping scheme. This allows the devices to limit the output current in case of motor stall, high torque, or other high current load events without involvement from the external controller as shown in Figure 7.

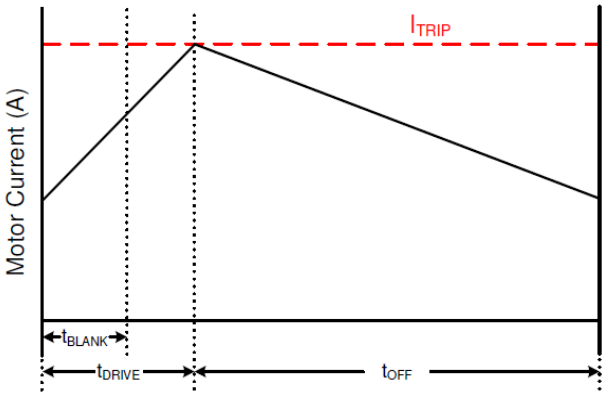


Figure 7. Current-Regulation Time Periods

The current chopping threshold (I_{TRIP}) is set through a combination of the VREF voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

ITRIP (A) x AIPROPI (μA/A) = VVREF (V) / RIPROPI (Ω) (3)

For example, if V_{VREF} = 3.3V, R_{IPROPI} = 1310Ω, and A_{IPROPI} = 1575 μA/A, then I_{TRIP} will be approximately 1.6 A.

The fixed off-time current chopping scheme supports up to 100% duty cycle current regulation since the H-bridge automatically enables after the t_{OFF} period and does not require a new control input edge on the INx pins to reset the outputs. When the motor current exceeds the ITRIP threshold, the outputs will enter a current chopping mode with a fixed off time (t_{OFF}). During t_{OFF}, the H-bridge enters a brake/low-side slow decay state (both low- side MOSFETs ON) for t_{OFF} duration after I_{OUT} exceeds I_{TRIP}. After t_{OFF}, the outputs re-enable according to the control inputs if I_{OUT} is less than I_{TRIP}. If I_{OUT} is still greater than I_{TRIP}, the H-bridge enters another period of brake/low-side slow decay for t_{OFF}. If the state of the INx control pins changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs will again follow the inputs.

The I_{TRIP} comparator has both a blanking time (t_{BLK}) and a deglitch time (t_{DEG}). The internal blanking time helps to prevent voltage and current transients during output switching from effecting the current regulation. These transients may be caused by a capacitor inside the motor or on the connections to the motor terminals. The internal deglitch time ensures that transient conditions do not prematurely trigger the current regulation. In certain cases, where the transient conditions are longer than the deglitch time, placing a 10-nF capacitor on the IPROPI pin, close to the device, will help filter the transients on IPROPI output so current regulation does not prematurely trigger. The capacitor value can be adjusted as needed, however large capacitor values may slow down the response time of the current regulation circuitry.

8.7 Protection Circuits

The HT8251 device is fully protected against VM undervoltage, overcurrent, and overtemperature events.

8.7.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive internally. If this analog current limit persists for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge will disable. The driver re-enables after the OCP retry period (t_{RETRY}) has passed. If the fault condition is still present, the cycle repeats.

8.7.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

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8.7.4 VM Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, VUVLO, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset.

8.8 Device Functional Modes

Table 6 summarizes the HT8251A functional modes described in this section.

Table 6 Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	IN1 or IN2 = logic high	Operating	Operating
Low-Power Sleep Mode	IN1 = IN2 = logic low	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See Table 7

8.8.1 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the INx pins are in a state other than IN1 = 0 & IN2 = 0, and t_{WAKE} has elapsed, the device enters active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

8.8.2 Low-Power Sleep Mode

When the IN1 and IN2 pins are both low for time t_{SLEEP}, the HT8251A device enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin (IVMQ). If the device is powered up while all inputs are low, it immediately enters sleep mode. After any of the input pins are set high for longer than the duration of t_{WAKE}, the device becomes fully operational. Figure 8 shows an example timing diagram for entering and leaving sleep mode.

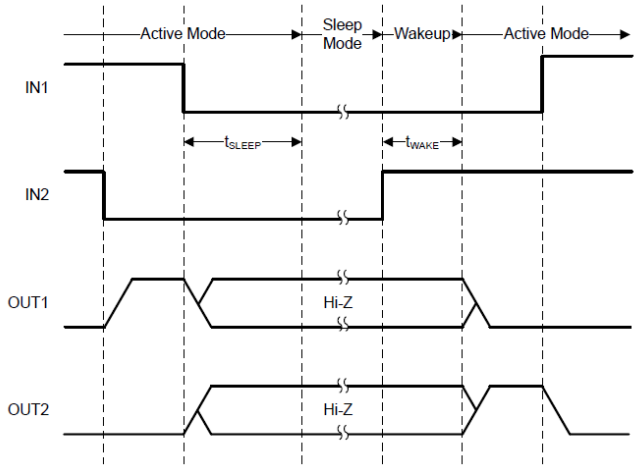


Figure 8. Sleep Mode Entry and Wakeup Timing Diagram

8.8.3 Fault Mode

The HT8251A device enters a fault mode when a fault is encountered. This is utilized to protect the device and the output load. The device behavior in the fault mode is described in and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

Table 7 Fault Conditions Summary

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	$V_M < V_{UVLO,falling}$	Disabled	Disabled	$V_M > V_{UVLO,rising}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	Disabled	Operating	$I_{OUT} < I_{OCP}$
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	Disabled	Operating	$T_J < T_{TSD} - T_{HYS}$

8.9 Typical Application

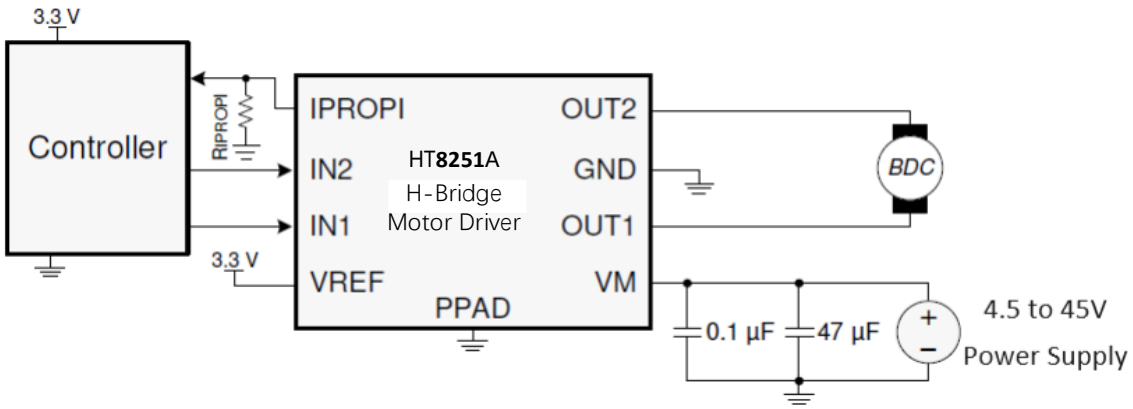
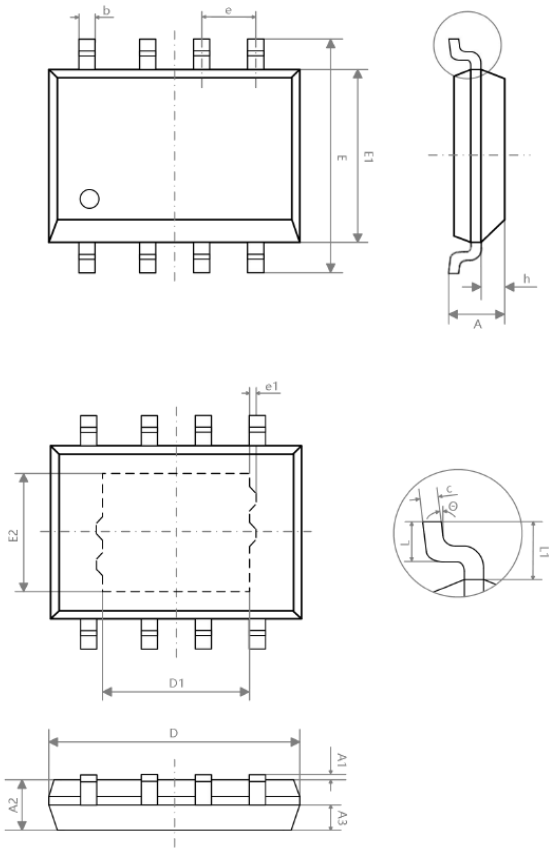


Figure 9. Typical Application Schematic

9. Package（eSOP 4.9*6.0-8）



符号	毫米(mm)		
	最小	典型	最大
A	——	——	1.65
A1	0.05	——	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	——	0.47
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
h	0.25	——	0.50
L	0.50	0.60	0.80
L1	1.05(REF)		
θ	0	——	8°
e1	0.10(REF)		
D1	3.10(REF)		
E2	2.21(REF)		

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