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SEMICONDUCTOR

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AOZ6682CI-MS

Product specification

GENERAL DESCRIPTION

The AOZ6682CI-MS is a fully integrated, high–efficiency 2.0A synchronous rectified step-down converter. The AOZ6682CI-MS operates at high efficiency over a wide output current load range.

This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

The AOZ6682CI-MS requires a minimum number of readily available standard external components and is available in a 6-pin SOT23-6 ROHS compliant package.

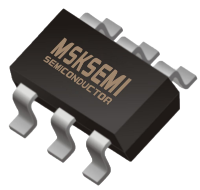
FEATURES

- High Efficiency: Up to 95%@5V
- 600kHz Frequency Operation
- 2.0A Output Current
- No Schottky Diode Required
- 3.5V to 18V Input Voltage Range
- 0.8V Reference
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Integrated internal compensation Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup-Mode
- Input overvoltage protection (OVP)
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Available in SOT23-6 Package

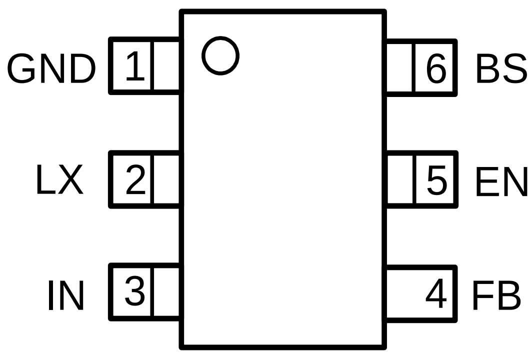
APPLICATIONS

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Notebook computer
- Wireless and DSL Modems

Reference News

Type No	SOT-23-6	MARKING
AOZ6682CI-MS		S42B***

Pin Assignments



PIN FUNCTIONS

Pin	Name	Function
1	GND	Ground Pin
2	LX	Switching Pin
3	IN	Power supply Pin
4	FB	Output Voltage feedback input. Connect FB to the center point of the external resistor divider.
5	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode. Don’t floating this pin.
6	BS	Bootstrap. A capacitor connected between LX and BST pins is required to form a floating supply across the high-side switch driver.

TYPICAL APPILCATION

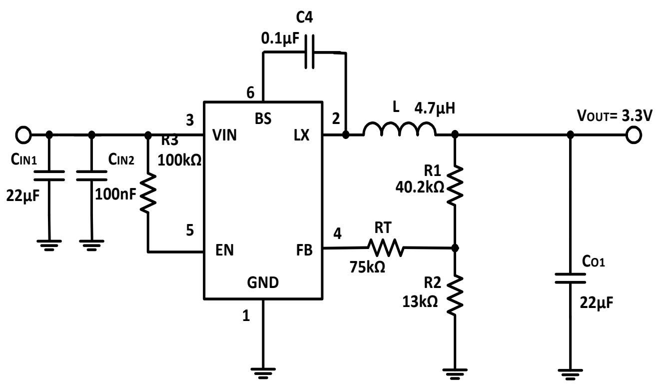
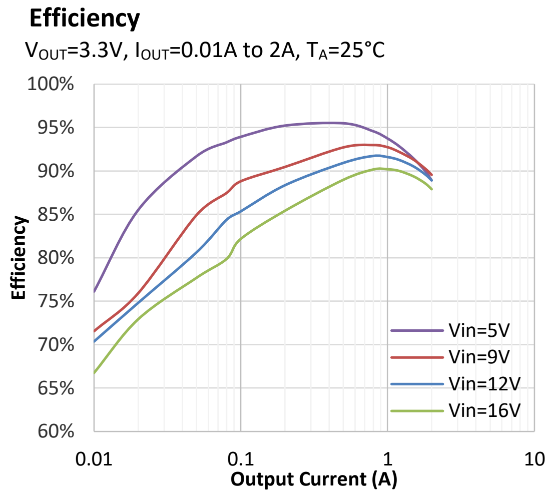


Figure 1. Basic Application Circuit



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Min	Max	Unit
Input Supply Voltage, EN	-0.3	20	V
LX Voltages	-0.3	20	V
FB Voltage	-0.3	6	V
BS Voltage	-0.6	25	V
Storage Temperature Range	-65	150	°C
Junction Temperature (Note 2)		160	°C
Power Dissipation		1000	mW
Lead Temperature (Soldering,10s)		260	°C

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human Body Model for all pins	±2000	V

JEDEC specification JS-001

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
Voltage Range	IN Voltage	3.5	18	V
T_J	Operating Junction Temperature	-40	125	°C

THERMAL RESISITANCE (Note 3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	130	°C/W

ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, V_{OUT}=5V, T_A = 25°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		3.5		18	V
OVP Threshold			19		V
UVLO Threshold		3.0			V
Supply Current in Operation	V_{EN}=2.0V, No Load		400	600	μA
Supply Current in Shutdown	V_{EN} =0		2		μA
Regulated Feedback Voltage	T_A = 25°C,3.5V≤ V_{IN} ≤18V	0.784	0.8	0.816	V
High-Side Switch On-Resistance			120		mΩ
Low-Side Switch On-Resistance			70		mΩ
High-Side Switch Leakage Current	V_{EN}=0V, V_{LX}=0V		0	10	μA
Upper Switch Current Limit	Minimum Duty Cycle		3.0		A
Oscillation Frequency	V_{FB}=0.8V		600		kHz
Maximum Duty Cycle	V_{FB}=0.8V		95		%
EN High-Level Input Voltage		1.50			V
EN Low-Level Input Voltage				0.30	V
Soft Start time			800		μs
Minimum On-Time			100		ns
Thermal Shutdown Threshold (Note 4)			160		°C
Thermal Shutdown Hysteresis (Note 4)			30		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\,(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.

Note 3: Measured on JESD51-7, 4-layer PCB.

Note 4: Thermal shutdown threshold and hysteresis are guaranteed by design.

OPERATION

Internal Regulator

The AOZ6682CI-MS is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high volta ge power MOSFET, and operates at a high 600kHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (V_{FB}) and outputs a current pr oportional to the difference between the two. This output current is then used to charge or discharge the inter nal compensation network to form the COMP voltage, which is used to control the power MOSFET current . The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. W hen the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.8V. Whe n it is lower than the internal reference (V_{REF}), SS overrides REF so the error amplifier uses SS as the referen ce. When SS is higher than REF, REF regains control. The SS time is internally fixed to 800µs.

Over-Current-Protection and Hiccup

The AOZ6682CI-MS has cycle-by-cycle over current limit when the inductor current peak value exceeds th e set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 55% below the reference. Once a UV is triggered, the AOZ6682CI-MS enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-sh ort toground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The AOZ6682CI-MS exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts fir st, generating stable reference voltage and currents, and then the internal regulator is enabled. The regul ator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault trigg ering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject t o this shutdown command.

FUNCTIONAL BLOCK DIAGRAM

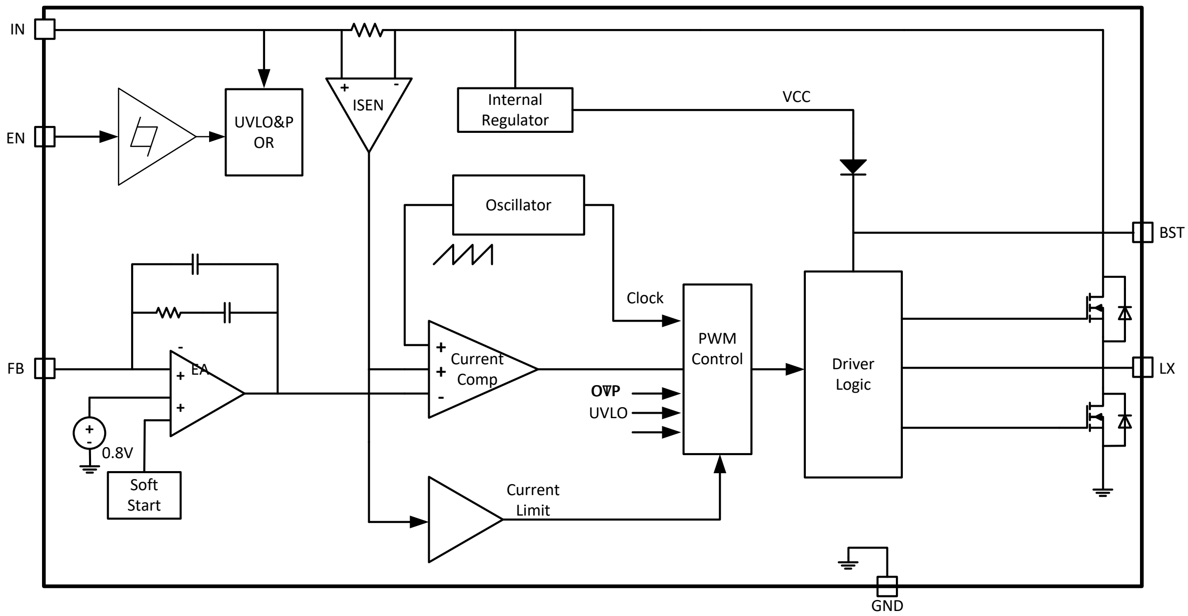


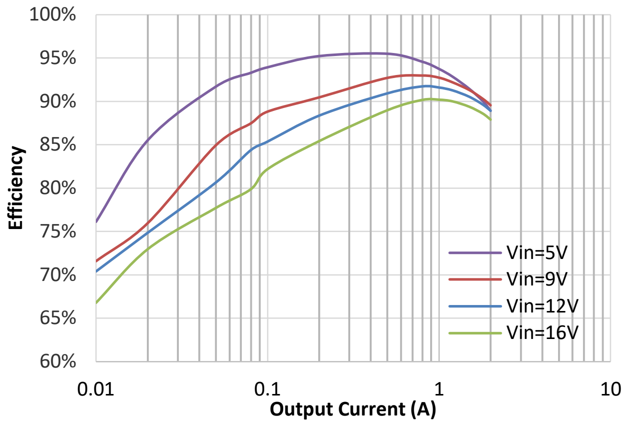
Figure 2. AOZ6682CI-MS **Block Diagram**

TYPICAL PERFORMANCE CHARACTERISTICS

Test condition: V_{IN}=12V, V_{OUT}=3.3V, L=4.7µH, T_A=+25°C, unless other noted.

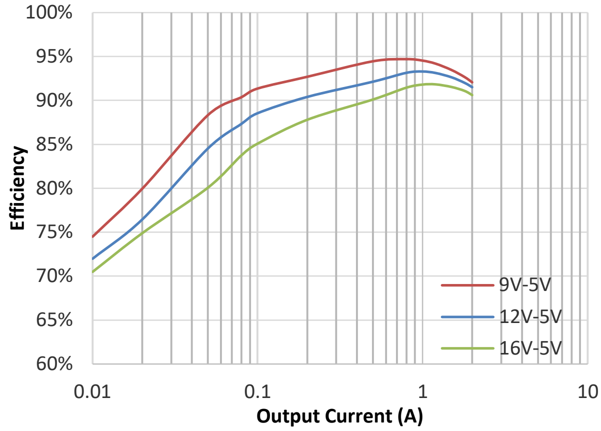
Efficiency at V_{OUT} = 3.3V

V_{OUT} =3.3V, L=4.7µH, DCR=30mΩ



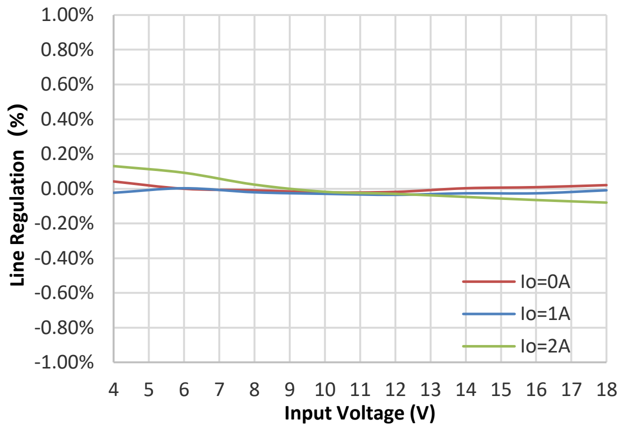
Efficiency at V_{OUT} = 5V

V_{OUT} =5V, L=4.7µH, DCR=30mΩ



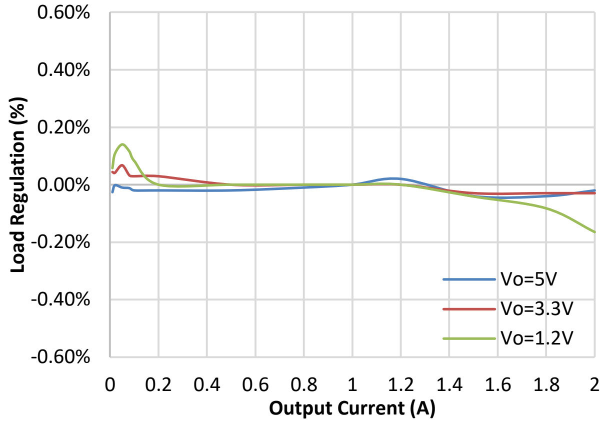
Line Regulation at V_{OUT}=3.3V

V_{OUT}=3.3V, T_A=25°C



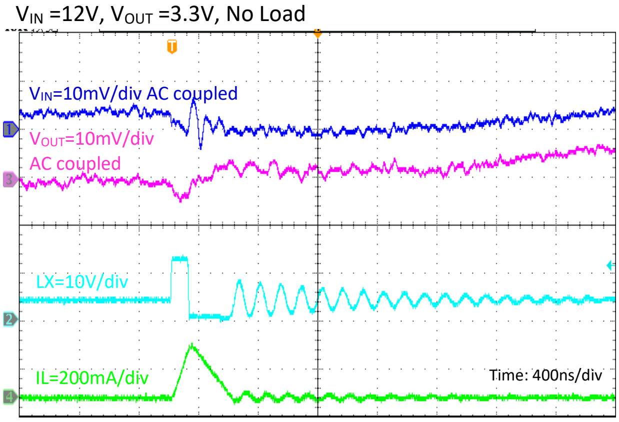
Load Regulation at V_{IN} = 12V

V_{IN}=12V, T_A=25°C



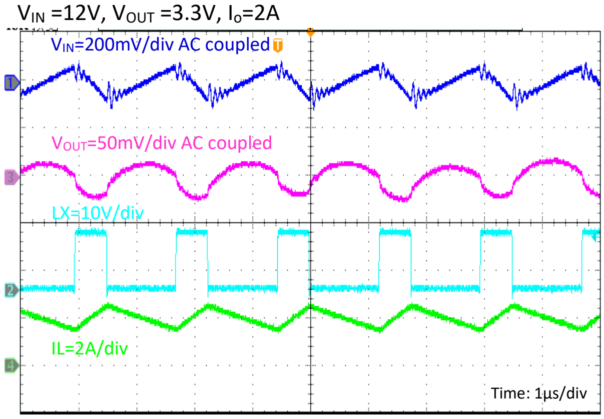
Steady State Operation

V_{IN} =12V, V_{OUT} =3.3V, No Load



Steady State Operation

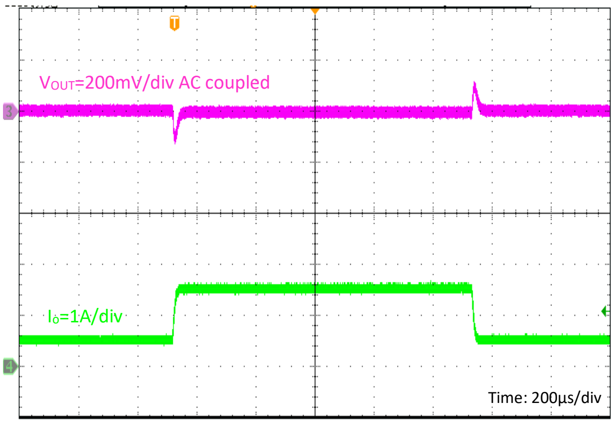
V_{IN} =12V, V_{OUT} =3.3V, I_o=2A



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

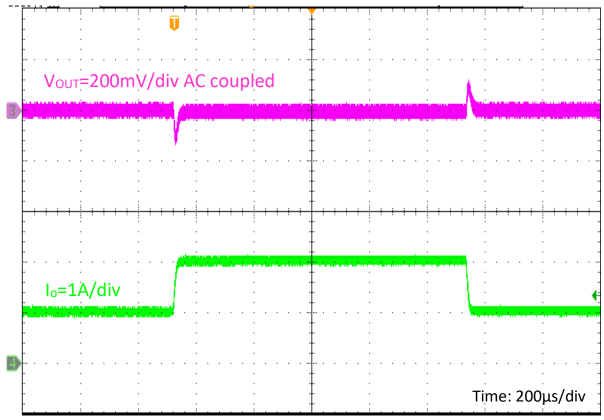
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =0.5A to 1.5A



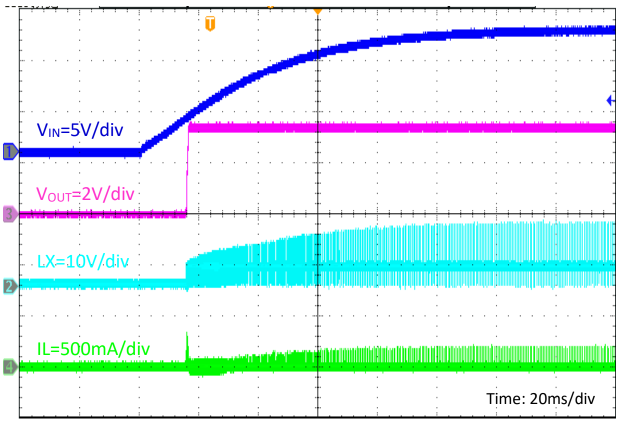
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =1.0A to 2A



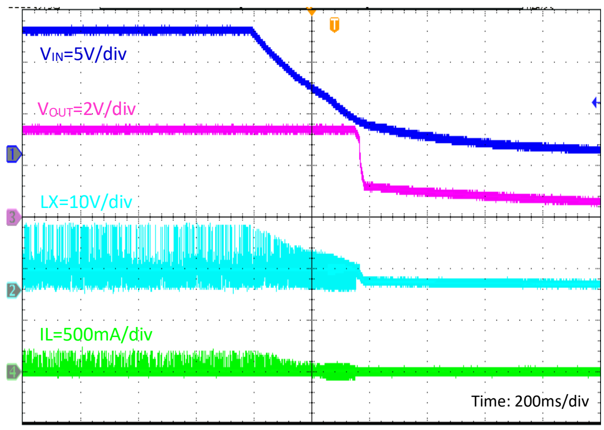
Input Power On

V_{IN} =12V, V_{OUT} =3.3V, No Load



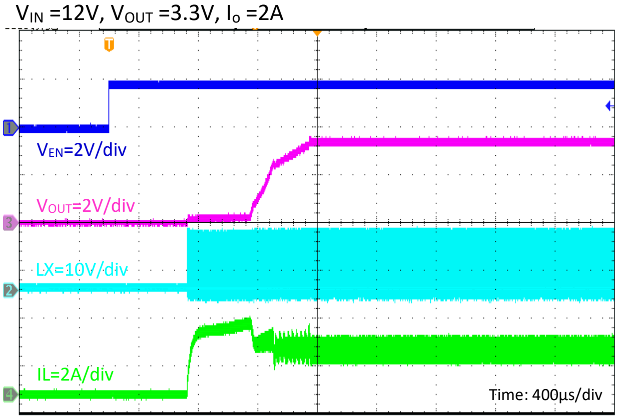
Input Power Down

V_{IN} =12V, V_{OUT} =3.3V, No Load



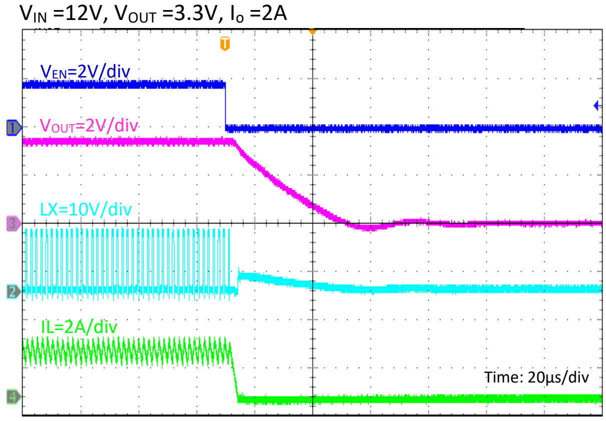
EN Enable Power On

V_{IN} =12V, V_{OUT} =3.3V, I_o =2A



EN Disable Power down

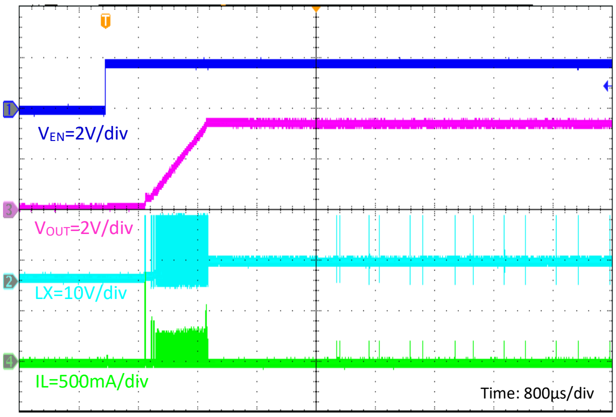
V_{IN} =12V, V_{OUT} =3.3V, I_o =2A



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

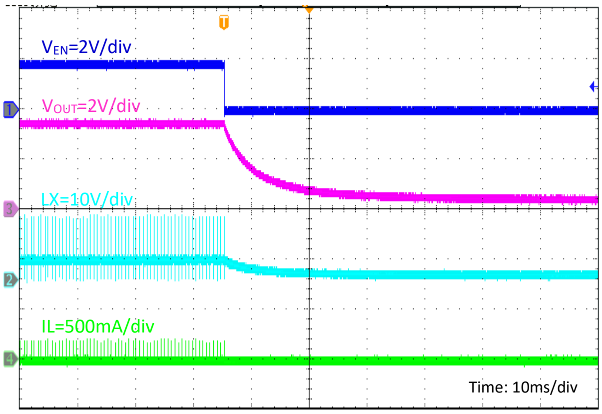
EN Enable Power On

V_{IN} =12V, V_{OUT} =3.3V, No Load



EN Disable Power down

V_{IN}=12V, V_{OUT} =3.3V, No Load

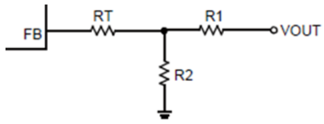


APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 10kΩ for optimal transient response. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$



Use a T-type network for when VOUT is low.

Vout	R1(kΩ)	R2(kΩ)	RT(kΩ)
5V	40.2	7.26	75
3.3V	40.2	12.13	75
2.5V	40.2	17.73	100
1.8V	40.2	29.71	120
1.2V	20.5	36.05	249
1.05V	10	26.84	300

Inductor Selection

A DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. Inductance value is related to inductor ripple current value, input voltage, output voltage setting and switching frequency. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor ripple current. Large value inductors result in lower ripple current and small value inductors result in high ripple current, so inductor value has effect on output voltage ripple value. DC resistance of inductor which has impact on efficiency of DC/DC converter should be taken into account when selecting the inductor. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Output Capacitor Selection

The output capacitor (Co1) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S{}^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The AOZ6682CI-MS can be optimized for a wide range of capacitance and ESR values.

Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.

2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.

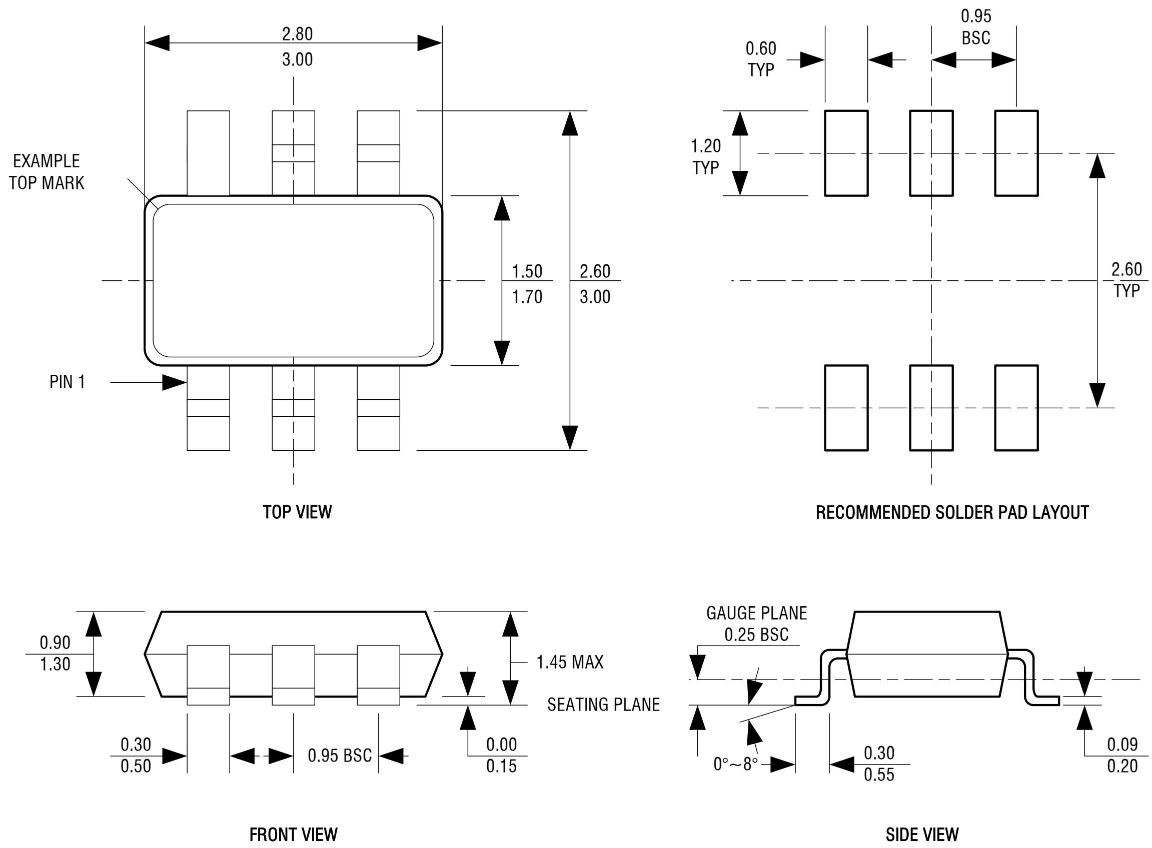
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) VOUT, LX away from sensitive analog areas such as FB.

5) Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

PACKAGE INFORMATION

SOT23-6



NOTE:
1.DIMENSIONS ARE IN MILLIMETERS.
2.DRAWING NOT TO SCALE.
3.DIMENSIONS ARE INCLUSIVE OF PLATING.
4.DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR.

Order information

Orderable Device	Package	Packing Option
AOZ6682CI-MS	SOT-23-6	3000PCS

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