# UMW FDS8958A

30V N-Channel MOSFET
-30V P-Channel MOSFET

## 1.Description

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

## 2.1Features(N-Ch)

- $V_{DS\ (V)}$=30V
- $I_D$=7A
- $R_{DS(ON)}$<28mΩ($V_{GS}$=10V)
- $R_{DS(ON)}$<40mΩ($V_{GS}$=4.5V)

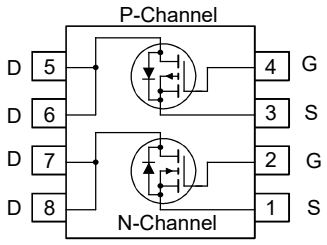
## 2.2Features(P-Ch)

- $V_{DS\ (V)}$=-30V
- $I_D$=-5A
- $R_{DS(ON)}$<52mΩ($V_{GS}$=-10V)
- $R_{DS(ON)}$<80mΩ($V_{GS}$=-4.5V)

## 3.Pinning information

| Pin | Symbol | Description |
|---|---|---|
| 1,3 | S | SOURCE |
| 2,4 | G | GATE |
| 5,6,7,8 | D | DRAIN |

**SOP-8**




## 4.Absolute Maximum Ratings $T_A$=25°C unless otherwise noted

| Parameter | Symbol | N-Channel | P-Channel | Units |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 30 | 30 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | ±20 | V |
| Drain Current – Continuous (Note 1a) | $I_D$ | 7 | -5 | A |
| – Pulsed | | 20 | -20 | |
| Drain-Source Avalanche Energy | $E_{AS}$ | 2 | | W |
| Power Dissipation for Dual Operation (Note 1a) | $P_D$ | 1.6 | | W |
| Power Dissipation for Single Operation (Note 1c) | | 0.9 | | W |
| Storage Junction Temperature Range | $T_J$, $T_{STG}$ | -55 to 150 | | °C |

## 5.Thermal Characteristics

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Thermal Resistance, Junction-to-Ambient (Note 1a) | $R_{\theta JA}$ | 78 | °C/W |
| Thermal Resistance, Junction-to-Case (Note 1) | $R_{\theta JC}$ | 40 | °C/W |

## 6.Electrical Characteristics $T_A$=25°C

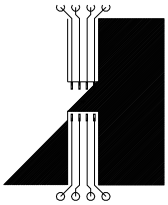
| Parameter | Symbol | | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | N-Ch | $I_D$=250μA, $V_{GS}$=0V | 30 | | | V |
| | | P-Ch | $I_D$=-250μA, $V_{GS}$=0V | -30 | | | V |
| Breakdown Voltage Temperature Coefficient | $\Delta BV_{DSS}/\Delta T_J$ | N-Ch | $I_D$=250μA,Reference to 25°C | | 25 | | mV/°C |
| | | P-Ch | $I_D$=-250μA,Reference to 25°C | | -23 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | N-Ch | $V_{DS}$=24V, $V_{GS}$=0V | | | 1 | μA |
| | | P-Ch | $V_{DS}$=-24V, $V_{GS}$=0V | | | -1 | μA |
| Gate-Body Leakage, Forward | $I_{GSSF}$ | All | $V_{GS}$=20V, $V_{DS}$=0V | | | 100 | nA |
| Gate-Body Leakage, Reverse | $I_{GSSR}$ | All | $V_{GS}$=-20V, $V_{DS}$=0V | | | -100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | N-Ch | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 1 | 1.9 | 3 | V |
| | | P-Ch | $V_{DS}$=$V_{GS}$, $I_D$=-250μA | -1 | -1.7 | -3 | V |
| Gate Threshold Voltage Temperature Coefficient | $\Delta V_{GS(th)}/\Delta T_J$ | N-Ch | $I_D$=250μA,Reference to 25°C | | -4.5 | | mV/°C |
| | | P-Ch | $I_D$=-250μA,Reference to 25°C | | 4.5 | | mV/°C |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | N-Ch | $V_{GS}$=10V, $I_D$=7A | | 19 | 28 | mΩ |
| | | | $V_{GS}$=4.5V, $I_D$=6A | | 24 | 40 | mΩ |
| | | P-Ch | $V_{GS}$=-10V, $I_D$=-5A | | 42 | 52 | mΩ |
| | | | $V_{GS}$=-4.5V, $I_D$=-4A | | 65 | 80 | mΩ |
| On-State Drain Current | $I_{D(on)}$ | N-Ch | $V_{GS}$=10V, $V_{DS}$=5V | 20 | | | A |
| | | P-Ch | $V_{GS}$=-10V, $V_{DS}$=-5V | -20 | | | A |
| Forward Transconductance | $g_{FS}$ | N-Ch | $V_{DS}$=5V, $I_D$=7A | | 25 | | S |
| | | P-Ch | $V_{DS}$=-5V, $I_D$=-5A | | 10 | | S |
| Input Capacitance | $C_{iss}$ | N-Ch | N-Ch: $V_{DS}$=15V, $V_{GS}$=0V, f =1MHz P-Ch: $V_{DS}$=-15V, $V_{GS}$=0V, f =1MHz | | 575 | | pF |
| | | P-Ch | | | 528 | | pF |
| Output Capacitance | $C_{oss}$ | N-Ch | | | 145 | | pF |
| | | P-Ch | | | 132 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | N-Ch | | | 65 | | pF |
| | | P-Ch | | | 70 | | pF |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Gate Resistance | $R_G$ | N-Ch | $V_{GS}$=15mV, f=1MHz | | 2.1 | | Ω |
| | | P-Ch | | | 6 | | Ω |
| Turn-On Delay Time | $t_{D(on)}$ | N-Ch | | | 8 | 16 | ns |
| | | P-Ch | N-Ch: | | 7 | 14 | ns |
| Turn-On Rise Time | $t_r$ | N-Ch | $V_{DD}$=15V, $I_D$=1A, | | 5 | 10 | ns |
| | | P-Ch | $V_{GS}$=10V, $R_{GEN}$=6Ω | | 13 | 24 | ns |
| Turn-Off Delay Time | $t_{D(off)}$ | N-Ch | P-Ch: | | 23 | 37 | ns |
| | | P-Ch | $V_{DD}$=-15V, $I_D$=-1A, | | 14 | 25 | ns |
| Turn-Off Fall Time | $t_f$ | N-Ch | $V_{GS}$=-10V, $R_{GEN}$=6Ω | | 3 | 6 | ns |
| | | P-Ch | | | 9 | 17 | ns |
| Total Gate Charge | $Q_g$ | N-Ch | | | 11.4 | 16 | nC |
| | | P-Ch | N-Ch: | | 9.6 | 13 | nC |
| Gate-Source Charge | $Q_{gs}$ | N-Ch | $V_{DS}$=15V, $I_D$=7A, $V_{GS}$=10V | | 1.7 | | nC |
| | | P-Ch | P-Ch: | | 2.2 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | N-Ch | $V_{DS}$=-15V, $I_D$=-5A, $V_{GS}$=-10V | | 2.1 | | nC |
| | | P-Ch | | | 1.7 | | nC |
| Maximum Continuous Drain-Source Diode Forward Current | $I_S$ | N-Ch | | | | 1.3 | A |
| | | P-Ch | | | | -1.3 | A |
| Maximum Plused Drain-Source Diode Forward Current (Note 2) | $I_{SM}$ | N-Ch | | | | 20 | A |
| | | P-Ch | | | | -20 | A |
| Drain-Source Diode Forward Voltage | $V_{SD}$ | N-Ch | $V_{GS}$=0V, $I_S$=1.3A (Note 2) | | 0.75 | 1.2 | V |
| | | P-Ch | $V_{GS}$=0V, $I_S$=-1.3A (Note 2) | | -0.88 | -1.2 | V |
| Diode Reverse Recovery Time | $t_{rr}$ | N-Ch | N-Ch: | | 19 | | ns |
| | | P-Ch | $I_F$=7A, $d_{iF}/d_t$=100A/μs | | 19 | | ns |
| Diode Reverse Recovery Charge | $Q_{rr}$ | N-Ch | P-Ch: | | 9 | | nC |
| | | P-Ch | $I_F$=-5A, $d_{iF}/d_t$=100A/μs | | 6 | | nC |

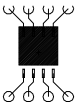
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

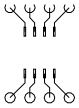
$R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 $in^2$ pad of 2 oz copper



b) 125°/W when mounted on a .02 $in^2$ pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Starting $T_J$=25°C, L=3mH, $I_{AS}$=6A, $V_{DD}$=30V, $V_{GS}$=10V (Q1).

Starting $T_J$=25°C, L=3mH, $I_{AS}$=3A, $V_{DD}$=30V, $V_{GS}$=10V (Q2)

## 7.1 Typical Characterisitics

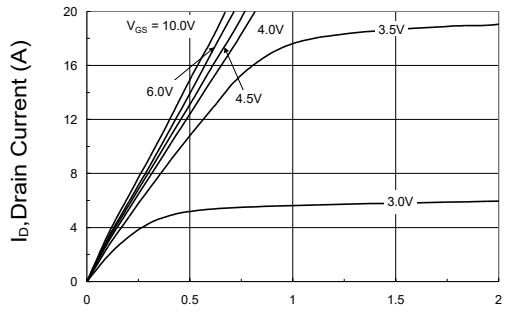



Figure 1: On-Region Characteristics

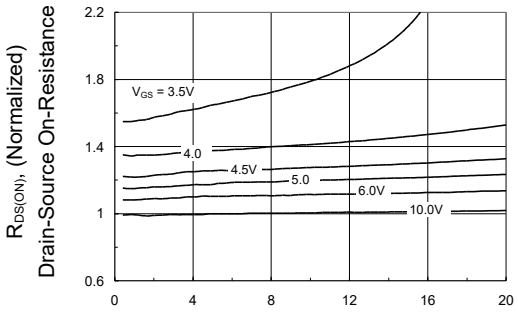



Figure 2: On-Resistance Variation with Drain Current and Gate Voltage

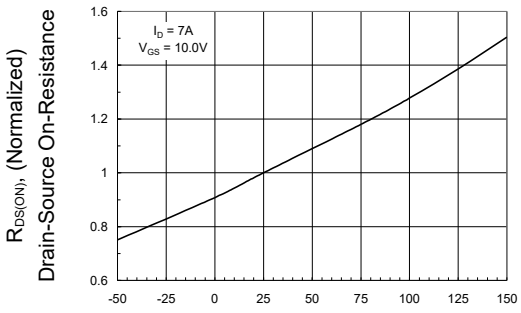



Figure 3: On-Resistance Variation with Temperature

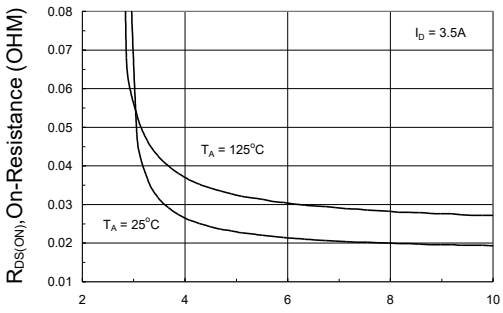



Figure 4: On-Resistance Variation with Gate-to-Source Voltage.

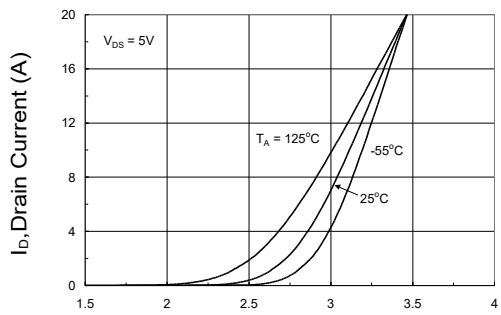



Figure 5: Transfer Characteristics

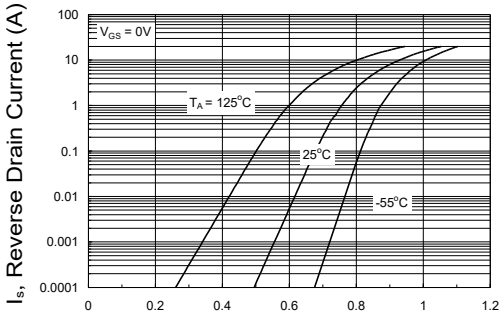



Figure 6: Body Diode Forward Voltage Variation with Source Current and Temperature

## 7.2 Typical Characterisitics

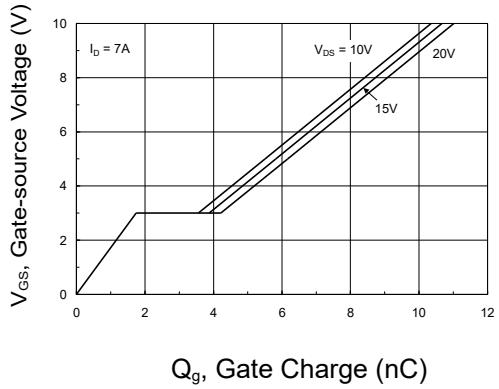



Figure 7: Gate Charge Characteristics

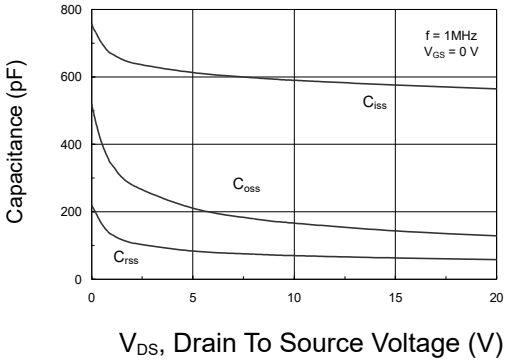



Figure 8: Capacitance Characteristics

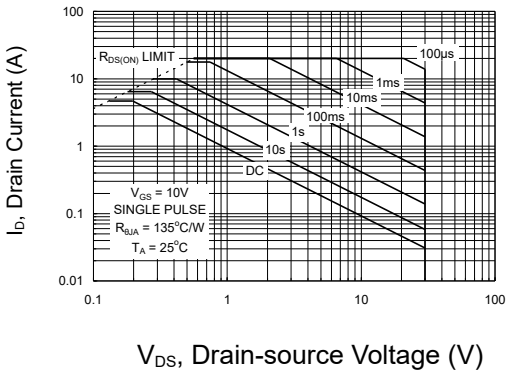



Figure 9: Maximum Safe Operating Area

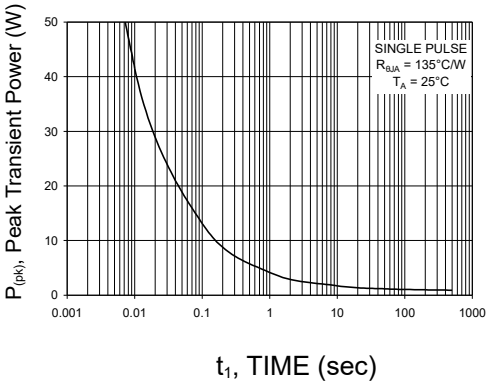



Figure 10: Single Pulse Maximum Power Dissipation

## 7.3 Typical Characterisitics

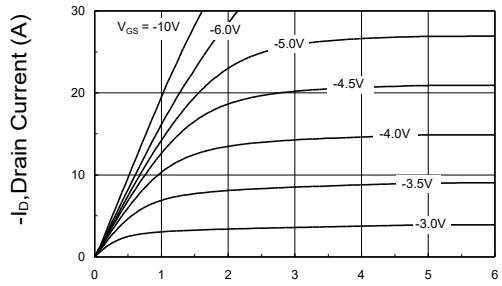



Figure 11: On-Region Characteristics

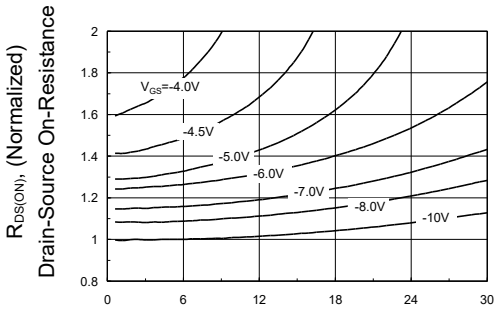



Figure 12: On-Resistance Variation with Drain Current and Gate Voltage

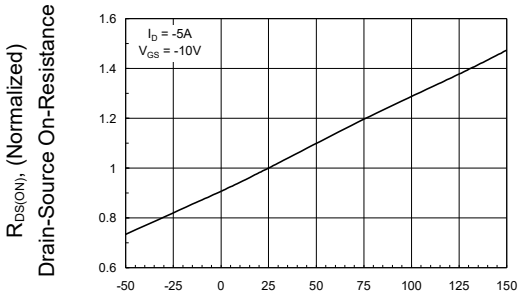



Figure 13: On-Resistance Variation with Temperature

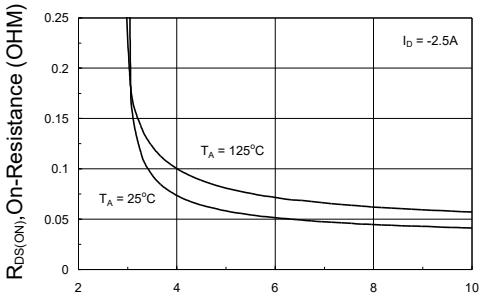



Figure 14: On-Resistance Variation with Gate-to-Source Voltage.

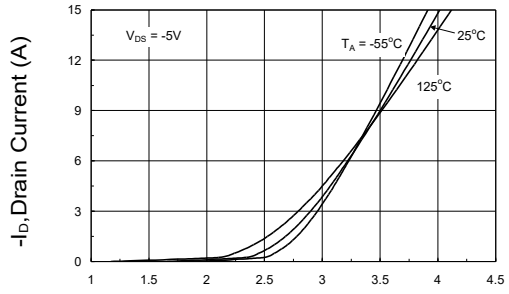



Figure 15: Transfer Characteristics

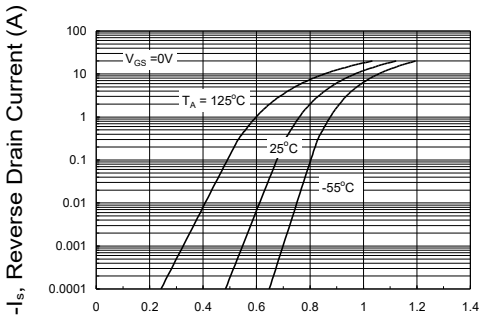
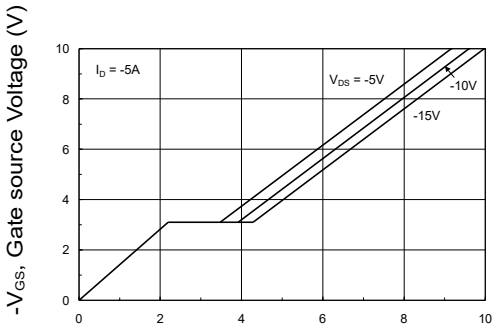


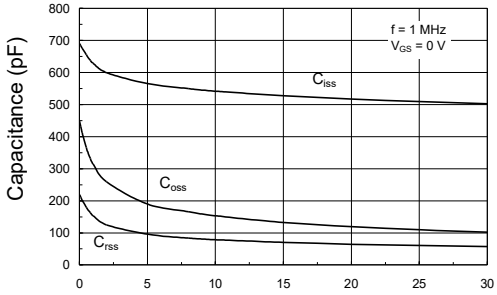

Figure 16: Body Diode Forward Voltage Variation with Source Current and Temperature

## 7.4 Typical Characterisitics



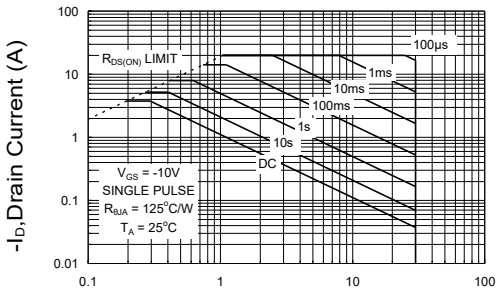

$Q_G$, Gate Charge (nC)

Figure 17: Gate Charge Characteristics



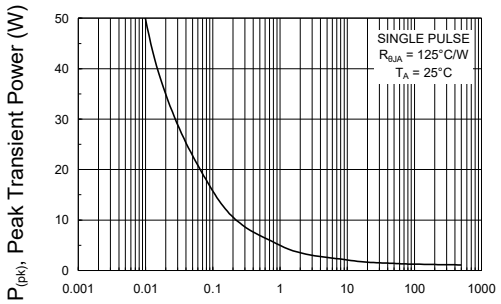

$-V_{DS}$,Drain to Source Voltage (V)

Figure 18: Capacitance Characteristics




$-V_{DS}$,Drain Source Voltage (V)

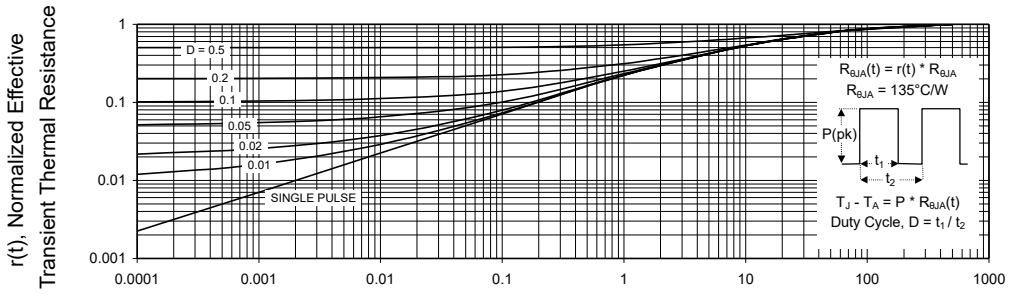
Figure 19: Maximum Safe Operating Area




$t_1$, TIME (sec)

Figure 20: Single Pulse Maximum Power Dissipation

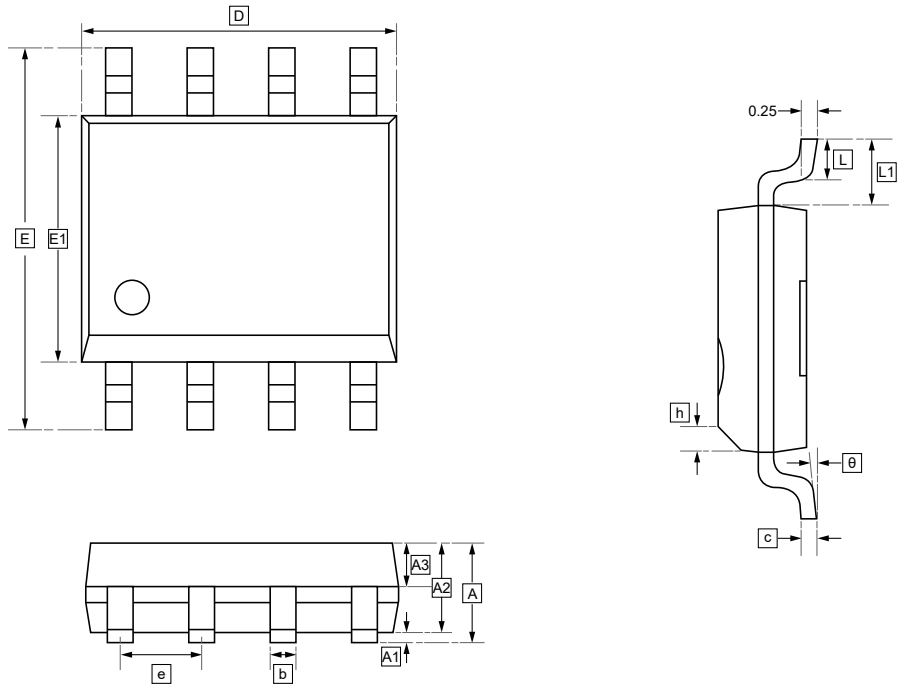
Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.




$t_1$, TIME (sec)

Figure 21: Transient Thermal Response Curve

## 8.SOP-8 Package Outline Dimensions

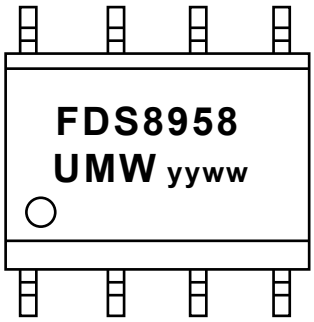



**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | A3 | b | c | D | E | E1 | e | h | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | - | 0.05 | 1.30 | 0.60 | 0.39 | 0.20 | 4.80 | 5.80 | 3.80 | 1.24 | 0.30 | 0.50 |
| Max | 1.75 | 0.20 | 1.50 | 0.70 | 0.47 | 0.24 | 5.00 | 6.20 | 4.00 | 1.30 | 0.50 | 0.80 |

| Symbol | L1 | θ |
|---|---|---|
| Min | 1.00 | 0° |
| Max | 1.10 | 8° |

## 9.Ordering information




yy: Year Code
ww: Week Code

| Order Code | Package | Base QTY | Delivery Mode |
|---|---|---|---|
| UMW FDS8958A | SOP-8 | 3000 | Tape and reel |

## 10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.