

1.Description

These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching and low in-line power loss are needed in a very small outline surface mount package

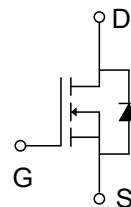
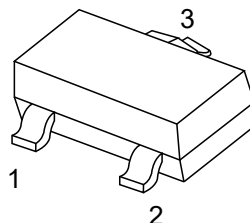
2.Features

- $V_{DS(V)}=30V$
- $I_D=2.2A$
- $R_{DS(ON)}<40m\Omega(V_{GS}=4.5V)$
- $R_{DS(ON)}<40m\Omega(V_{GS}=2.5V)$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23



4.Maximum ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage - Continuous	V_{GSS}	± 8	V
Drain/Output Current – Continuous – Pulsed	I_D	2.2	A
		10	
Maximum Power Dissipation (Note 1a) (Note 1b)	P_D	0.5	W
		0.46	
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}C$
Thermal Characteristics			
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	250	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	75	$^{\circ}C/W$



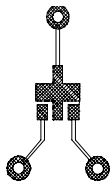
5. $T_A=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Breakdown Voltage Temp. Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA Referenced to 25°C		41		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			1	μA
		T _J =55°C			10	μA
Gate - Body Leakage, Forward	I _{GSSF}	V _{GS} =8V, V _{DS} =0V			100	nA
Gate - Body Leakage, Reverse	I _{GSSR}	V _{GS} =-8V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS (Note)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.4	0.7	1	V
Gate Threshold Voltage Temp. Coefficient	ΔV _{GS(th)} /T _J	I _D =250μA Referenced to 25°C		-2.3		mV/°C
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =2.2A		54	40	mΩ
		V _{GS} =2.5V, I _D =2A		40	82	
On-State Drain Current	I _{D(ON)}	V _{GS} =4.5V, V _{DS} =5V	10			A
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =2.2A		13		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =10V, f=1MHz		300		pF
Output Capacitance	C _{oss}			145		pF
Reverse Transfer Capacitance	C _{rss}			35		pF
SWITCHING CHARACTERISTICS (Note)						
Turn - On Delay Time	t _{D(on)}	V _{DD} =5V, I _D =1A V _{GS} =4.5V, R _{GEN} =6Ω		4	10	ns
Turn - On Rise Time	t _r			10	18	ns
Turn - Off Delay Time	t _{D(off)}			17	28	ns
Turn - Off Fall Time	t _f			4	10	ns

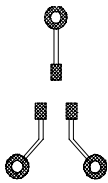


Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-2A		7	9	nC
Gate-Source Charge	Q _{gs}			1.1		nC
Gate-Drain Charge	Q _{gd}	V _{GS} =-4.5V		1.9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain–Source Diode Forward Current	I _s				0.42	A
Drain–Source Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _s =0.42A (Note)		0.65	1.2	V

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. Typical $R_{\theta JA}$ using the board layouts shown below on FR-4 PCB in a still air environment :



a. 250°C/W when mounted on
a 0.02 in² pad of 2oz Cu.



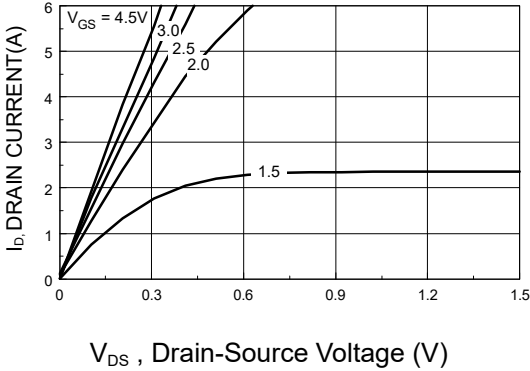
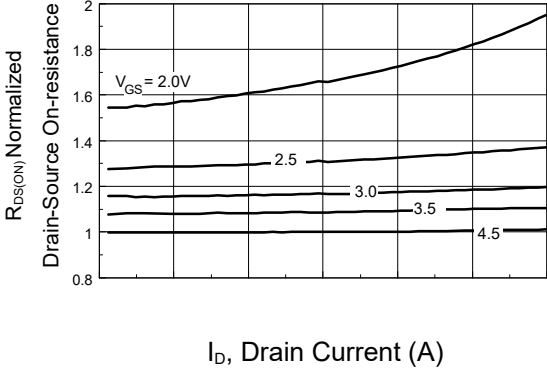
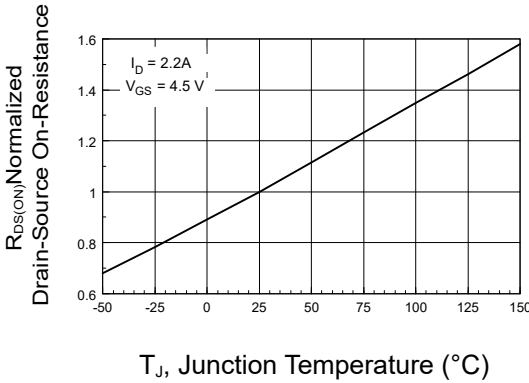
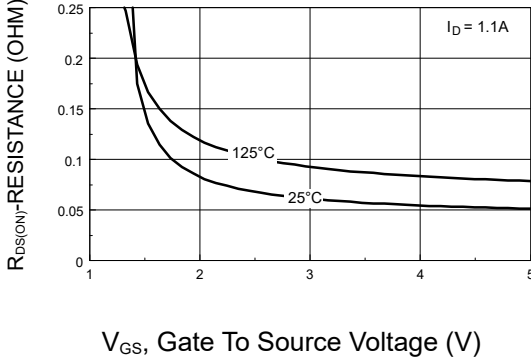
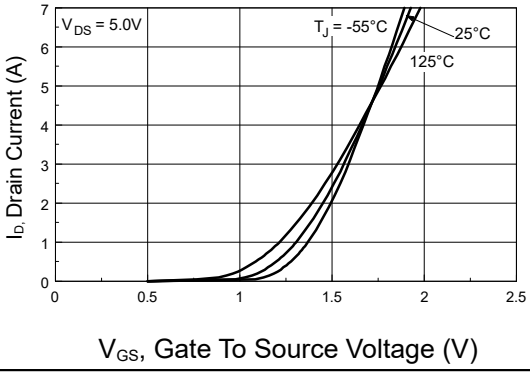
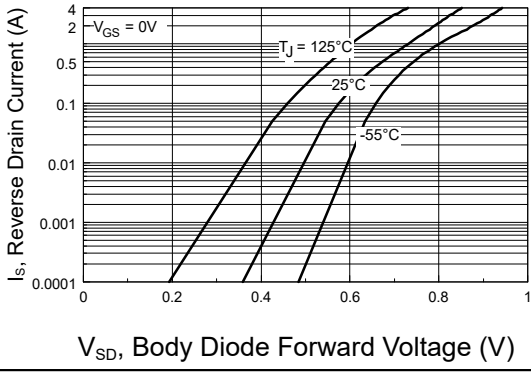
b) 270°C/W when mounted on a
0.001 in² pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



6.1 Typical Characteristics

	
Figure 1: On-Region Characteristics.	Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.
	
Figure 3: On-Resistance Variation with Temperature.	Figure 4: On-Resistance Variation with Gate-to-Source Voltage.
	
Figure 5: Transfer Characteristics.	Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.



6.2 Typical Characteristics

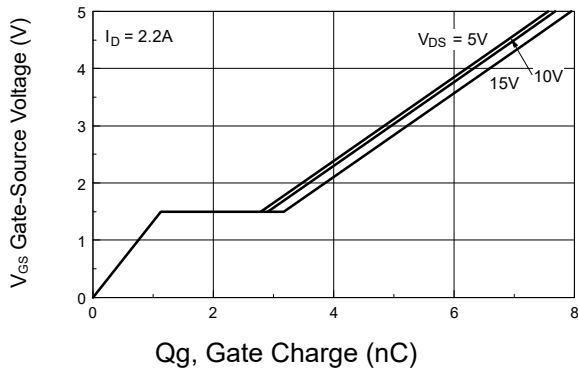


Figure 7: Gate-Charge Characteristics

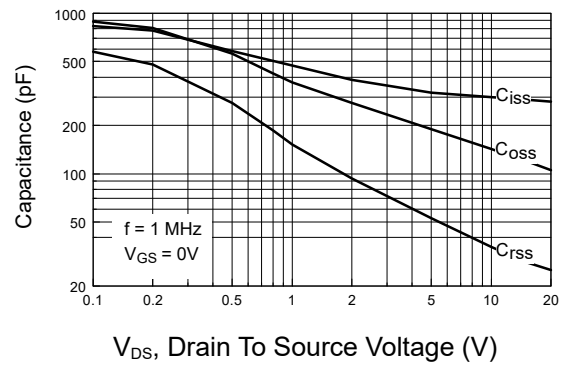


Figure 8: Capacitance Characteristics

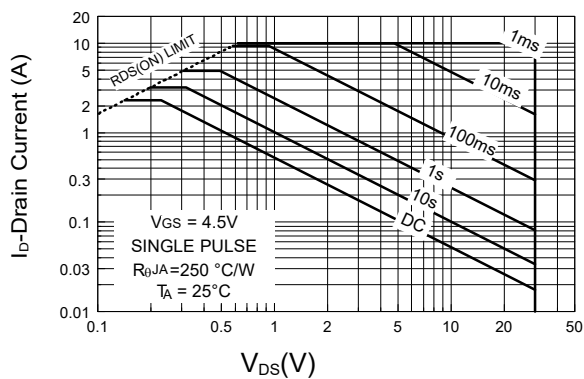


Figure 9: Maximum Safe Operating Area.

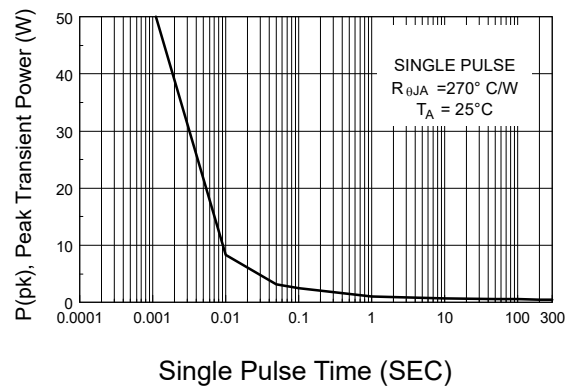


Figure 10: Single Pulse Maximum Power Dissipation.

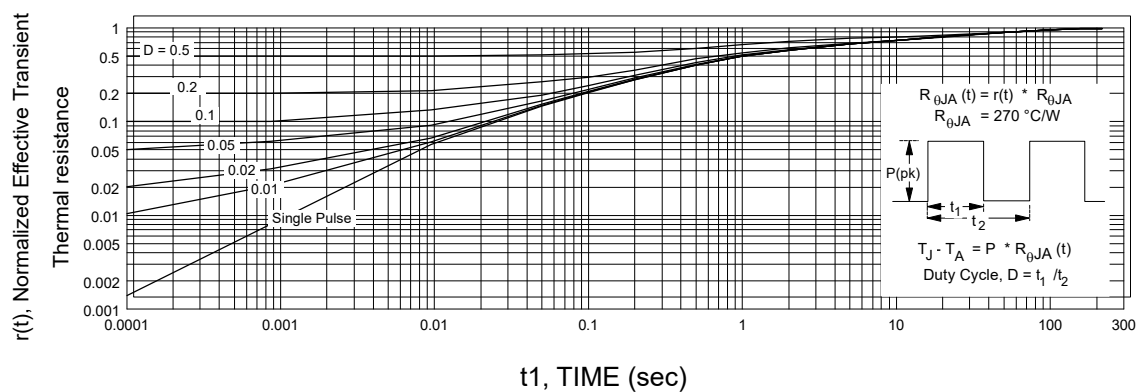
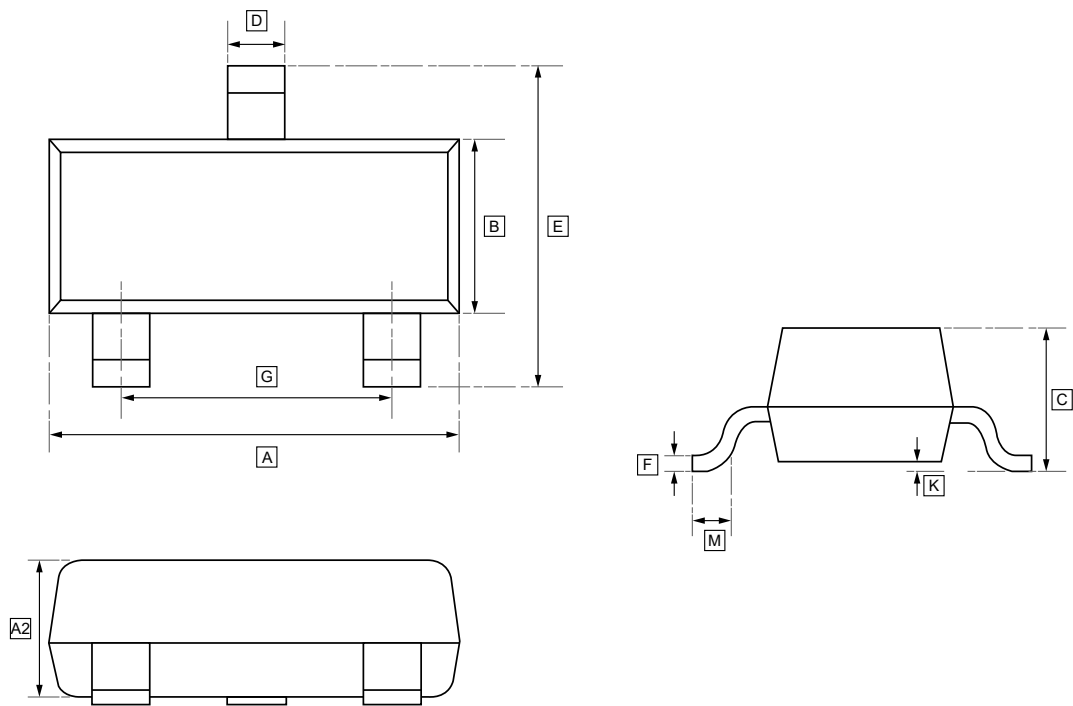


Figure 11. Transient Thermal Response Curve.



7.SOT-23 Package Outline Dimensions

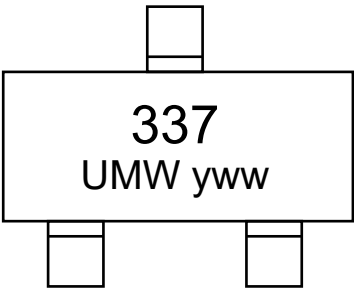


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	D	E	G	K	M	A2	F
Min	2.85	1.20	0.90	0.40	2.25	1.80	0.00	0.30	0.95	0.095
Max	3.04	1.40	1.10	0.50	2.55	2.00	0.10	-	1.05	0.115



8.Ordering Information



yww: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDN337N	SOT-23	3000	Tape and reel



9.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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