UMW FDD6796A

25V N-Channel MOSFET

1.Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

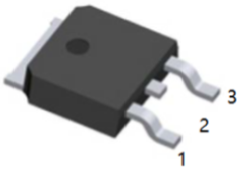
2.Features

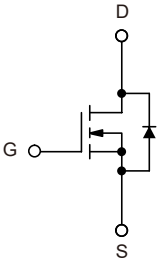
- $V_{DS\ (V)}$=25V
- I_D=40A
- $R_{DS(ON)}$<5.7mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<15mΩ(V_{GS}=4.5V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_C= 25°C

Parameter		Symbol	Rating	Units
Drain to Source Voltage		V_{DS}	25	V
Gate to Source Voltage		V_{GS}	±20	
Drain Current -Continuous (Package limited)	T_C=25°C	I_D	40	A
-Continuous (Silicon limited)	T_C=25°C		67	
-Continuous	T_A=25°C (Note 1a)		20	
-Pulsed			150	
Single Pulse Avalanche Energy	(Note 3)	E_{AS}	40	mJ
Power Dissipation	T_C=25°C	P_D	42	W
Power Dissipation	T_A=25°C (Note 1a)		3.7	
Storage Junction Temperature Range		T_J, T_{STG}	-55 to 175	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction to Case		$R_{\theta JC}$	3.6	°C/W
Thermal Resistance, Junction to Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W

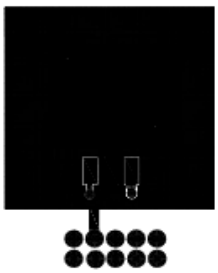
6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	25			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		16		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V, V_{GS}=0V			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.9	3	V
Gate to Source Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		-6		mV/°C
Static Drain to Source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		4.3	5.7	mΩ
		V_{GS}=4.5V, I_D=15.2A		11.1	15	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=20A		118		S
Input Capacitance	C_{iss}	V_{DS}=13V, V_{GS}=0V f=1MHz		1336	1780	pF
Output Capacitance	C_{oss}			298	400	pF
Reverse Transfer Capacitance	C_{rss}			266	400	pF
Gate Resistance	R_g			1.2		Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=13V, I_D=20A V_{GS}=10V, R_{GEN}=6Ω		8	16	ns
Rise Time	t_r			7	14	ns
Turn-Off DelayTime	$t_{D(off)}$			19	34	ns
Fall Time	t_f			4	10	ns
Total Gate Charge	Q_g	V_{GS}=0V to 10V		24	34	nC
Total Gate Charge	Q_g	V_{GS}=0V to 5V		14	20	nC
Gate to Source Gate Charge	Q_{gs}	V_{DD}=13V I_D=20A		4		nC
Gate to Drain “Miller” Charge	Q_{gd}			5.7		nC
Source to Drain Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=3.1A (Note 2)		0.8	1.2	V
		V_{GS}=0V, I_S=20A (Note 2)		0.9	1.3	V
Reverse Recovery Time	t_{rr}	I_F=20A, di/dt=100A/μs		15	27	ns
Reverse Recovery Charge	Q_{rr}			4	10	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the drain tab.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40°C/W when mounted on a $1in^2$ pad of 2oz copper.

b) 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3: E_{AS} of 40 mJ is based on starting T_J=25 °C, L=1mH, I_{AS}=9A, V_{DD}=23 V, V_{GS}=10 V. 100% test at L=0.1mH, I_{AS}= 1 A.

7.1Typical characteristic

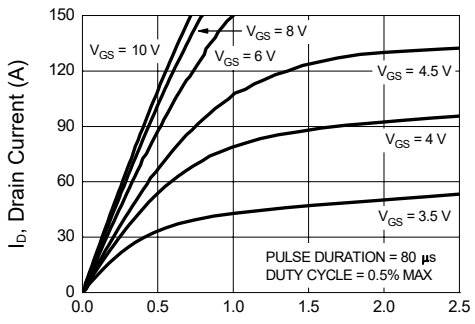


Figure 1: On-Region Characteristics

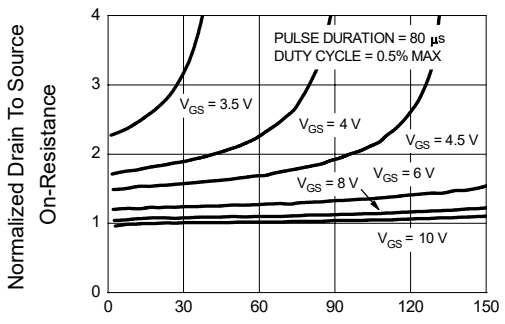


Figure 2: Normalized On-Resistance vs Drain Current and Gate Voltage

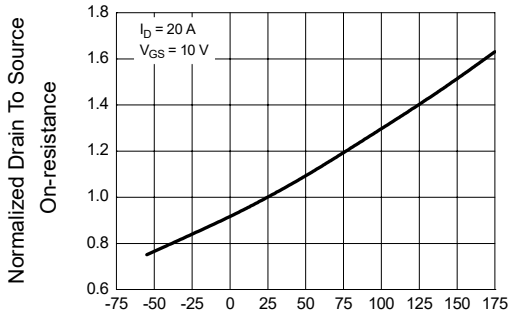


Figure 3: Normalized On Resistance vs Junction Temperature

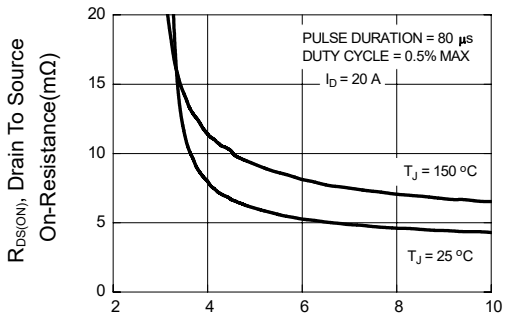


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

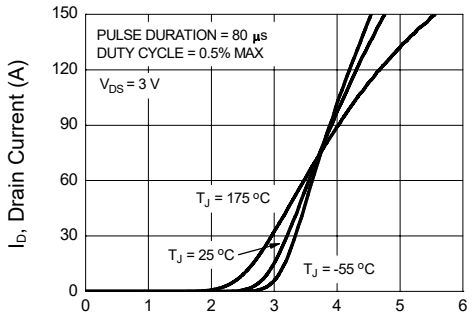


Figure 5: Transfer Characteristics

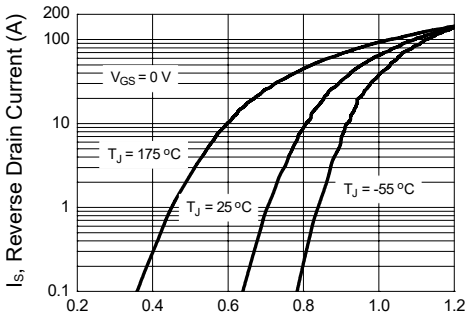


Figure 6: Source to Drain Diode Forward Voltage vs Source Current

7.2Typical characteristic

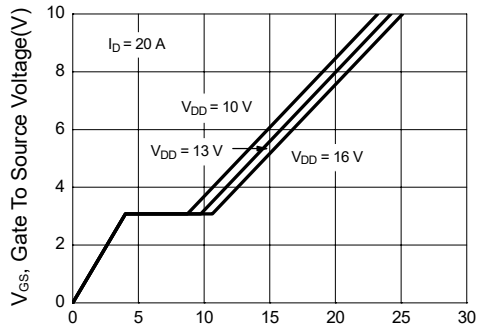


Figure 7: Gate Charge Characteristics

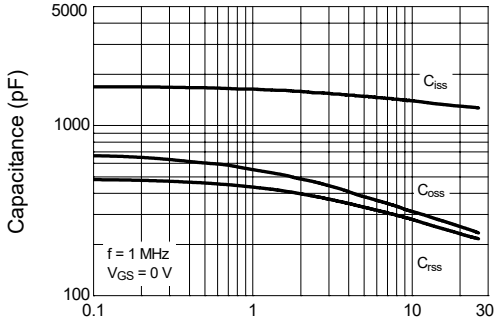


Figure 8: Capacitance vs Drain to Source Voltage

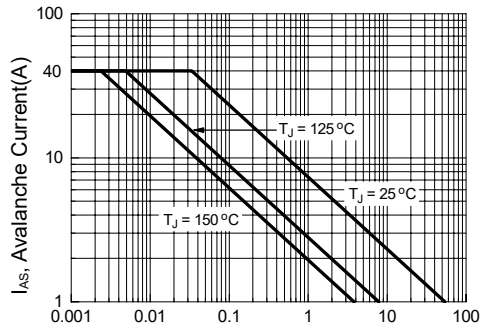


Figure 9: Unclamped Inductive Switching Capability

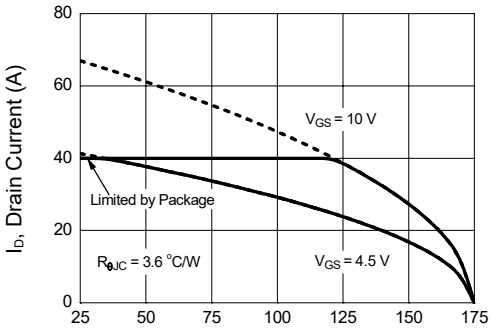


Figure 10: Maximum Continuous Drain Current vs Case Temperature

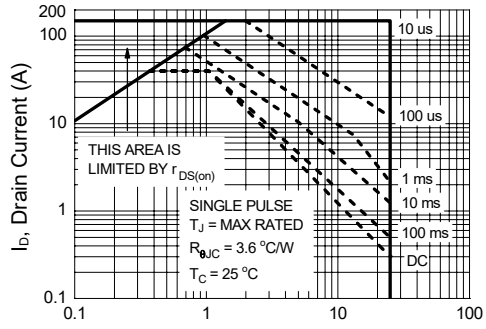


Figure 11: Forward Bias Safe Operating Area

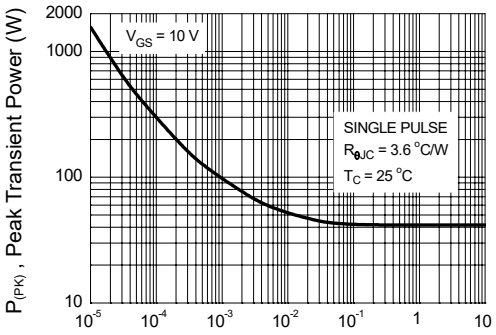


Figure 12: Single Pulse Maximum Power Dissipation

7.3Typical characteristic

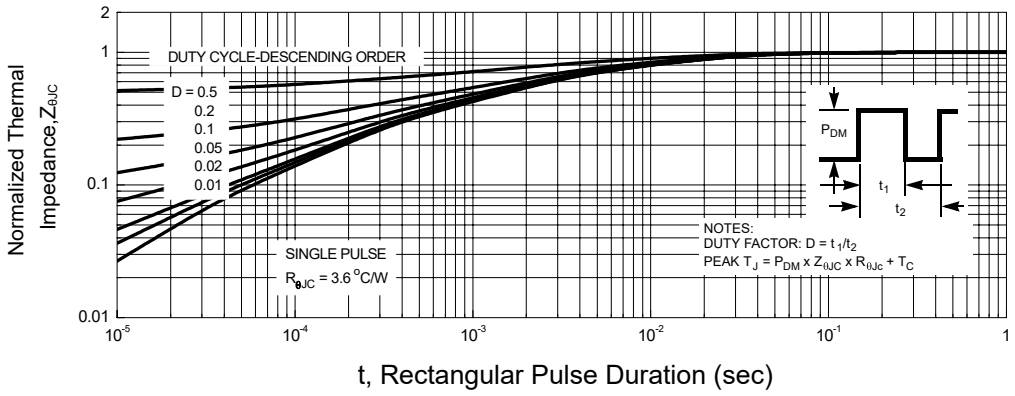


Figure 13: Transient Thermal Response Curve

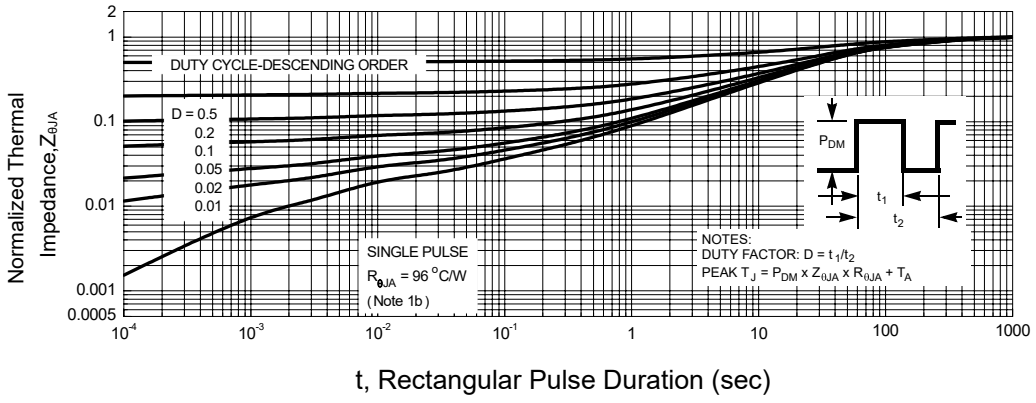
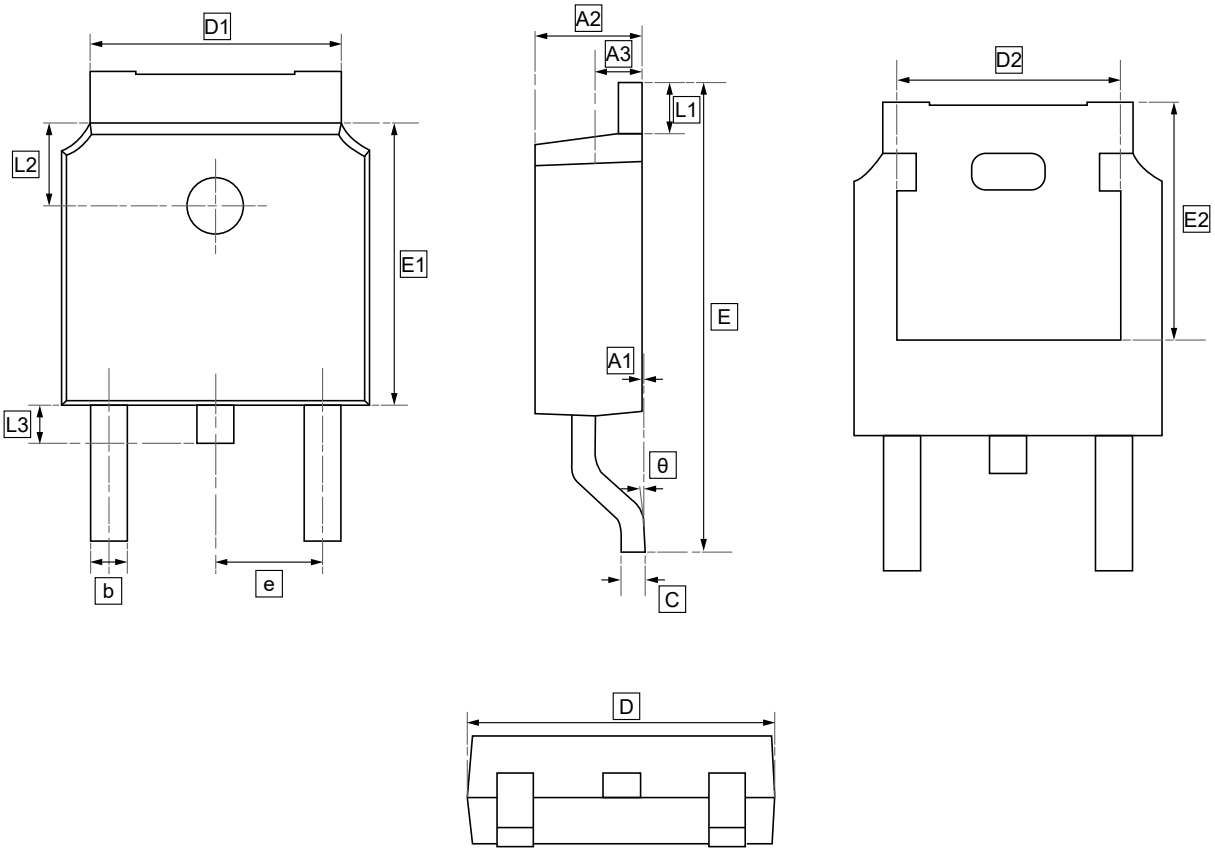


Figure 14: Transient Thermal Response Curve

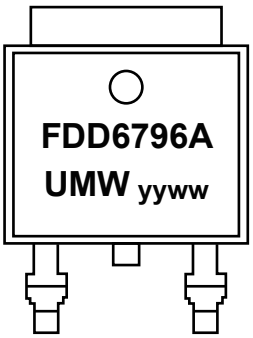
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD6796A	TO-252	2500	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.