

1.Description

STN4438 is the N-Channel logiceenhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

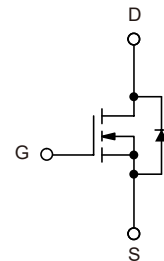
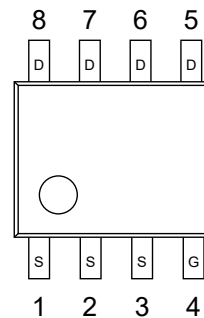
2.Features

- $V_{DS(V)}=60V$
- $R_{DS(ON)}<32m\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<37m\Omega(V_{GS}=4.5V)$

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings $T_A=25^{\circ}C$

Parameter		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current ($T_J=150^{\circ}C$)	$T_A=25^{\circ}C$	I_D	8.2	A
	$T_A=70^{\circ}C$		6.6	
Pulsed Drain Current		I_{DM}	40	
Continuous Source Current (Diode Conduction)		I_S	3	
Power Dissipation	$T_A=25^{\circ}C$	P_D	3.1	W
	$T_A=70^{\circ}C$		2	W
Operation Junction Temperature		T_J	150	$^{\circ}C$
Storage Temperature Range		T_{STG}	-55 to 150	$^{\circ}C$
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	70	$^{\circ}C/W$



5. $T_A=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
Gate-source leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS}=48V, V_{GS}=0V$			1	μA
		$V_{DS}=48V, V_{GS}=0V, T_J=50^{\circ}\text{C}$			5	μA
On-State Drain Current	$I_{D(ON)}$	$V_{DS}\geq 5V, V_{GS}=10V$	40			A
Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=8A$		25	32	m Ω
		$V_{GS}=4.5V, I_D=6.6A$		30	37	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=6.2A$		24		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total gate charge	Q_g	$V_{DS}=30V, V_{GS}=10V, I_D=8.2A$		48	58	nC
Gate-Source Charge	Q_{gs}			24.2	30	nC
Gate-Drain Charge	Q_{gd}			14.5		nC
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V, f=1\text{MHz}$		1600		pF
Output Capacitance	C_{oss}			155		pF
Reverse Transfer Capacitance	C_{rss}			116		pF
Turn-On Time	$t_{D(on)}$	$V_{DS}=30V, R_L=3.6\Omega$		8.5		nS
	t_r			6		nS
Turn-Off Time	$t_{D(off)}$	$V_{GEN}=3V$		29		nS
	t_f			6		nS



6.1 Typical Characteristics

Figure 1: On-Region Characteristics	Figure 2: Transfer Characteristics
Figure 3: On-Resistance vs. Drain Current and Gate Voltage	Figure 4: On-Resistance vs. Junction Temperature
Figure 5: On-Resistance vs. Gate-Source Voltage	Figure 6: Body-Diode Characteristics



6.2 Typical Characteristics

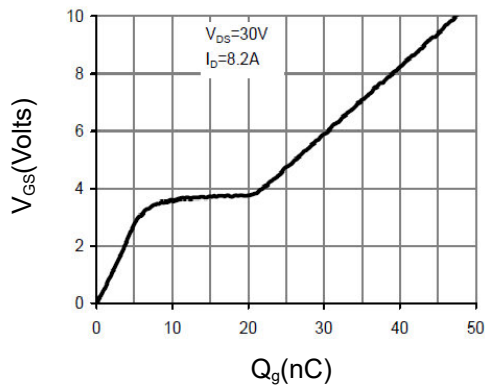


Figure 7: Gate-Charge Characteristics

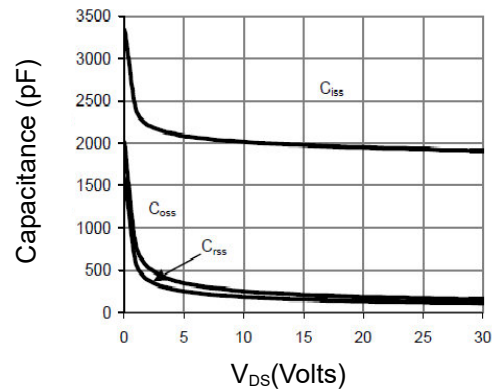


Figure 8: Capacitance Characteristics

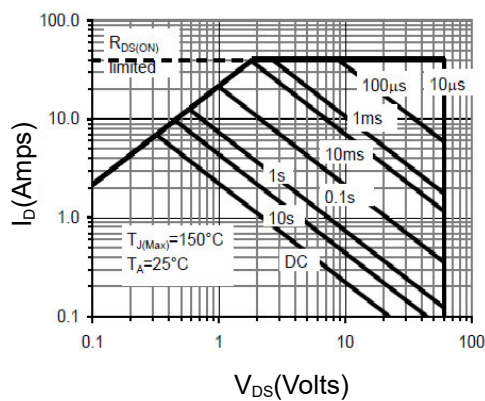


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

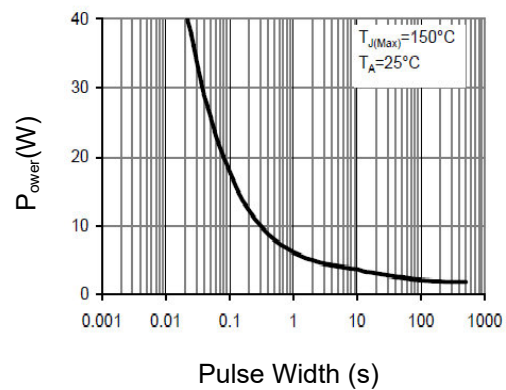


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

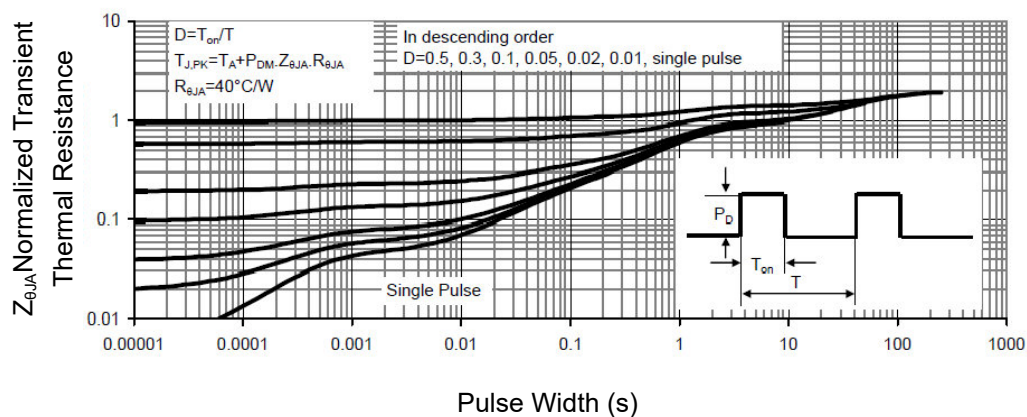
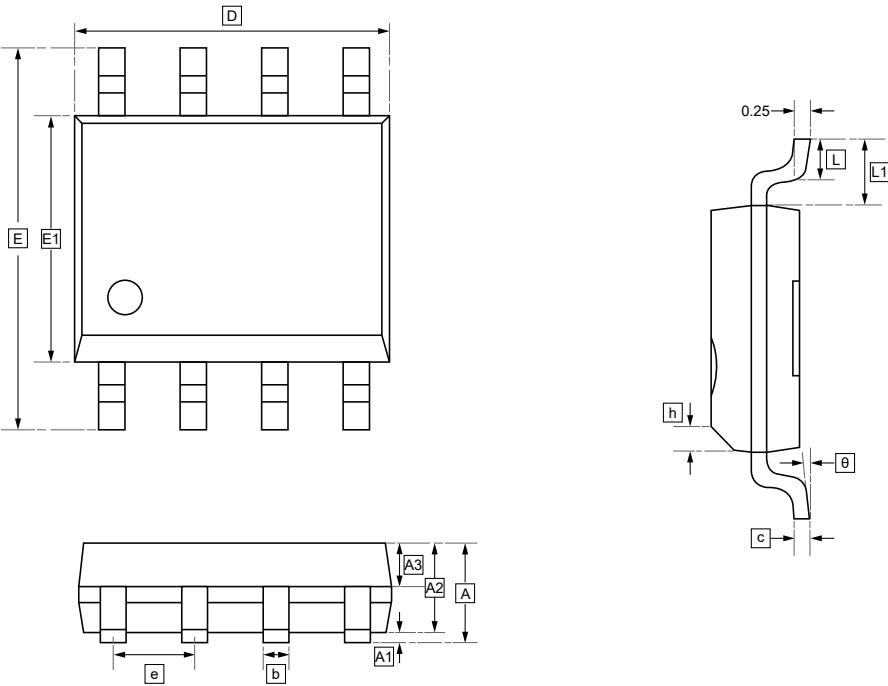


Figure 11: Normalized Maximum Transient Thermal Impedance



7.SOP-8 Package Outline Dimensions



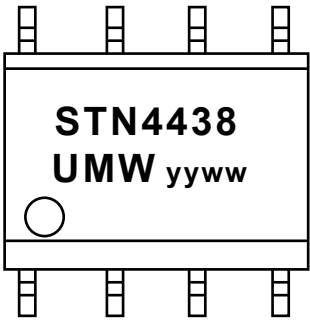
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW STN4438	SOP-8	3000	Tape and reel



9.Disclaimer

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