UMW FDS8984

Dual 30V N-Channel MOSFET

1.Description

This Dual 30V N-channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized forlow gate charge, low $R_{DS(ON)}$ and fast switching speed.

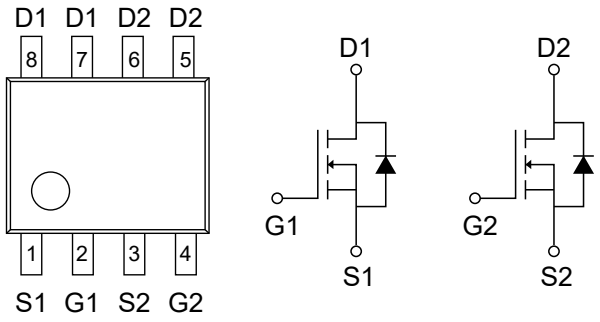
2.Features

- $V_{DS\ (V)}$=30V
- I_D=7A
- $R_{DS(ON)}$<23mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<30mΩ(V_{GS}=4.5V)
- Low gate charge

3.Pinning information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Drain to Source Voltage		V_{DS}	30	V
Gate to Source Voltage		V_{GS}	±20	V
Drain Current Continuous		I_D	7	A
Pulsed	(Note 1a)		30	A
Single Pulse Avalanche Energy	(Note 2)	E_{AS}	32	mJ
Power dissipation		P_D	1.6	W
Derate above 25°C			13	mW/°C
Operating and Storage Temperature		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	78	°C/W
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JA}$	40	°C/W

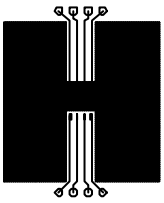
6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		23		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
		T_J=125°C			250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2	1.7	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		-4.3		mV/°C
Drain to Source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=7A		19	23	mΩ
		V_{GS}=4.5V, I_D=6A		24	30	mΩ
Input Capacitance	C_{iss}	V_{DS}=15V		475	635	pF
Output Capacitance	C_{oss}	V_{GS}=0V		100	135	pF
Reverse Transfer Capacitance	C_{rss}	f =1MHz		65	100	pF
Gate Resistance	R_G	f =1MHz		0.9	1.6	Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=15V, I_D=7A V_{GS}=10V, R_{GS}=33Ω		5	10	ns
Rise Time	t_r			9	18	ns
Turn-Off DelayTime	$t_{D(off)}$			42	68	ns
Fall Time	t_f			21	34	ns
Total Gate Charge	Q_g	V_{DS}=15V,I_D=7A,V_{GS}=10V		9.2	13	nC
Total Gate Charge	Q_g	V_{DS}=15V, I_D=7A V_{GS}=5V		5	7	nC
Gate to Source Gate Charge	Q_{gs}			1.5		nC
Gate to Drain “Miller” Charge	Q_{gd}			2		nC
Source to Drain Diode Voltage	V_{SD}	I_{SD}=7A		0.9	1.25	V
		I_{SD}=2.1A		0.8	1	V

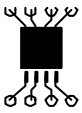
Diode Reverse Recovery Time	t_{rr}	I_F=7A, d_{IF}/d_t=100A/μs			33	nS
Diode Reverse Recovery Charge	Q_{rr}				20	nC

Notes:

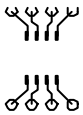
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in ^{2} pad of 2 oz copper.



b) 125° C/W when mounted on a 0.02 in ^{2} pad of oz. copper.



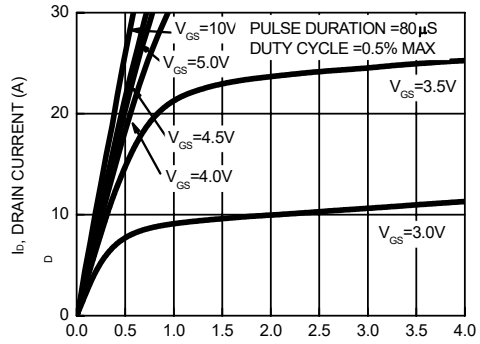
c) 135° C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2: Starting T_J =25°C, L =1mH, I_{AS}=8A, V_{DD}=27V, V_{GS}=10V.

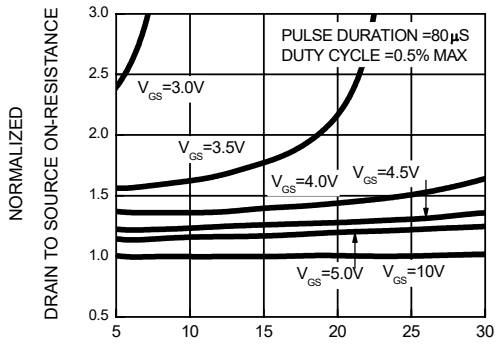
3: Pulse Test:Pulse Width <300μs, Duty Cycle <2%.

7.1TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



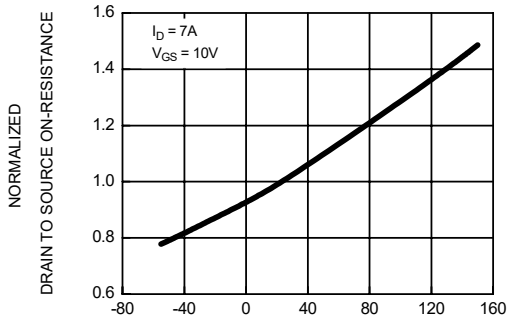
V_{DS}, DRAIN TO SOURCE VOLTAGE (V)

Figure 1: On-Region Characteristics.



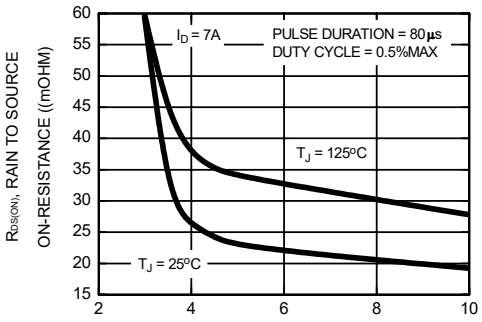
I_D, DRAIN CURRENT (A)

Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.



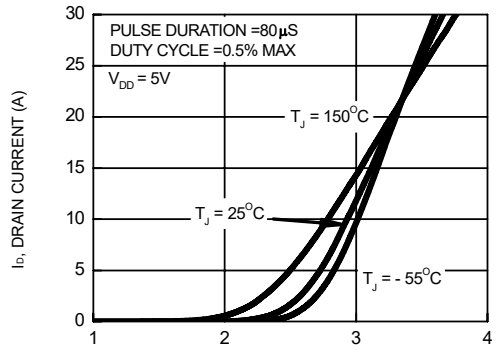
T_J, JUNCTION TEMPERATURE (°C)

Figure 3: On-Resistance Variation with Temperature.



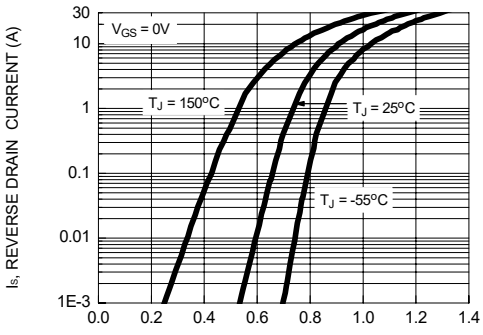
V_{GS}, GATE TO SOURCE VOLTAGE (V)

Figure 4: On-Resistance vs Gate to Source Votlage.



V_{GS}, GATE TO SOURCE VOLTAGE (V)

Figure 5: Transfer Characteristics.



V_{SD}, BODY DIODE FORWARD VOLTAGE (V)

Figure 6: Source to Drain Diode Forward Voltage vs Source Current.

7.2TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

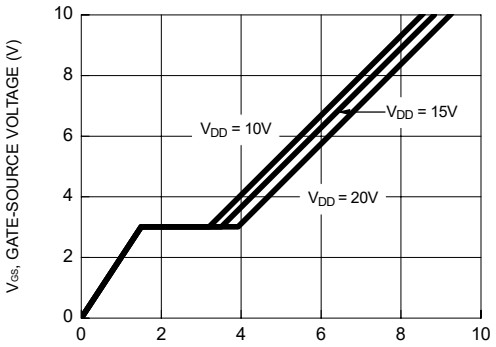


Figure 7: Gate-Charge Characteristics.

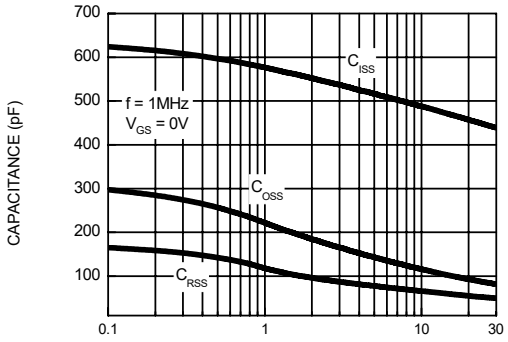


Figure 8: Capacitance vs Drain to Source Voltage.

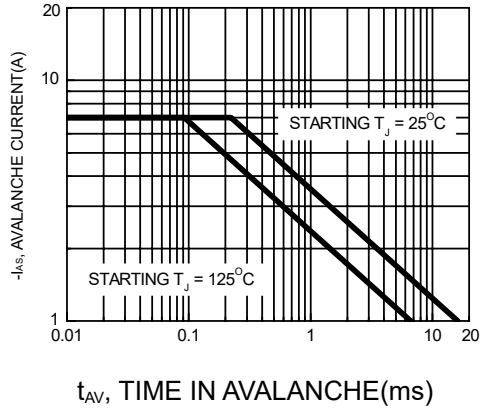


Figure 9: Unclamped Inductive Switching Capability.

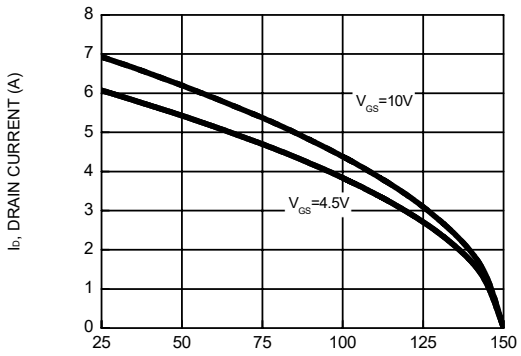


Figure 10: Maximum Continuous Drain Current vs Ambient Temperature.

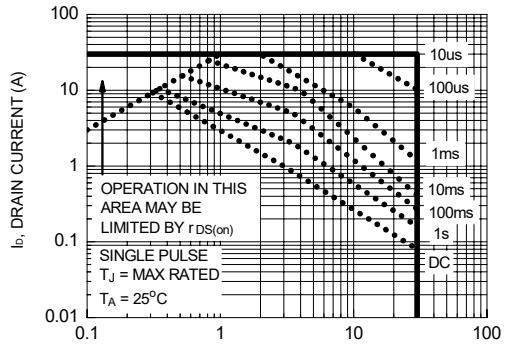


Figure 11: Forward Bias Safe Operating Area.

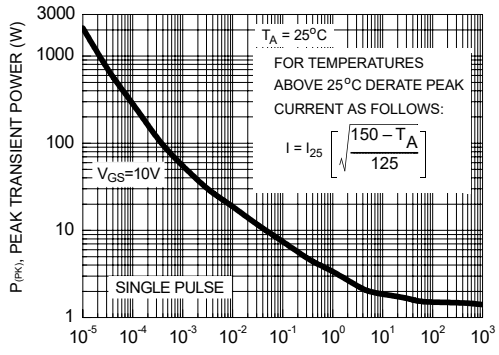


Figure 12: Single Pulse Maximum Power Dissipation.

7.3Typical Characterisitics

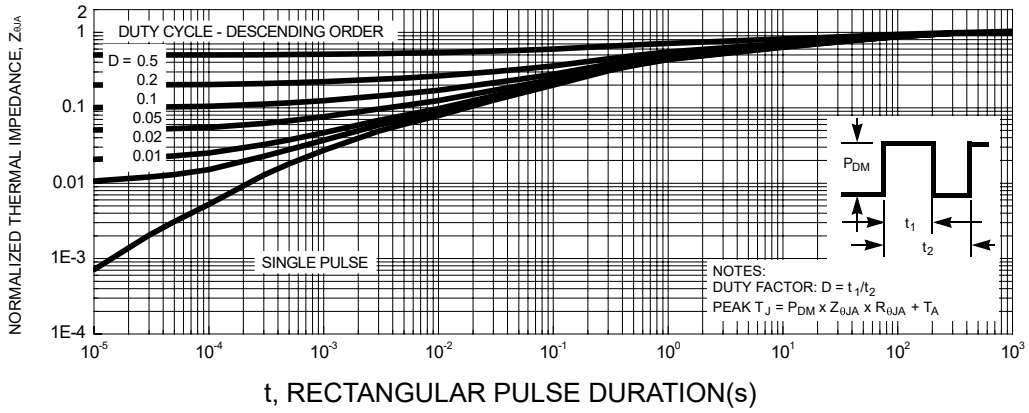
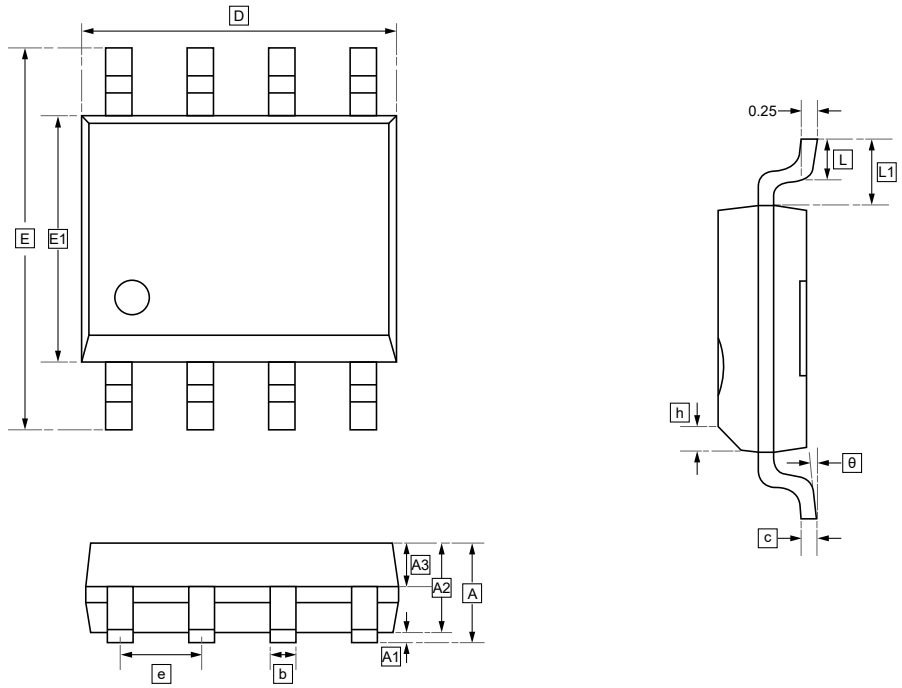


Figure 13: Transient Thermal Response Curve.

8.SOP-8 Package Outline Dimensions

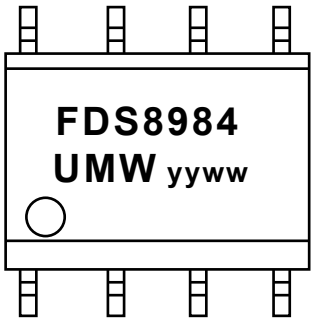


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS8984	SOP-8	3000	Tape and reel

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