UMW TMP709

Resistor-programmable Temperature Switch

1.Description

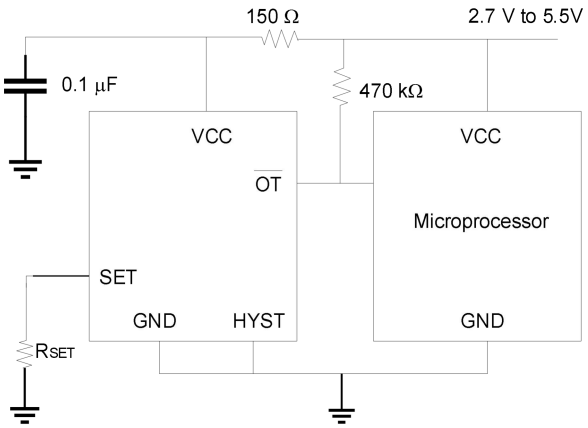
The TMP709 is a fully integrated, resistor-programmable temperature switch with a temperature threshold that is set by just one external resistor within the entire operating range. The TMP709 provides an open-drain, active-low output and has a 2.7V to 5.5V supply-voltage range. The temperature threshold accuracy is typically ±0.5°C, with a maximum of ±3°C (60°C to 100°C). The quiescent current consumption is typically 33µA. Hysteresis is pinselectable to 2°C or 10°C. The TMP709 is available in a 5-pin SOT-23 and small DFN 6 package.

2.Features

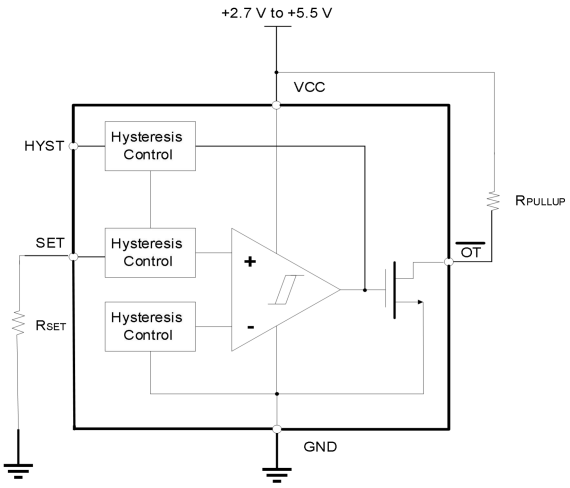
- Threshold accuracy:
  – ± 0.5°C Typical
  - ± 3°C Maximum (+ 60°C to 100°C)
- Temperature threshold set by 1% external resistor
- Low quiescent current: 33µA typical
- Open-drain, active-low output stage
- Pin-selectable 2°C or 10°C hysteresis
- Reset operation specified at VCC =0.8V
- Power range: 2.7V to 5.5V
- Packaging: 5-pin SOT23, 6-pin DFN package

3.Applications

- Computers (laptops and desktops)
- servers
- Industrial and medical equipment
- Storage Area Networks
- Automobiles

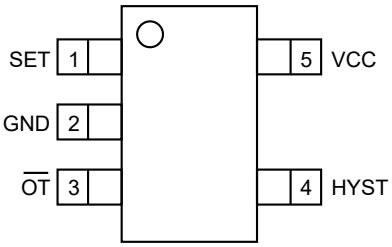


Typical Application

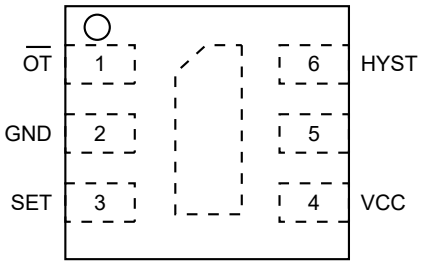


Chip Internal Structure Diagram

4.Pinning Information



SOT23-5



DFN6

Pin Functions

Pin			Description
SOT23-5	DFN6	Name	
1	3	SET	Temperature set point. Connect an external 1% resistor between SET and GND
2	2	GND	Device ground
3	1	$\overline{OT}$	Open-drain, active-low output
4	6	HYST	Hysteresis selection. For 10°C, HYST = VCC; for 2°C, HYST = GND
5	4	VCC	Supply voltage pin. The voltage range is 2.7V to 5.5V
	5	NC	No connection

5.Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage VCC	-0.3	6	V
$\overline{OT}$ Pin Voltage	-0.3	6	V
HYST and SET Pin Voltage	-0.3	(V_{CC}+0.3)	V
Operating Temperature	-40	125	°C
Junction Temperature		150	°C
Storage Temperature	-65	150	°C

Unless otherwise stated, over operating free-air temperature range. Stress above these ratings may cause permanent damage to the device.

6.ESD Ratings

Parameter		Value	Unit
Electrostatic Discharge Voltage, V_{ESD}	Human-body Model (HBM)	5000	V
	Charged-device Model (CDM)	2000	V
	Latch up Test	100	mA
	Machine Model (MM)	200	V

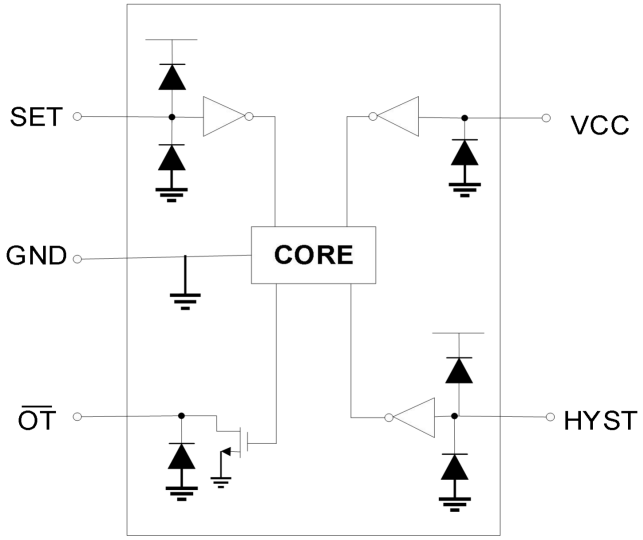
7.Recommended Operating Conditions

Parameter	Symbol	Min	Nom	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	5.5	V
Operating Temperature	T_A	0		125	°C

Unless otherwise stated, the specifications in the above table apply within the atmospheric temperature range.

8.Thermal Information

Parameter	Symbol	DBV(SOT23)	Unit
		5 PINS	
Junction to ambient thermal resistance	θ_{JA}	217.9	°C/W
Junction to chip case (top) thermal resistance	θ_{JCtop}	86.3	°C/W
Junction to board thermal resistance	θ_{JB}	44.6	°C/W
Junction to top characterization parameters	ψ_{JT}	4.4	°C/W
Junction to circuit board characterization parameters	ψ_{JB}	43.8	°C/W
Junction to chip case (bottom) thermal resistance	θ_{JCbo}	unavailable	°C/W



TMP709 Internal ESD Equivalent Circuit

9.Electrical Characteristics

Unless otherwise specified, electrical characteristics of devices at T_A=0°C to +125°C and V_{CC}=2.7V ~ 5.5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply voltage range	V_{CC}		2.7		5.5	V
Supply current	I_{CC}	V_{CC}=5V		33	55	μA
		V_{CC}=2.7V		33	55	μA
Temperature						
Temperature error	T_E	T_A=+60°C to + 100°C		±0.5	±3	°C
Digital input (HYST)						
High level input voltage	V_{IH}		0.7×V_{CC}			V
Low level input voltage	V_{IL}				0.3×V_{CC}	V
Input capacitance	C_{IN}			10		pF
Analog input (SET)						
Input voltage range	V_{IN}		0		V_{CC}	V
Input leakage current	I_{lkg_in}			1		μA
Digital open-drain output (OT)						
Output sink current	$I_{(OT\_SINK)}$	V_{OT}=0.3V	5	12		mA
Output leakage current	$I_{lkg(OT)}$	V_{OT}=V_{CC}		1		μA

10.Typical Characteristic

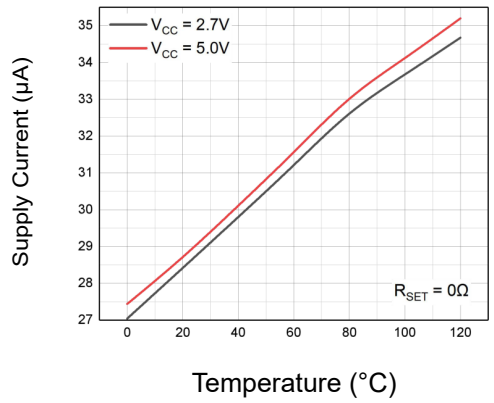


Figure 1: Supply Current vs Temperature

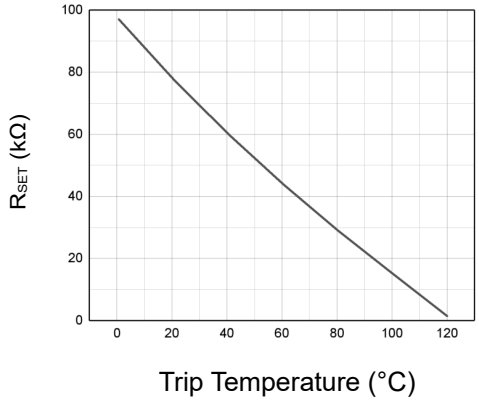


Figure 2: Rset vs Trip Temperature

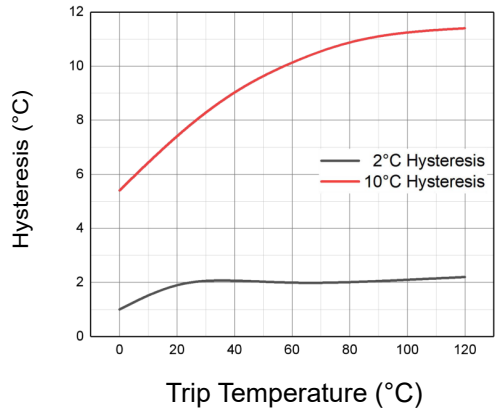


Figure 3: Hysteresis vs. Trip Temperature

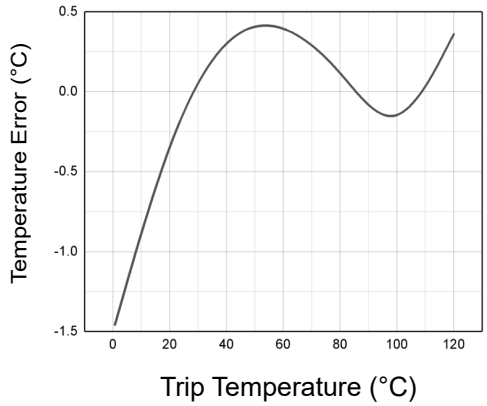


Figure 4: Temperature Error vs Trip Temperature

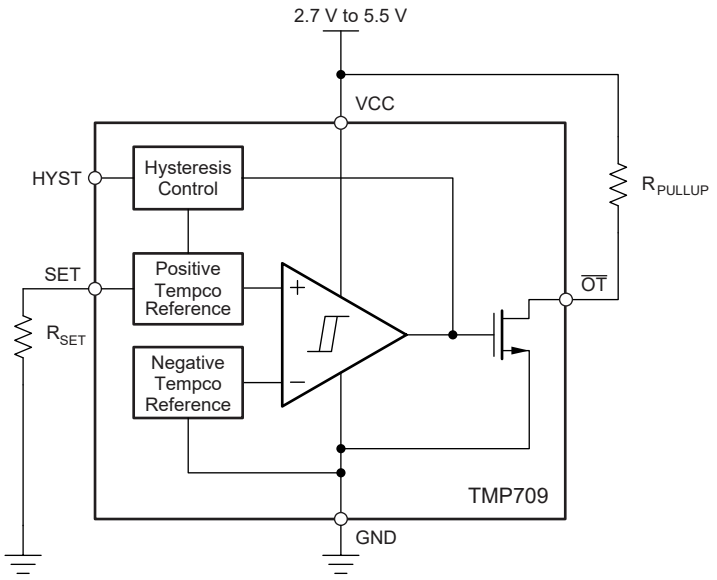
11.Detailed Description

11.1 Overview

The TMP709 is a fully-integrated, resistor-programmable temperature switch that incorporates two temperature dependent voltage references and one comparator. One voltage reference exhibits a positive temperature coefficient (tempco), and the other voltage reference exhibits a negative tempco. The temperature at which both voltage references are equal determines the temperature trip point.

The Functional Block Diagram shows the comparator, the NFET open-drain device connected to the $\overline{OT}$ pin, the positive tempco reference using the external R_{SET} resistor, the negative tempco reference, and the hysteresis control. The voltage of the positive tempco reference is controlled by external resistor RSET.

11.2 Functional Block Diagram



11.3 Feature Description

11.3.1 Temperature Switch

The TMP709 temperature threshold is programmable from 0°C to 125°C and is set by an external 1% resistor from the SET pin to the GND pin. The TMP709 has an open-drain, active-low output structure that easily interfaces with a microprocessor.

The TMP709 reaches the temperature trip point when the voltage from the positive tempco reference exceeds the voltage from the negative tempco reference. This difference causes the output of the comparator to switch from logic 0 to logic 1. The comparator output drives the gate of the NFET open-drain device, and pulls the voltage on the $\overline{OT}$ pin from logic 1 to logic 0 under these conditions; in other words, the output trips. Furthermore, the logic 1 output from the comparator causes the hysteresis control to increase the voltage of the positive tempco reference by an amount set by the logic setting on the HYST pin (10°C for logic 1 on the HYST pin; 2°C for logic 0 on the HYST pin). Increase the voltage of the positive tempco reference after the TMP709 trips to stop the TMP709 from untripping (voltage on the $\overline{OT}$ pin changing from logic 0 to logic 1) until the local temperature reduces by the amount set by the HYST pin. After the local temperature reduces, and the voltage from the positive tempco reference is less than the voltage from the negative tempco reference, the output of the comparator switches from logic 1 to logic 0. This condition causes the voltage on the $\overline{OT}$ pin to change from logic 0 to logic 1 (device untrips).

11.3.2 Hysteresis Input

The HYST pin is a digital input that allows the input hysteresis to be set at either 10°C (when HYST = VCC) or 2°C (when HYST = GND). The hysteresis function keeps the $\overline{OT}$ pin from oscillating when the temperature is near the threshold. Thus, always connect the HYST pin to either VCC or GND. Other input voltages on this pin can cause abnormal supply currents or a device malfunction.

11.3.3 Set-Point Resistor (RSET)

Set the temperature threshold by connecting RSET from the SET pin to GND. The value of RSET is determined using either Figure 2 or Equation 1:

$RSET\ (k\Omega) = 0.0012T^2 - 0.9308T + 96.147$

where

* T = temperature threshold in degrees Celsius.

11.4 Device Functional Modes

The TMP709 device has a single functional mode. Normal operation for the TMP709 device occurs when the power-supply voltage applied across the VCC and GND pins is within the specified operating range of 2.7V to 5.5V.

12.Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

12.1 Application Information

The TMP709 device is simple to configure. The only external components that the device requires are a bypass capacitor and pullup resistor. Power-supply bypassing is strongly recommended. Use a 0.1-µF capacitor placed as close as possible to the VCC supply pin. To minimize the internal power dissipation of the TMP709 family of devices, use a pullup resistor value greater than 10 kΩ from the $\overline{OT}$ pin to the VCC pin. See the Hysteresis Input section for hysteresis configuration, and the Set-Point Resistor (R_{SET}) section for configuring the temperature threshold.

12.2 Typical Application

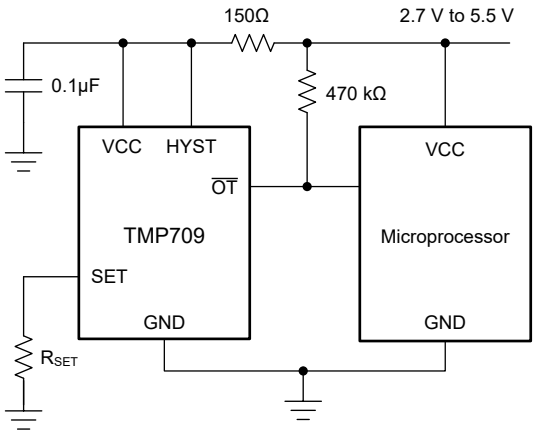


Figure 5. Overtemperature Protection for a 60°C Trip Point

12.2.1 Design Requirements

For this design example, a 2.7-V to 5.5-V power supply, 60°C trip point, and 10°C hysteresis are used.

12.2.2 Detailed Design Procedure

Connect the HYST pin to VCC for 10°C hysteresis. For a 60°C temperature threshold, see the Set-Point Resistor (R_{SET}) section to compute an ideal RSET resistor value of 44.619 kΩ. Select the closest standard value resistor available; in this case, 44.2 kΩ. Use a 10-kΩ pullup resistor from the $\overline{OT}$ pin to the VCC pin. To minimize power, a larger-value pullup resistor can be used, but must not exceed 470 kΩ. Place a 0.1-µF bypass capacitor close to the TMP709 device in order to reduce noise coupled from the power supply.

12.2.3 Application Curves

Figure 6 shows an example of the hysteresis feature. The HYST pin is connected to VCC, so the TMP709 device is configured for 10°C of hysteresis. The device is configured for a 60°C trip temperature by the RSET resistor value; therefore, the $\overline{OT}$ output asserts low when the 60°C threshold is exceeded. The $\overline{OT}$ output remains asserted low until the sensor reaches 50°C

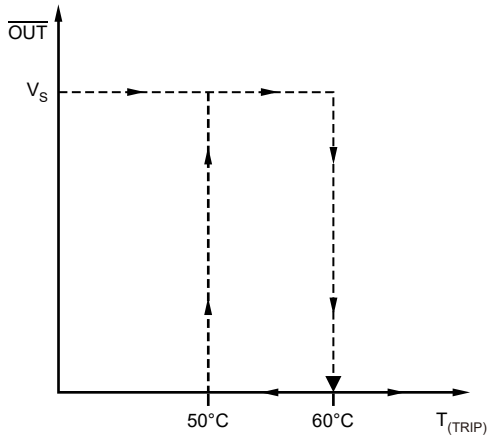


Figure 6. TMP709 Hysteresis Function

13.Power Supply Recommendations

The TMP709 low supply current and supply range allow this device to be powered from many sources. Any significant noise on the VCC pin can result in a trip-point error. Minimize this noise by low-pass filtering the device supply (VCC) using a 150-Ω resistor and a 0.1-µF capacitor.

14.Layout

14.1 Layout Guidelines

The TMP709 is extremely simple to lay out. Figure 7 shows the recommended board layout.

14.2 Layout Example

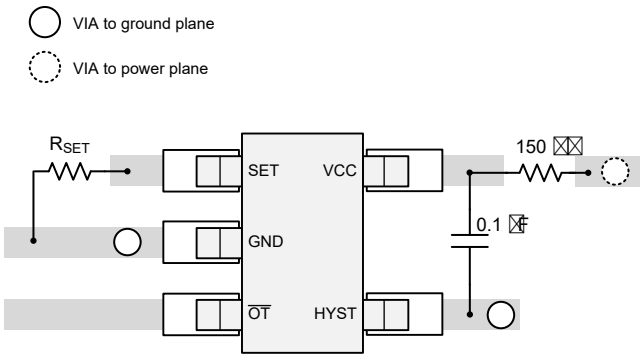


Figure 7. Recommended Layout

14.3 Thermal Considerations

The TMP709 quiescent current is typically 40 µA. The device dissipates negligible power when the output drives a high-impedance load. Thus, the die temperature is the same as the package temperature. In order to maintain accurate temperature monitoring, provide a good thermal contact between the TMP709 package and the device being monitored. The rise in die temperature as a result of self-heating is given by Equation 2:

$\Delta T_J = P_{DISS} \times \theta_{JA}$

where

• P_{DISS} = power dissipated by the device.

• θ_{JA} = package thermal resistance. Typical thermal resistance for SOT-23 package is 217.9°C/W. (2)

To limit the effects of self-heating, keep the output current at a minimum level.

15.Device and Documentation Support

15.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

15.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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15.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

15.5 Glossary

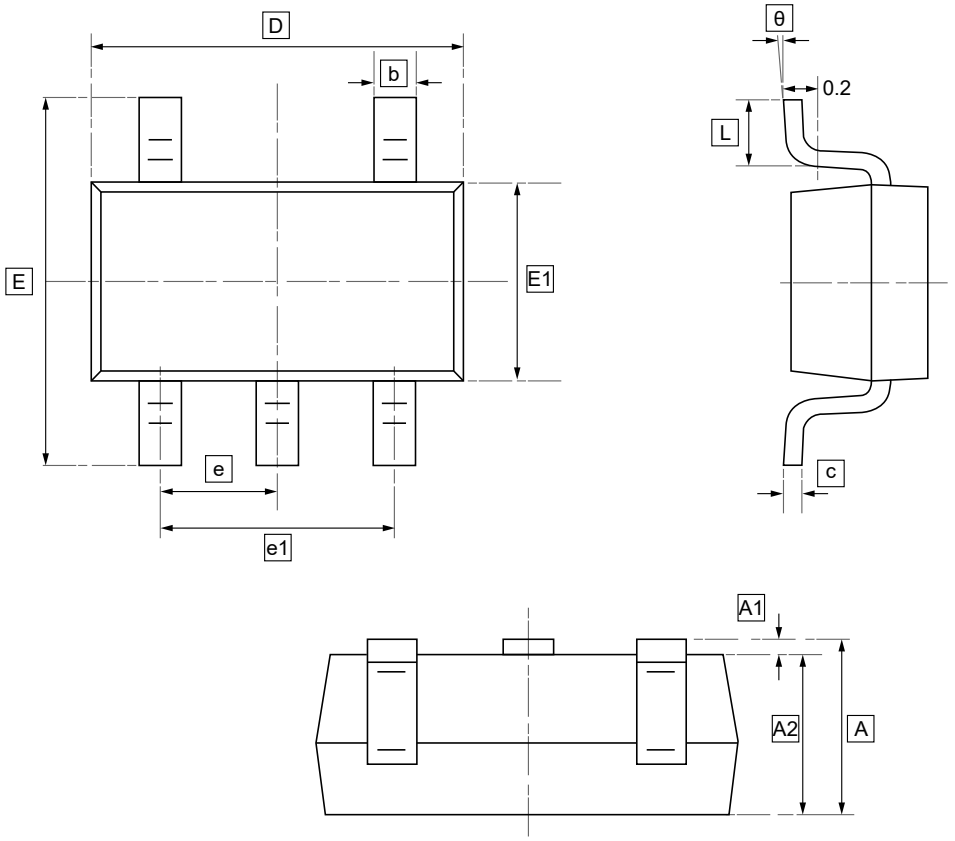
SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

16.Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

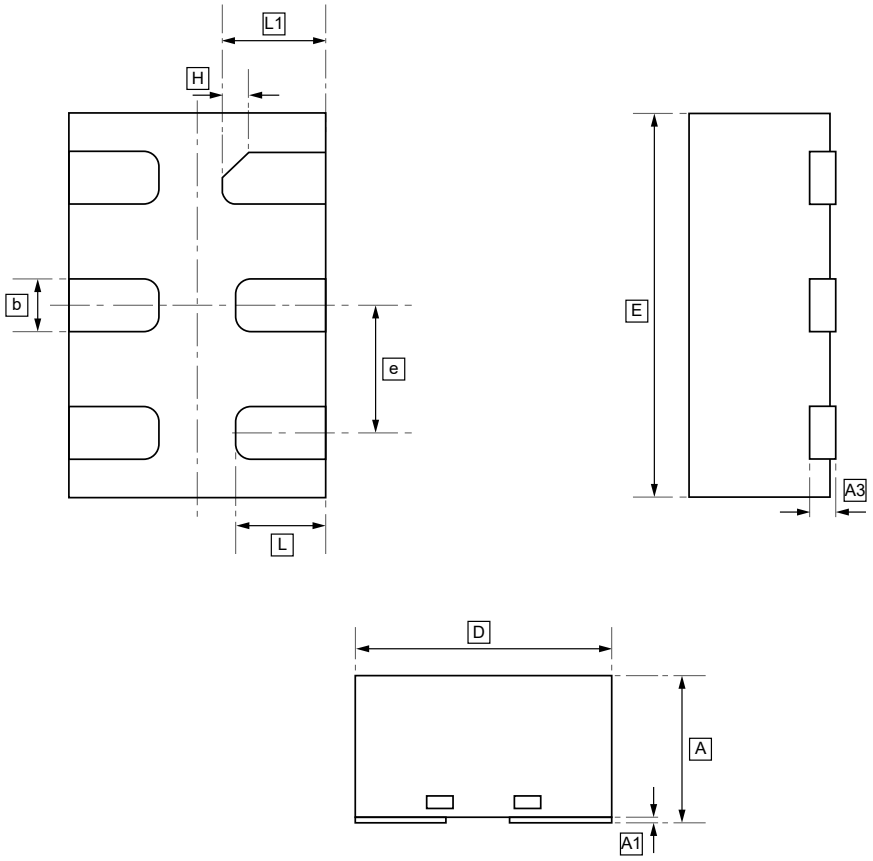
11.1 SOT-23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

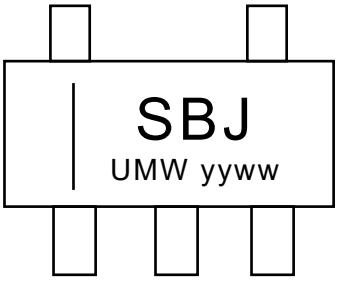
11.2 DFN6(1x1.5) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A3	b	D	E	e	H	L	L1
Min	0.50	0	0.10	0.15	0.90	1.40	0.40	0.10	0.30	0.35
Max	0.60	0.05	REF	0.25	1.10	1.60	0.60	REF	0.40	0.45

12.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW TMP709AIDBVR	SBJ	SOT23-5	3000	Tape and reel
UMW TMP709D	SBJ	DFN6	5000	Tape and reel

13.Disclaimer

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