

1.Description

STP4925 is the dual P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

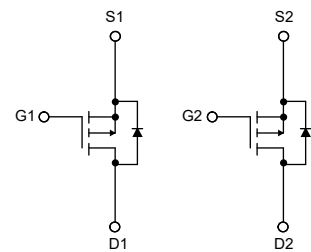
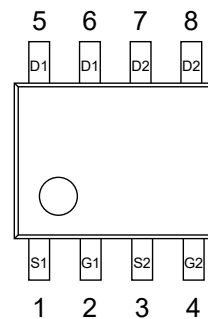
2.Features

- $V_{DS(V)} = -30V$
- $I_D = -7.2A$
- $R_{DS(ON)} < 25m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 32m\Omega (V_{GS} = -4.5V)$

3.Pinning information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8



4.Absolute Maximum Ratings $T_A = 25^\circ C$

Parameter		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ C$)	$T_A = 25^\circ C$	I_D	-7.2	A
	$T_A = 70^\circ C$		-5.6	
Pulsed Drain Current		I_{DM}	-50	
Continuous Source Current (Diode Conduction)		I_S	-2.3	
Power Dissipation	$T_A = 25^\circ C$	P_D	2.8	W
	$T_A = 70^\circ C$		1.8	W
Junction Temperature		T_J	-55 to 150	$^\circ C$
Storage Temperature Range		T_{STG}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	70	$^\circ C/W$

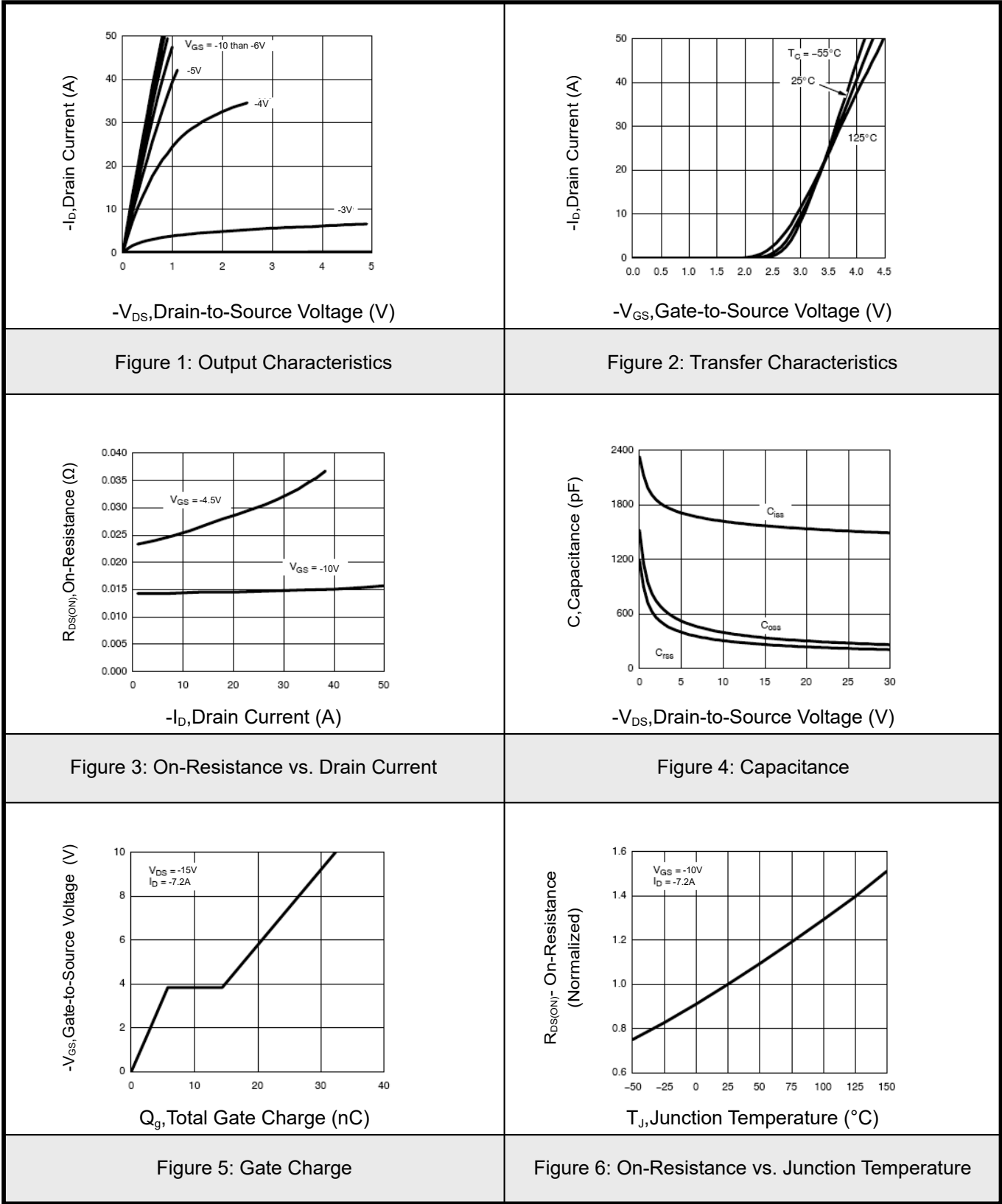


5. $T_A=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-3	V
Gate-source leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$			-1	μA
		$V_{DS}=-30V, V_{GS}=0V, T_J=55^{\circ}\text{C}$			-5	μA
Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-7.2A$		21	25	m Ω
		$V_{GS}=-4.5V, I_D=-5.6A$		29	32	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-10V, I_D=-5.6A$		24		S
Diode Forward Voltage	V_{SD}	$I_S=-2.3A, V_{GS}=0V$		-0.8	-1	V
Dynamic						
Total gate charge	Q_g	$V_{DS}=-15V, V_{GS}=-10V, I_D=-5.6A$		16	24	nC
Gate-Source Charge	Q_{gs}			2.3		nC
Gate-Drain Charge	Q_{gd}			4.5		nC
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$		1650		pF
Output Capacitance	C_{oss}			350		pF
Reverse Transfer Capacitance	C_{rss}			235		pF
Turn-On Time	$t_{D(on)}$	$V_{DS}=-15V, R_L=15\Omega$		16	30	nS
	t_r			17	30	nS
Turn-Off Time	$t_{D(off)}$	$I_D=-1A, V_{GEN}=-10V, R_G=6\Omega$		65	110	nS
	t_f			35	80	nS



6.1 Typical Characteristics



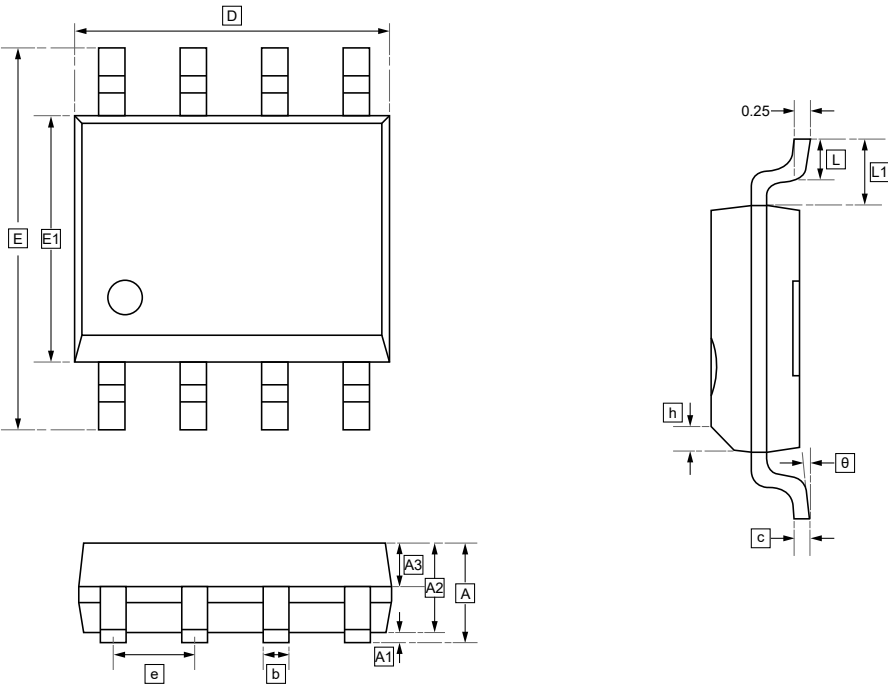


6.2Typical Characterisitics

Figure 7: Source-Drain Diode Forward Voltage	Figure 8: On-Resistance vs. Gate-to-Source Voltage
Figure 9: Threshold Voltage	Figure 10: Single Pulse Power
Figure 11: Normalized Thermal Transient Impedance, Junction-to-Ambient	



7.SOP-8 Package Outline Dimensions



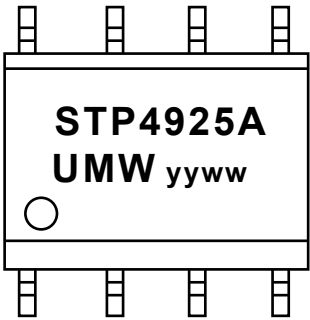
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW STP4925A	SOP-8	3000	Tape and reel



9.Disclaimer

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