

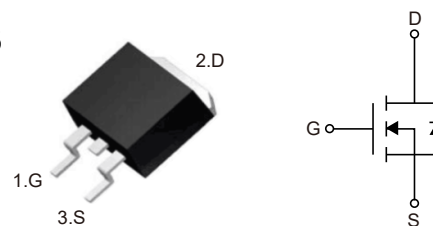
1.Features

- $V_{DS(V)}=40V$
- $I_D=120A$
- $R_{DS(ON)}<1.5m\Omega(V_{GS}=10V)$
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{(ON)}$ product (FOM)
- Very low on-resistance $R_{DS(ON)}$

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-263



3.Absolute Maximum Ratings $T_J=25^{\circ}C$

Parameter	Symbol	Conditions	Rating	Units
Continuous drain current	I_D	$V_{GS}=10V, T_C=25^{\circ}C$	120	A
		$V_{GS}=10V, T_C=100^{\circ}C$	120	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25^{\circ}C$	400	
Avalanche current, single pulse ³⁾	I_{AS}	$T_C=25^{\circ}C$	100	
Avalanche energy, single pulse	E_{AS}	$I_D=100A, R_{GS}=25\Omega$	865	mJ
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25^{\circ}C$	250	W
storage temperature	T_J, T_{STG}		-55 to 175	$^{\circ}C$
IEC climatic category; DIN IEC 68-1			55/175/56	



4. Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal resistance, junction -case	R _{thJC}				0.6	K/W
SMD version, device on PCB	R _{thJA}	minimal footprint			62	K/W
		6 cm ² cooling area ⁴⁾			40	K/W
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =1mA	40			V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =200μA	2		4	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =40V, V _{GS} =0V, T _J =25°C		0.1	2	μA
		V _{DS} =40V, V _{GS} =0V, T _J =125°C		20	200	μA
Gate-source leakage current	I _{GSS}	V _{GS} =20V, V _{DS} =0V		10	100	nA
Drain-source on-state resistance ⁵⁾	R _{DS(ON)}	V _{GS} =10V, I _D =100A		1.2	1.5	mΩ
Gate resistance	R _G			1.5		Ω
Transconductance	g _{FS}	V _{DS} >2 I _D R _{DS(ON)max} , I _D =100 A	120	230		S
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =20V, f=1MHz		15000	20000	pF
Output capacitance	C _{oss}			4000	5300	pF
Reverse transfer capacitance	C _{rss}			160		pF
Turn-on delay time	t _{D(on)}	V _{DD} =20V, V _{GS} =10V I _D =30A, R _G =1.6Ω		40		ns
Rise time	t _r			10		ns
Turn-off delay time	t _{D(off)}			64		ns
Fall time	t _f			13		ns
Gate to source charge	Q _{gs}	V _{DD} =20V, I _D =100A V _{GS} =0 to 10V		76		nC
Gate charge at threshold	Q _{g(th)}			46		nC
Gate to drain charge	Q _{gd}			23		nC
Switching charge	Q _{SW}			75		nC
Gate charge total	Q _g			188	250	nC
Gate plateau voltage	V _{plateau}			5		V



Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1V, V_{GS}=0 \text{ to } 10V$		177		nC
Output charge	Q_{oss}	$V_{DD}=20V, V_{GS}=0V$		147		nC
Diode continuous forward current	I_S	$T_C=25^{\circ}C$			120	A
Diode pulse current	$I_{S,pulse}$				400	A
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=100A, T_J=25^{\circ}C$		0.88	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15V, I_F=I_S, di_F/dt=400A/\mu s$		141		nC

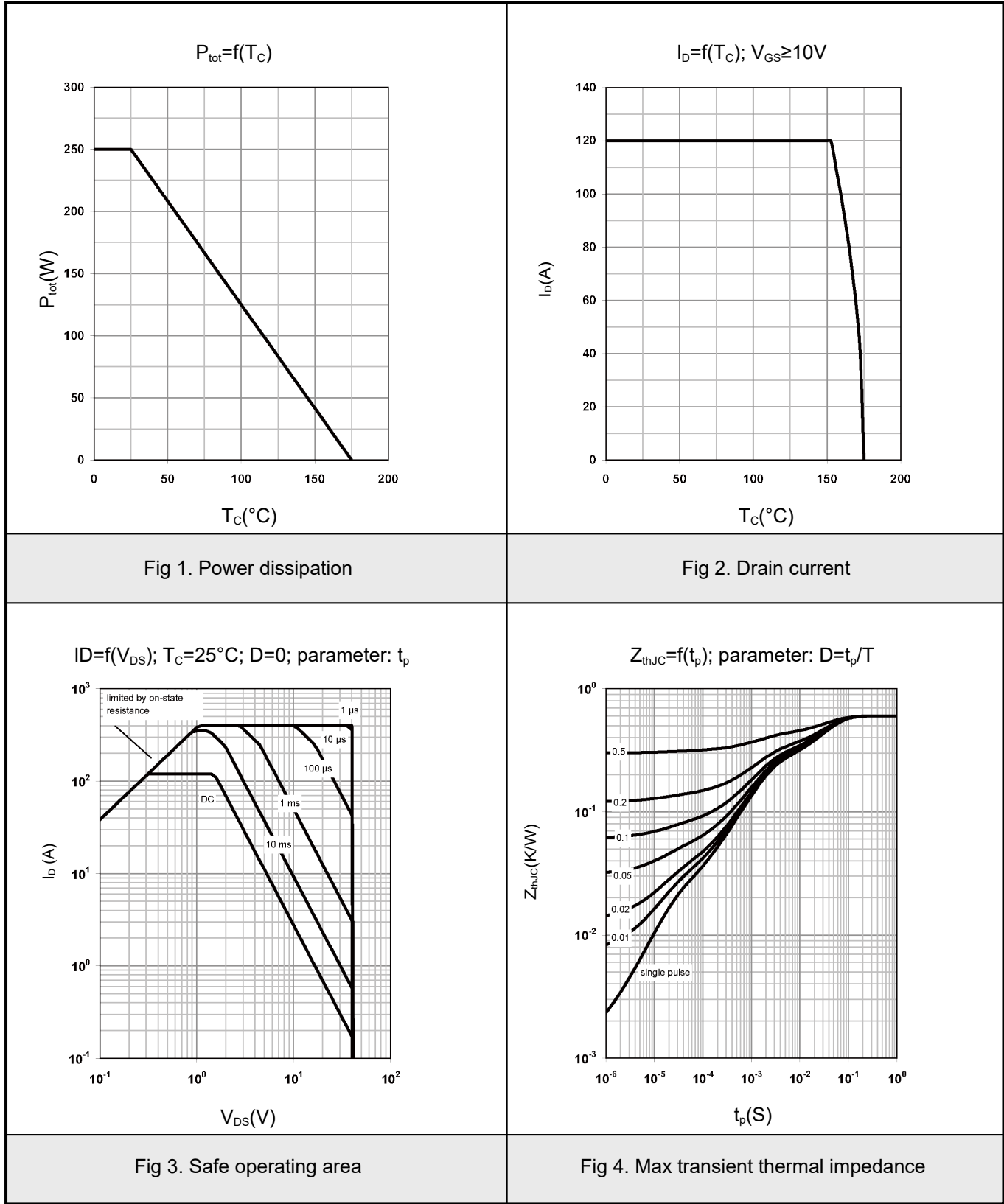
Notes:

Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer , 70 um thick) copper area for drainconnection .

PCB is vertical in still air. Measured from drain tab to source pin

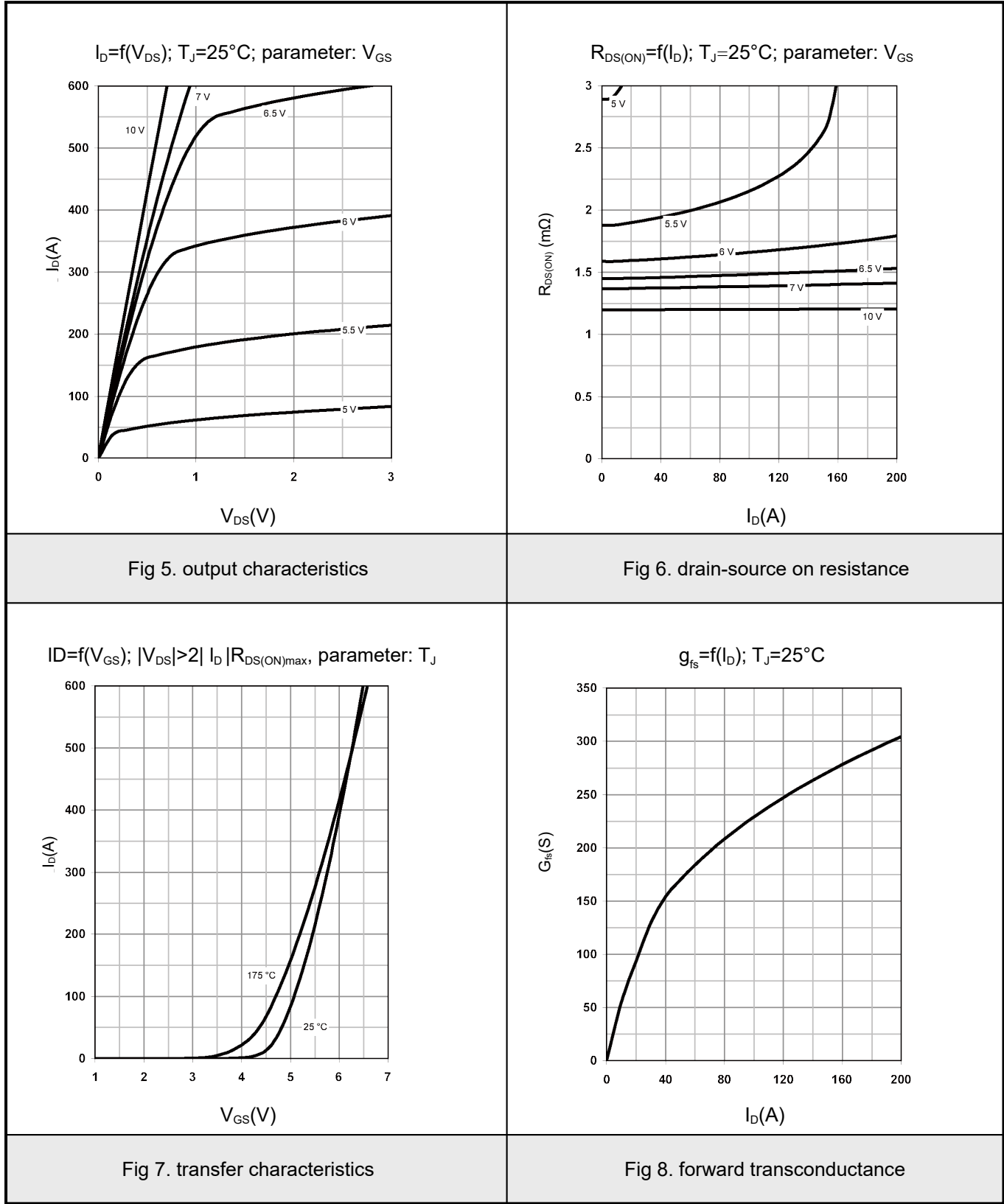


5.1Typical characteristic



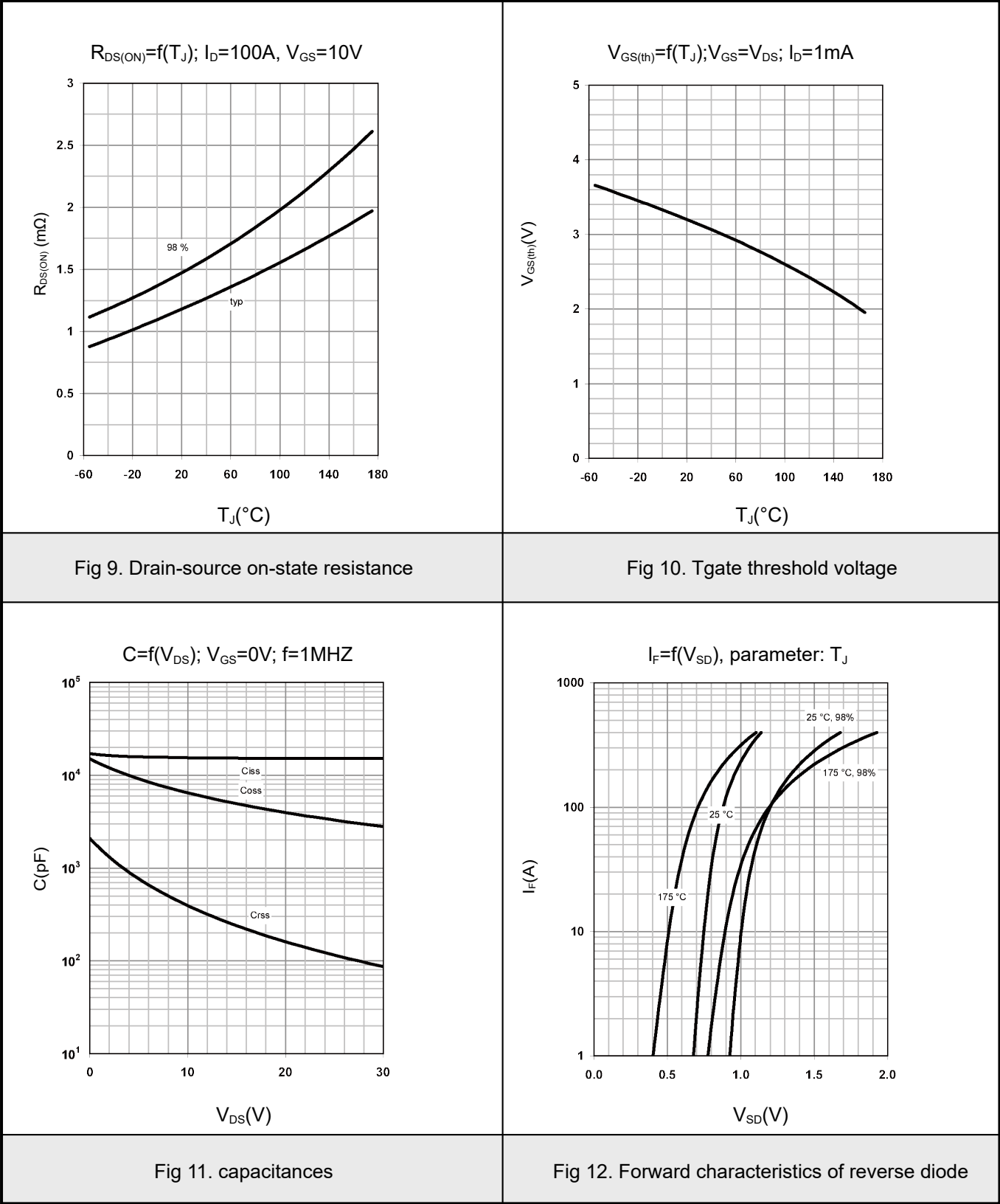


5.2Typical characteristic



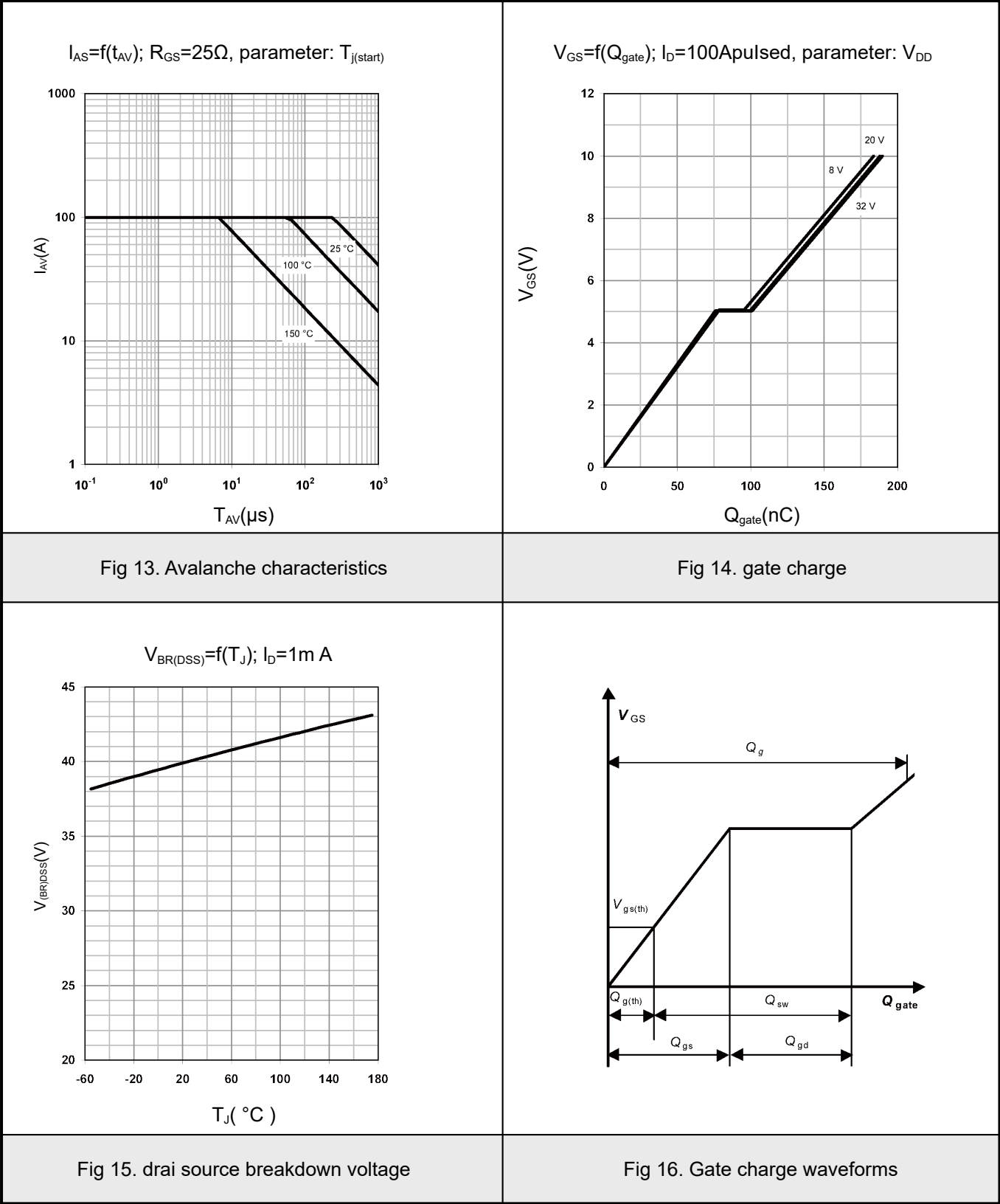


5.3Typical characteristic



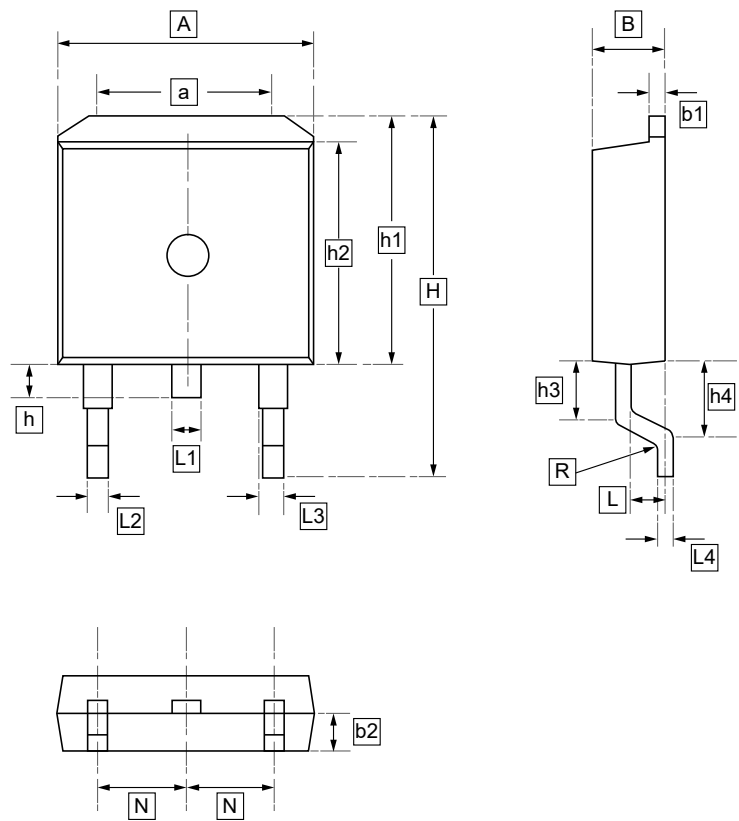


5.4Typical characteristic





8.TO-263 Package Outline Dimensions



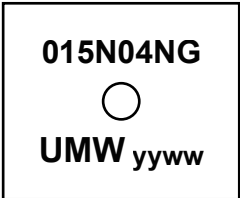
DIMENSIONS (mm are the original dimensions)

Symbol	A	a	B	b1	b2	H	h	h1	h2	h3	h4	L	L1	L2	L3
Min	9.6	7.2	4.3	1.25	2.2	15.2	1.34	10.3	9.1	1.34	2.5	2.2	1.2	0.7	1.2
Max	10.0	7.6	4.7	1.35	2.6	15.8	1.74	10.7	9.3	1.74	2.9	2.6	1.4	0.9	1.4

Symbol	L4	N	R
Min	0.4	2.4	0.45
Max	0.6	2.5	0.55



7.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IPB015N04NG	TO-263	800	Tape and reel



8.Disclaimer

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