UMW AO4411

30V P-Channel MOSFET

1.Description

The AO4411 uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge. This device is suitable for use as a load switch or in PWM applications.

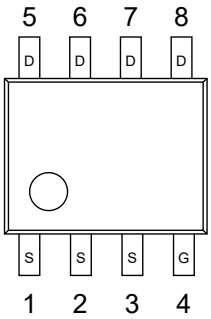
2.Features

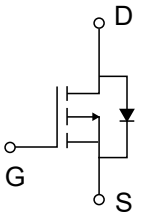
- V_{DS}=-30V
- I_D=-8A
- $R_{DS(ON)}$ (V_{GS}=-10V) <25mΩ
- $R_{DS(ON)}$ (V_{GS}=-4.5V) <55mΩ

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[A]	T_A=25°C	I_D	-8	A
	T_A=70°C		-6.6	
Pulsed Drain Current [B]		I_{DM}	-40	
Power Dissipation [A]	T_A=25°C	P_D	3	W
	T_A=70°C		2.1	
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	24	40	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		54	75	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	21	30	°C/W

6.Electrical Characteristics T_A=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250μA, V_{GS}=0V	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.2	-2	-2.4	V
On state drain current	$I_{D(ON)}$	V_{GS}=-10V, V_{DS}=-5V	-40			A
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-8A		15	25	mΩ
		V_{GS}=-4.5V, I_D=-5A		25	55	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-8A		14.5		S
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V		-0.76	-1	V
Maximum Body-Diode Continuous Current [G]	I_S				-4.2	A
DYNAMIC PARAMETERS						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, f=1MHz		920	1120	pF
Output Capacitance	C_{oss}			190		pF
Reverse Transfer Capacitance	C_{rss}			122		pF
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz		3.6	5	Ω
SWITCHING PARAMETERS						
Total Gate Charge(10V)	Q_g(10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-8A		18.4	23	nC
Total Gate Charge(4.5V)	Q_g(4.5V)			9.3	11.5	nC
Gate Source Charge	Q_{gs}			2.7		nC
Gate Drain Charge	Q_{gd}			4.9		nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V, R_L=1.8Ω,R_{GEN}=3Ω		7.1		ns
Turn-On Rise Time	t_r			3.4		ns
Turn-Off DelayTime	$t_{D(off)}$			18.9		ns
Turn-Off Fall Time	t_f			8.4		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F=-8A, dI/dt=100A/μs		21.5	27	ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=-8A, dI/dt=100A/μs		12.5		nC

7.1Typical characteristic

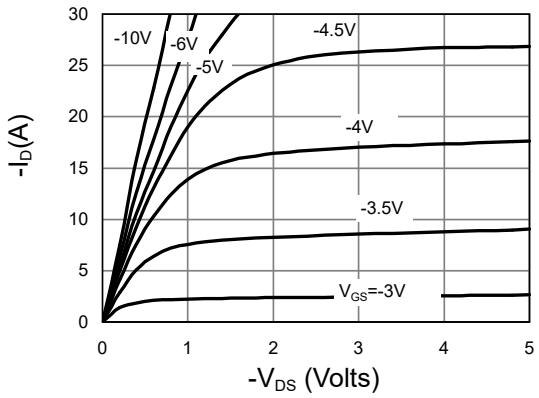


Fig 1: On-Region Characteristics

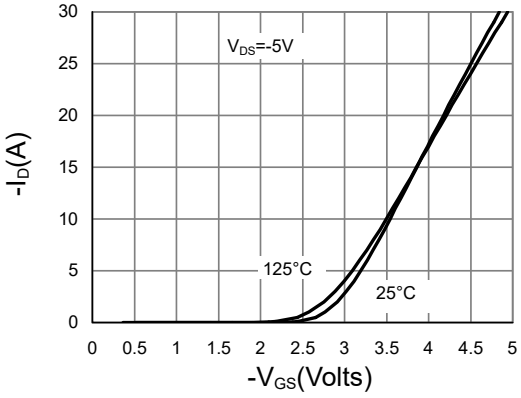


Figure 2: Transfer Characteristics

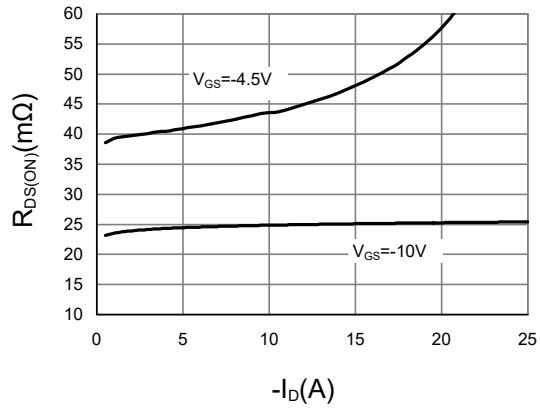


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

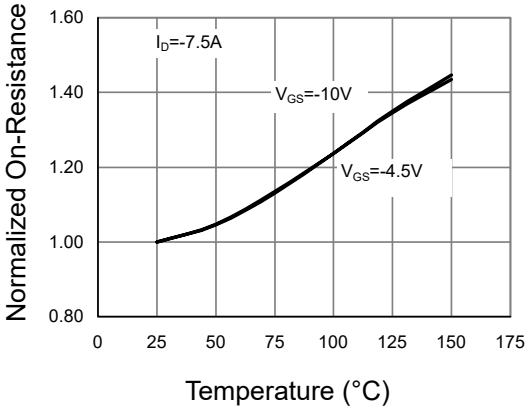


Figure 4: On-Resistance vs. Junction Temperature

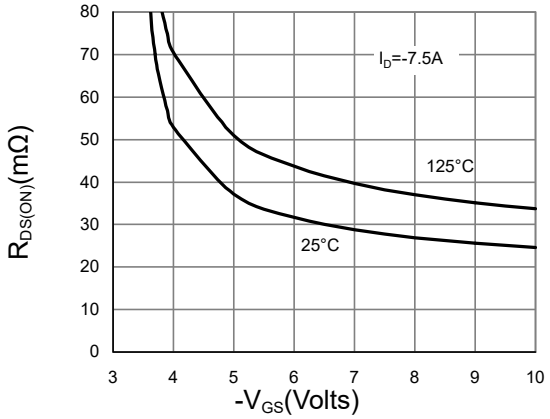


Figure 5: On-Resistance vs. Gate-Source Voltage

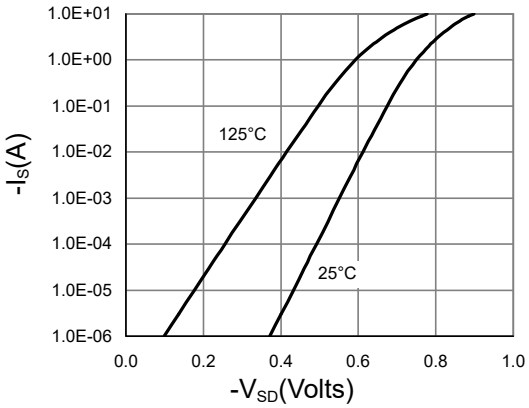


Figure 6: Body-Diode Characteristics

7.2Typical Characterisitics

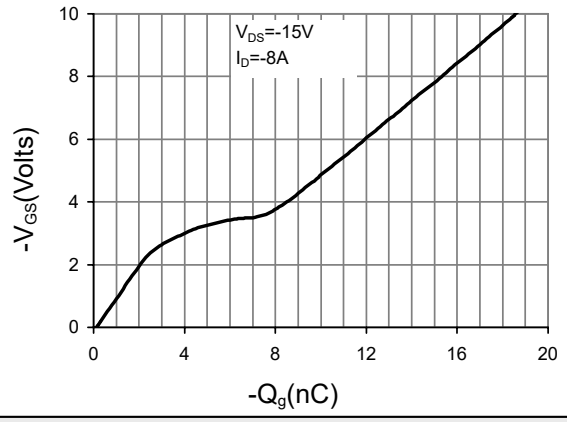


Figure 7: Gate-Charge Characteristics

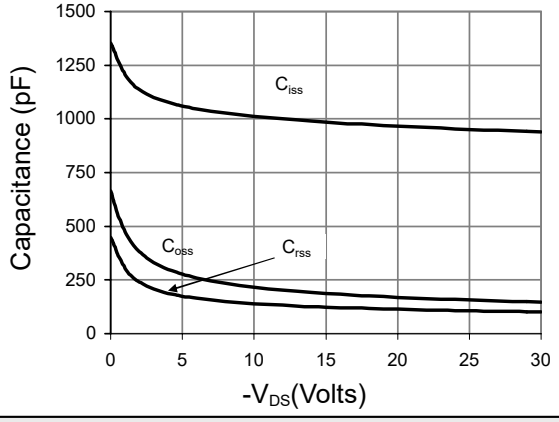


Figure 8: Capacitance Characteristics

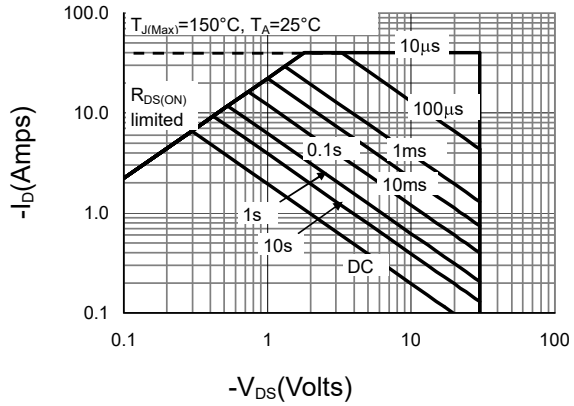


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

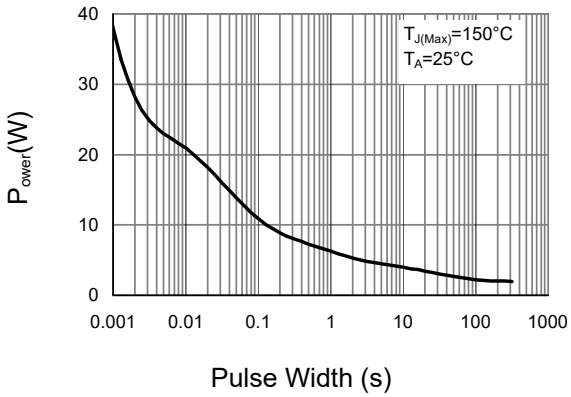


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

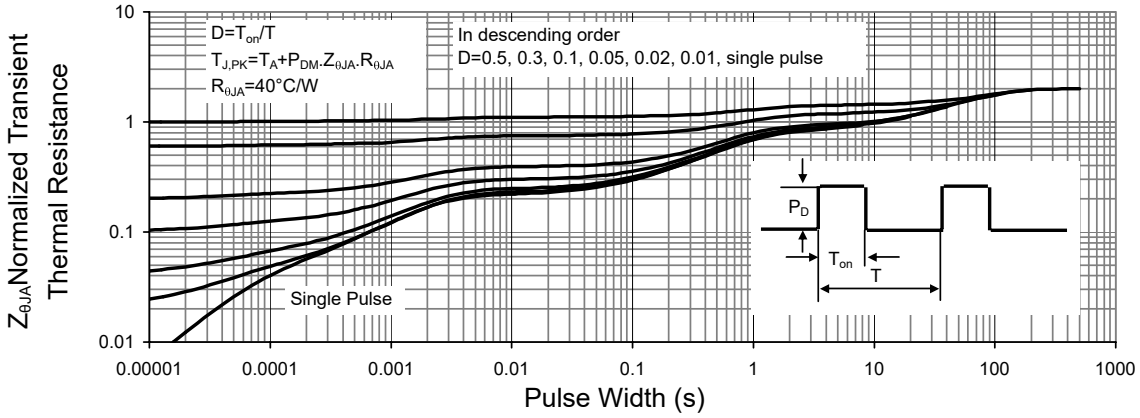
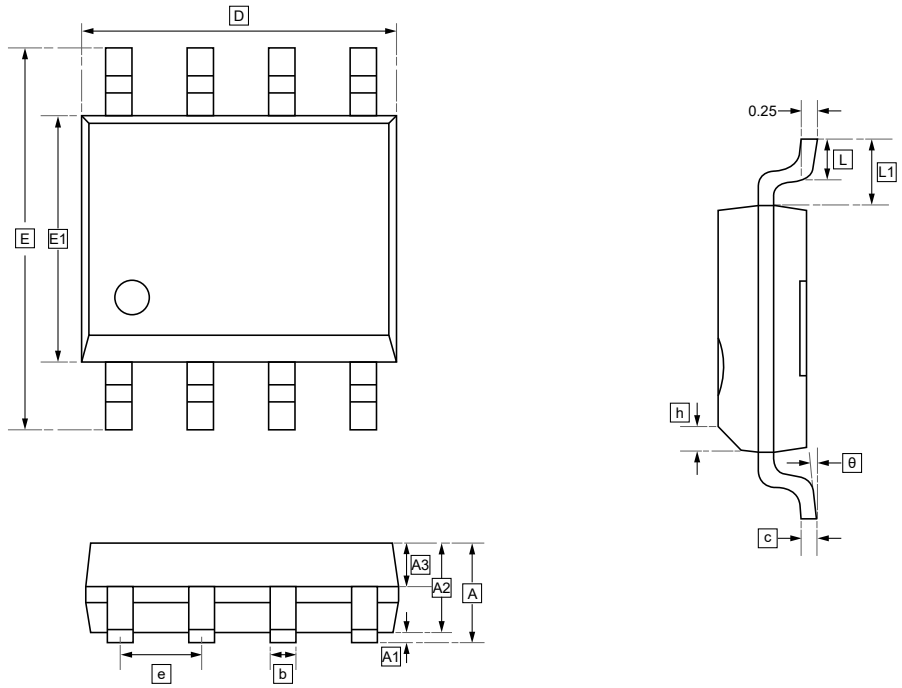


Figure 11: Normalized Maximum Transient Thermal Impedance

8.SOP-8 Package Outline Dimensions

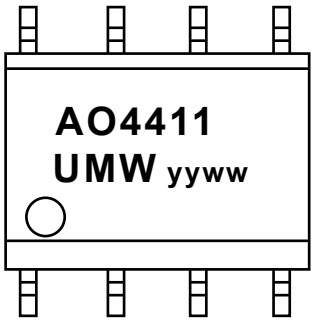


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO4411	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

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A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.