UMW TSZ121/122

Very high accuracy (5μV) zero drift micropower 5V operational amplifiers

1.Description

The TSZ121/122 of high precision operational amplifiers offer very low input offset voltages with virtually zero drift.TSZ121 is the single version, TSZ122 the dual version, with pinouts compatible with industry standards.The TSZ121/122 offers rail-to rail input and output, excellent speed/ power consumption ratio, and 400kHz gain bandwidth product, while consuming less than 40μA at 5V. The devices also feature an ultra-low input bias current.These features make theTSZ121/122 family ideal for sensor interfaces, battery-powered applications and portable applications.

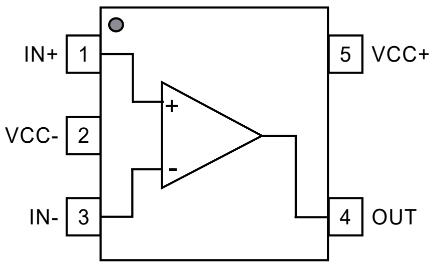
2.Features

- Very high accuracy and stability: offset voltage 5μV max at 25°C, 8μV over full temperature range (-40°C to 125°C)
- Rail-to-rail input and output
- Low supply voltage: 1.8 - 5.5V
- Low power consumption: 40μA max. at 5V
- Gain bandwidth product: 400kHz
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 to 125°C

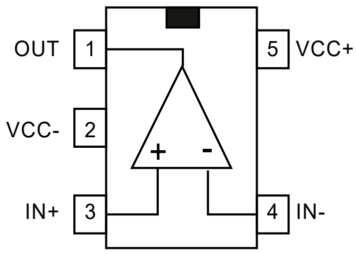
3.Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Medical instrumentation

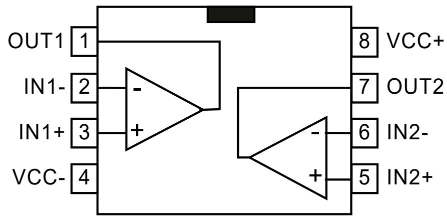
4.Pinning information



SC70-5



SOT23-5



SOP-8

5.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Supply voltage (1)		V_{CC}	6	V
Differential input voltage (2)		V_{id}	$\pm V_{CC}$	V
Input voltage (3)		V_{in}	(V_{CC-})-0.2 to (V_{CC+})+0.2	V
Input current (4)		I_{in}	10	mA
Storage temperature		T_{STG}	-65 to 150	°C
Maximum junction temperature		T_J	-65 to 150	°C
Thermal resistance junction to ambient (5)(6)	SC70-5	R_{thja}	205	°C/W
	SOT23-5		250	°C/W
	SOP-8		125	°C/W
HBM: human body model (7)		ESD	4	kV
MM: machine model (8)			300	V
CDM: charged device model (9)			1.5	kV
Latch-up immunity			200	mA

Notes:

1. All voltage values, except the differential voltage are with respect to the network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC} - V_{in} must not exceed 6 V, Vin must not exceed 6V
4. Input current must be limited by a resistor in series with the inputs.
5. R_{th} are typical values.
6. Short-circuits can cause excessive heating and destructive dissipation.
7. Human body model: 100 pF discharged through a 1.5kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

6.Operating conditions

Parameter	Symbol	Value	Units
Supply voltage	V_{CC}	1.8 to 5.5	V
Common mode input voltage range	V_{icm}	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	V
Operating free air temperature range	T_{oper}	-40 to +125	°C

7.1 Electrical Characteristics

V_{CC+}=1.8V with V_{CC-}=0V, V_{icm}=V_{CC}/2, T=25°C, and R_L=10kΩ connected to V_{CC}/2 (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input offset voltage	V_{io}	T=25°C		1	5	μV
		-40°C<T<125°C			8	μV
Input offset voltage drift [1]	$\Delta V_{io}/\Delta T$	-40°C<T<125°C		10	30	nV/°C
Input bias current (V_{out}=V_{CC}/2)	I_{ib}	T=25°C		50	200[2]	pA
		-40°C<T<125°C			300[2]	pA
Input offset current (V_{out}=V_{CC}/2)	I_{io}	T=25°C		100	400[2]	pA
		-40°C<T<125°C			600[2]	pA
Common mode rejection ratio,20 log ($\Delta V_{icm}/\Delta V_{io}$),$V_{ic}$=0V to V_{CC}, V_{out}=V_{CC}/2 R_L>1MΩ	CMR	T=25°C	110	122		dB
		-40°C<T<125°C	110			dB
Large signal voltage gain V_{out}=0.5V to (V_{CC} - 0.5V)	A_{vd}	T=25°C	118	135		dB
		-40°C<T<125°C	110			dB
High-level output voltage (V_{OH}=V_{CC}-V_{OUT})	V_{OH}	T=25°C			30	mV
		-40°C<T<125°C			70	mV
Low-level output voltage	V_{OL}	T=25°C			30	mV
		-40°C<T<125°C			70	mV
I_{sink} (V_{out}=V_{CC})	I_{out}	T=25°C	7	8		mA
		-40°C<T<125°C	6			mA
I_{source} (V_{out}=0V)		T=25°C	5	7		mA
		-40°C<T<125°C	4			mA
Supply current (per amplifier) V_{out}=V_{CC}/2, R_L>1MΩ)	I_{CC}	T=25°C		28	40	μA
		-40°C<T<125°C			40	μA
Gain bandwidth product	GBP	R_L=10kΩ, C_L=100pF		400		kHz
Unity gain frequency	F_u			300		kHz
Phase margin	ϕm			55		Degrees
Gain margin	G_m			17		dB
Slew rate [3]	SR			0.17		V/μs

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Setting time	t_s	To 0.1 %, V_{in}=1V_{p-p}, R_L=10kΩ, C_L=100pF		50		μs
Equivalent input noise voltage	e_n	f=1kHz		60		nV/√Hz
		f=10kHz		60		nV/√Hz
Low-frequency peak-to-peak input noise	$\int e_n$	Bandwidth, f=0.1 to 10Hz		1.1		μVpp
Channel separation	C_s	f=100Hz		120		dB
Initialization time	t_{init}	T=25°C		50		μs
		-40°C<T<125°C		100		μs

7.2 Electrical Characteristics

V_{CC+}=3.3V with V_{CC-}=0V, V_{icm}=V_{CC}/2, T=25°C, and R_L=10kΩ connected to V_{CC}/2 (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input offset voltage	V_{io}	T=25°C		1	5	μV
		-40°C<T<125°C			8	μV
Input offset voltage drift [1]	$\Delta V_{io}/\Delta T$	-40°C<T<125°C		10	30	nV/°C
Input bias current (V_{out}=V_{CC}/2)	I_{ib}	T=25°C		60	200[2]	pA
		-40°C<T<125°C			300[2]	pA
Input offset current (V_{out}=V_{CC}/2)	I_{io}	T=25°C		120	400[2]	pA
		-40°C<T<125°C			600[2]	pA
Common mode rejection ratio,20 log ($\Delta V_{icm}/\Delta V_{io}$),$V_{ic}$=0V to V_{CC}, V_{out}=V_{CC}/2 R_L>1MΩ	CMR	T=25°C	115	128		dB
		-40°C<T<125°C	115			dB
Large signal voltage gain V_{out}=0.5V to (V_{CC} - 0.5V)	A_{vd}	T=25°C	118	135		dB
		-40°C<T<125°C	110			dB
High-level output voltage (V_{OH}=V_{CC}-V_{OUT})	V_{OH}	T=25°C			30	mV
		-40°C<T<125°C			70	mV
Low-level output voltage	V_{OL}	T=25°C			30	mV
		-40°C<T<125°C			70	mV
I_{sink} (V_{out}=V_{CC})	I_{out}	T=25°C	15	18		mA
		-40°C<T<125°C	12			mA
I_{source} (V_{out}=0V)		T=25°C	14	16		mA
		-40°C<T<125°C	10			mA
Supply current (per amplifier) V_{out}=V_{CC}/2, R_L>1MΩ)	I_{CC}	T=25°C		29	40	μA
		-40°C<T<125°C			40	μA
Gain bandwidth product	GBP	R_L=10kΩ, C_L=100pF		400		kHz
Unity gain frequency	F_u			300		kHz
Phase margin	ϕm			56		Degrees
Gain margin	G_m			19		dB
Slew rate [3]	SR			0.19		V/μs

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Setting time	t_s	To 0.1 %, V_{in}=1V_{p-p}, R_L=10kΩ, C_L=100pF		50		μs
Equivalent input noise voltage	e_n	f=1kHz		40		nV/√Hz
		f=10kHz		40		nV/√Hz
Low-frequency peak-to-peak input noise	$\int e_n$	Bandwidth, f=0.1 to 10Hz		0.8		μVpp
Channel separation	C_s	f=100Hz		120		dB
Initialization time	t_{init}	T=25°C		50		μs
		-40°C<T<125°C		100		μs

7.3 Electrical Characteristics

V_{CC+}=5V with V_{CC-}=0V, V_{icm}=V_{CC}/2, T=25°C, and R_L=10kΩ connected to V_{CC}/2 (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input offset voltage	V_{io}	T=25°C		1	5	μV
		-40°C<T<125°C			8	μV
Input offset voltage drift (1)	$\Delta V_{io}/\Delta T$	-40°C<T<125°C		10	30	nV/°C
Input bias current (V_{out}=V_{CC}/2)	I_{ib}	T=25°C		70	200(2)	pA
		-40°C<T<125°C			300(2)	pA
Input offset current (V_{out}=V_{CC}/2)	I_{io}	T=25°C		140	400(2)	pA
		-40°C<T<125°C			600(2)	pA
Common mode rejection ratio,20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{ic}=0V to V_{CC} V_{out}=V_{CC}/2, R_L>1MΩ	CMR	T=25°C	115	136		dB
		-40°C<T<125°C	115			dB
Supply voltage rejection ratio, 20 log ($\Delta V_{CC}/\Delta V_{io}$), V_{CC}=1.8V to 5.5V V_{out}=V_{CC}/2, R_L>1MΩ	SVR	T=25°C	120	140		dB
		-40°C<T<125°C	120			dB
Large signal voltage gain V_{out}=0.5V to (V_{CC} - 0.5V)	A_{vd}	T=25°C	120	135		dB
		-40°C<T<125°C	110			dB
EMI rejection rate =-20 log ($V_{RFpeak}/\Delta V_{io}$)	EMIRR(3)	V_{RF}=100mV_p, f=400MHz		84		dB
		V_{RF}=100mV_p, f=900MHz		87		dB
		V_{RF}=100mV_p, f=1800MHz		90		dB
		V_{RF}=100mV_p, f=2400MHz		91		dB
High-level output voltage (V_{OH}=V_{CC}-V_{OUT})	V_{OH}	T=25°C			30	mV
		-40°C<T<125°C			70	mV
Low-level output voltage	V_{OL}	T=25°C			30	mV
		-40°C<T<125°C			70	mV
I_{sink} (V_{out}=V_{CC})	I_{out}	T=25°C	15	18		mA
		-40°C<T<125°C	14			mA
I_{source} (V_{out}=0V)		T=25°C	14	17		mA
		-40°C<T<125°C	12			mA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current (per amplifier V_{out}=V_{CC}/2, R_L>1MΩ)	I_{CC}	T=25°C		31	40	μA
		-40°C<T<125°C			40	μA
Gain bandwidth product	GBP	R_L=10kΩ, C_L=100pF		400		kHz
Unity gain frequency	F_u			300		kHz
Phase margin	ϕm			53		Degrees
Gain margin	G_m	R_L=10kΩ, C_L=100pF		19		dB
Slew rate (4)	SR			0.19		V/μs
Setting time	t_s	To 0.1 %,V_{in}=1V_{p-p},R_L=10kΩ,C_L=100pF		10		μs
Equivalent input noise voltage	e_n	f=1kHz		37		nV/√Hz
		f=10kHz		37		nV/√Hz
Low-frequency peak-to-peak input noise	$\int e_n$	Bandwidth, f=0.1 to 10Hz		0.75		μVpp
Channel separation	C_s	f=100Hz		120		dB
Initialization time	t_{init}	T=25°C		50		μs
		-40°C<T<125°C		100		μs

8.1 Typical characteristic

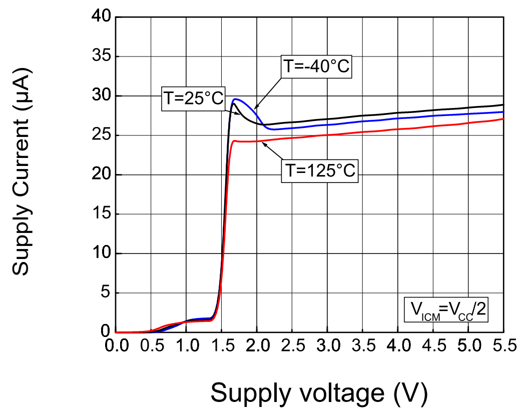


Figure 1: Supply current vs. supply voltage

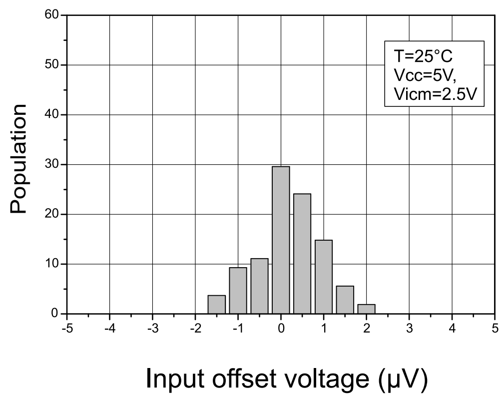


Figure 2: Input offset voltage distribution at V_{CC}=5V

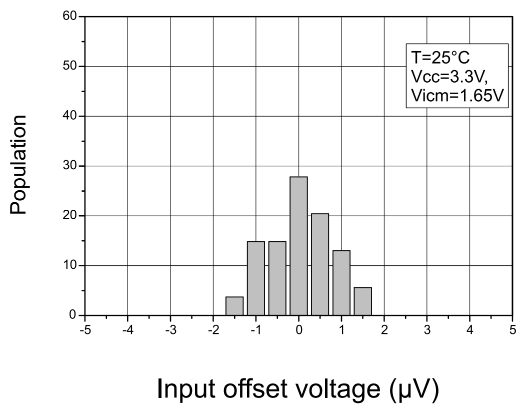


Figure 3: Input offset voltage distribution at V_{CC}=3.3V

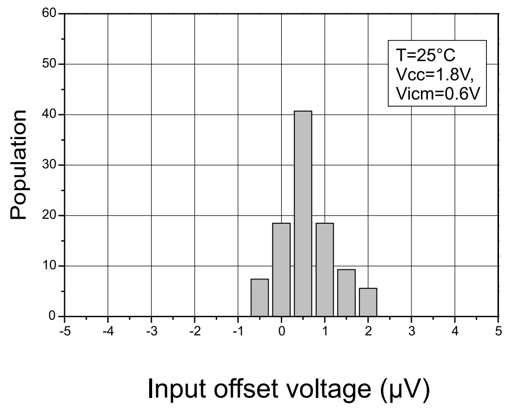


Figure 4: Input offset voltage distribution at V_{CC}=1.8V

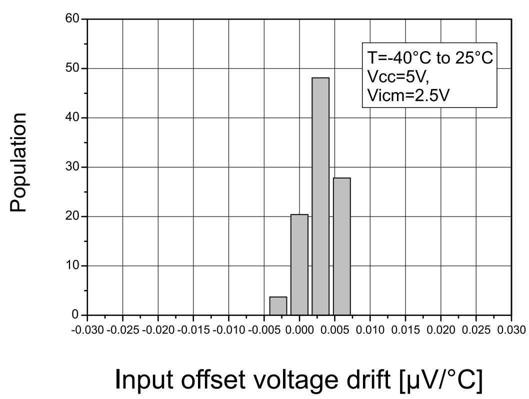


Figure 5: Vio temperature co-efficient distribution (-40 °C to 25 °C)

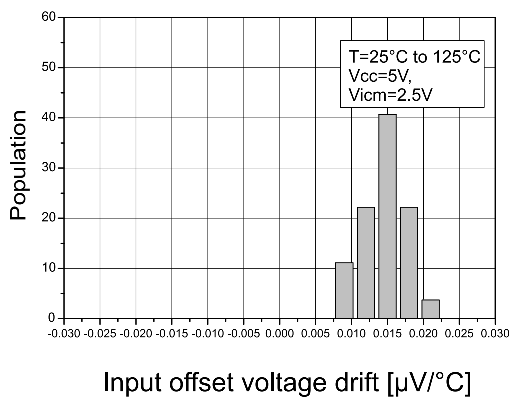


Figure 6: Vio temperature co-efficient distribution (25 °C to 125 °C)

8.2 Typical characteristic

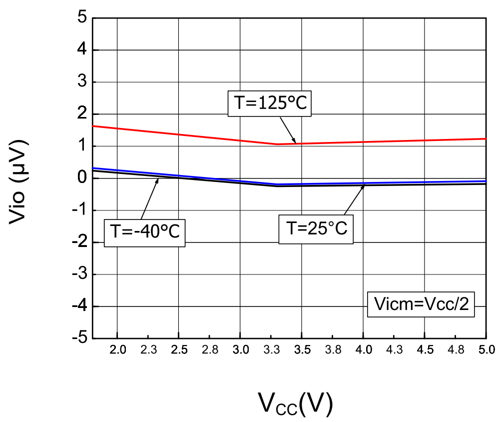


Figure 7: Input offset voltage vs. supply voltage

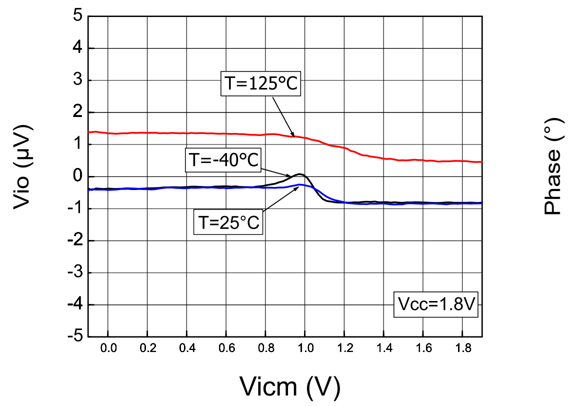


Figure 8: Input offset voltage vs. input common-mode at V_{CC} = 1.8 V

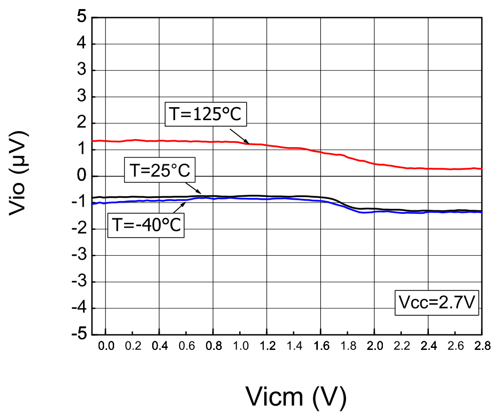


Figure 9: Input offset voltage vs. input common-mode at V_{CC} = 2.7 V

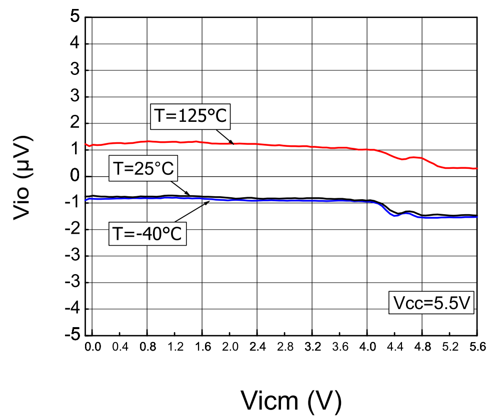


Figure 10: Input offset voltage vs. input common-mode at V_{CC} = 5.5 V

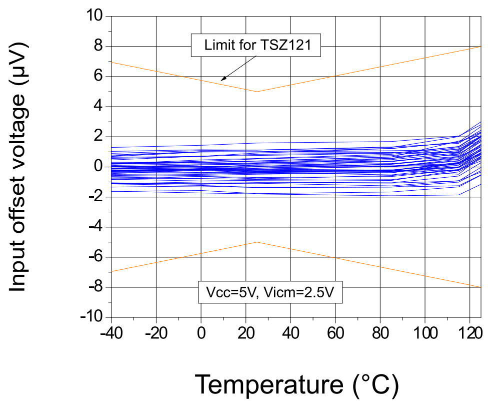


Figure 11: Input offset voltage vs. temperature

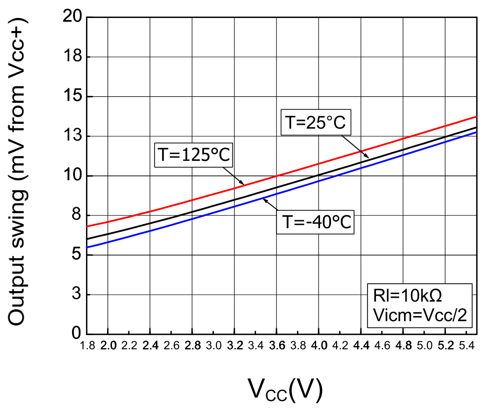


Figure 12: V_{OH} vs. supply voltage

8.3 Typical characteristic

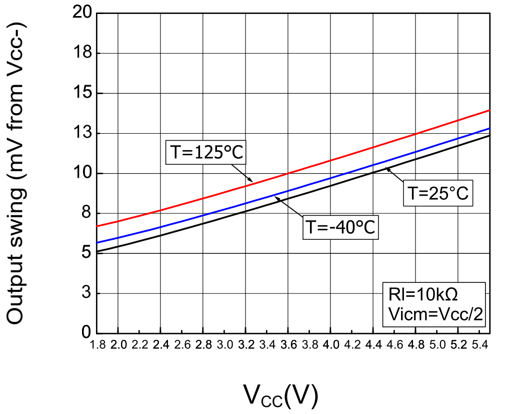


Figure 13: V_{OL} vs. supply voltage

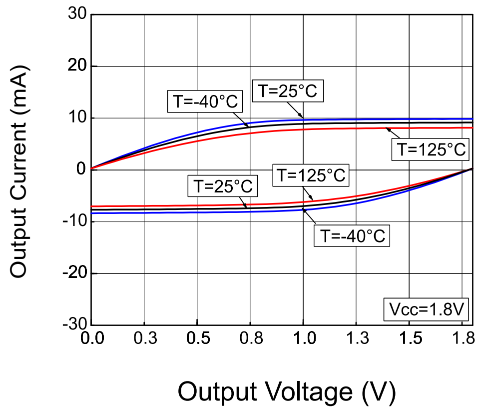


Figure 14: Output current vs. output voltage at V_{CC} = 1.8 V

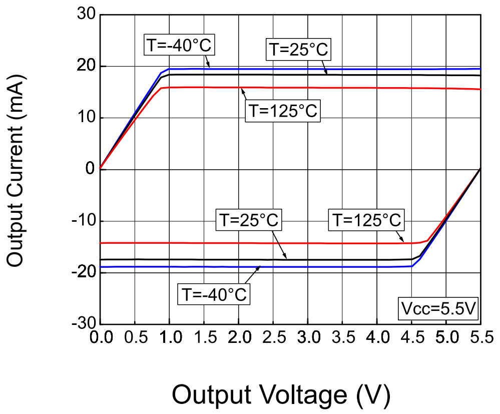


Figure 15: Output current vs. output voltage at V_{CC} = 5.5 V

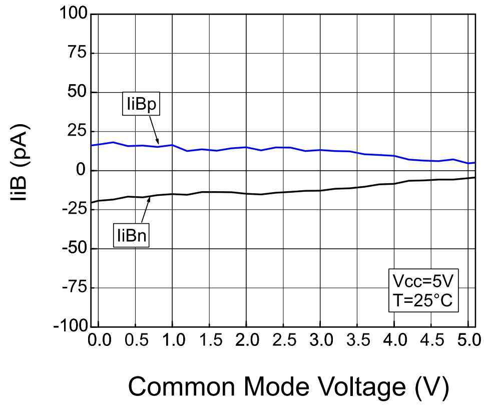


Figure 16: Input bias current vs. common mode at V_{CC} = 5 V

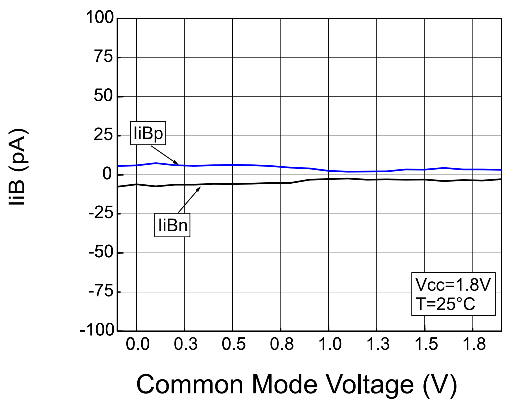


Figure 17: Input bias current vs. common mode at V_{CC} = 1.8 V

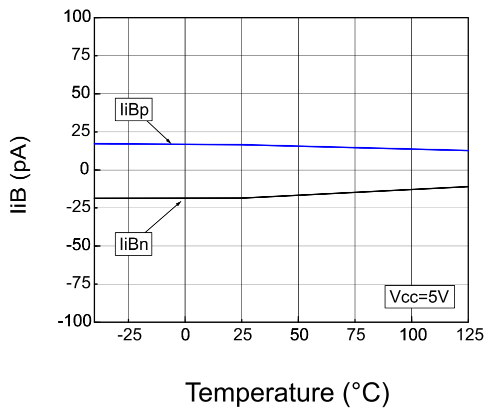


Figure 18: Input bias current vs. temperature at V_{CC} = 5 V

8.4 Typical characteristic

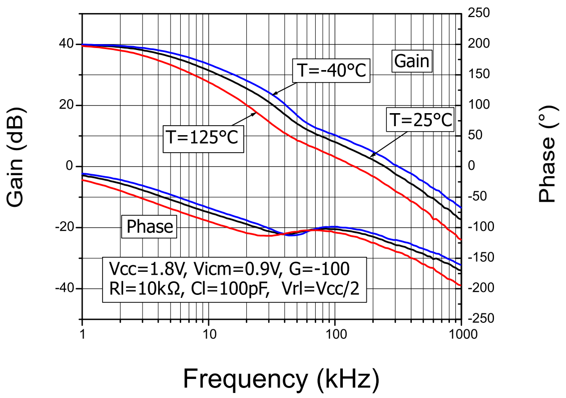


Figure 19: Bode diagram at V_{CC} = 1.8 V

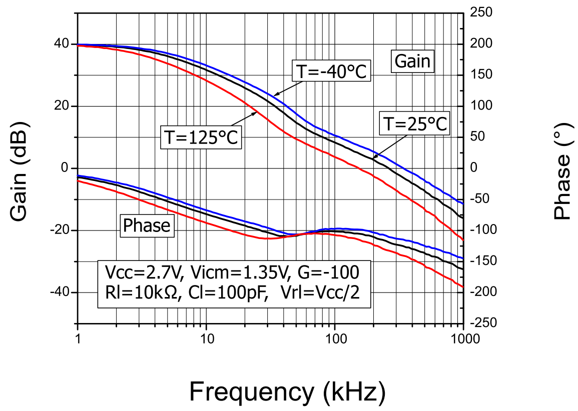


Figure 20: Bode diagram at V_{CC} = 2.7 V

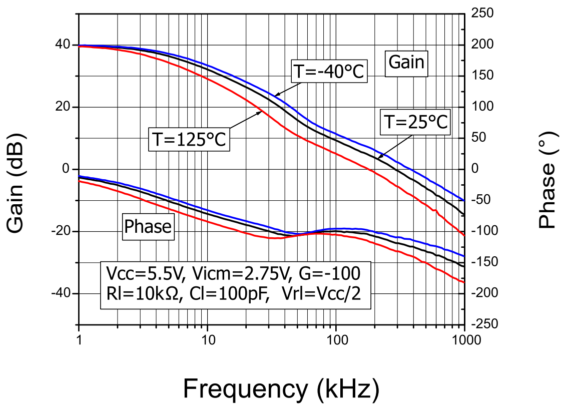


Figure 21: Bode diagram at V_{CC} = 5.5 V

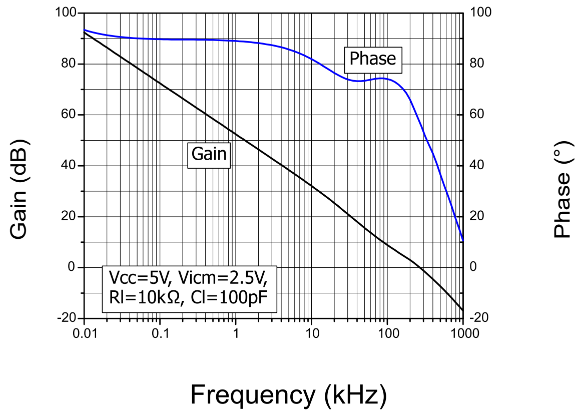


Figure 22: Open loop gain vs. frequency

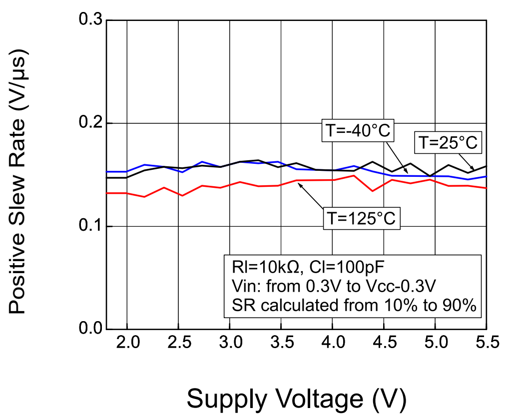


Figure 23: Positive slew rate vs. supply voltage

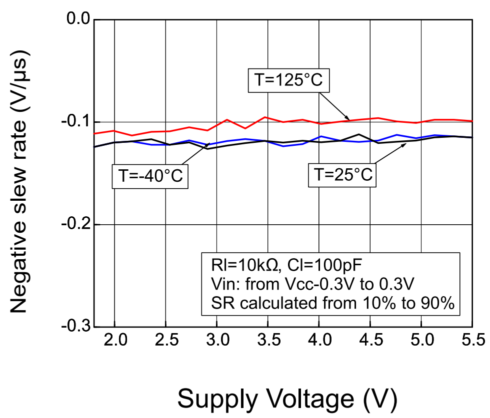


Figure 24: Negative slew rate vs. supply voltage

8.5 Typical characteristic

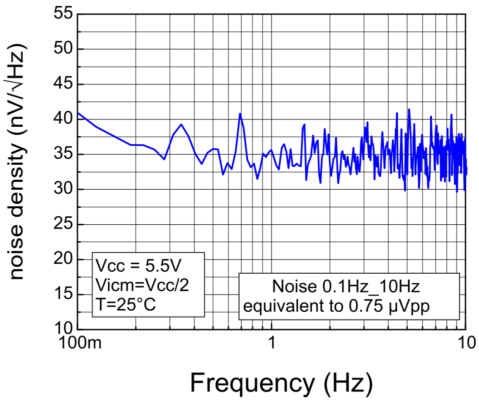


Figure 25: 0.1 Hz to 10 Hz noise

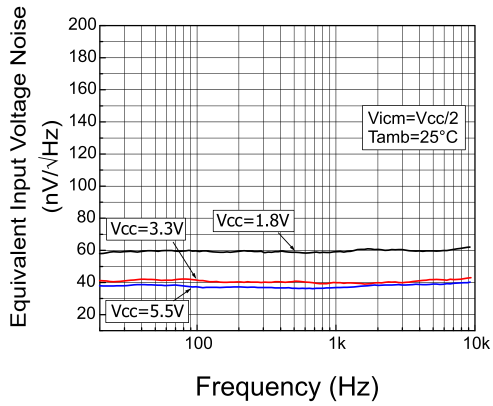


Figure 26: Noise vs. frequency

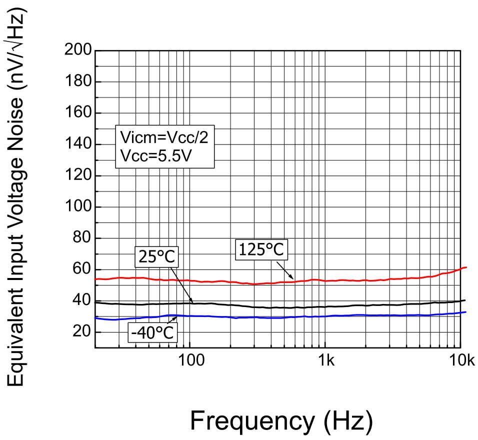


Figure 27: Noise vs. frequency and temperature

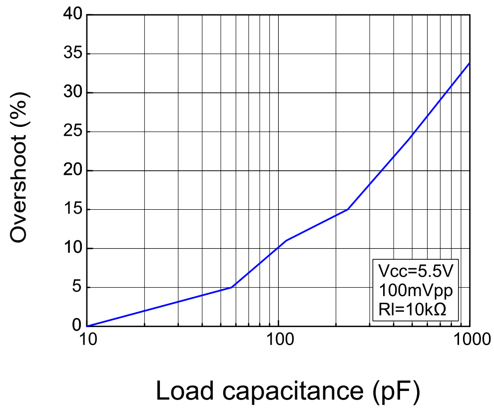


Figure 28: Output overshoot vs. load capacitance

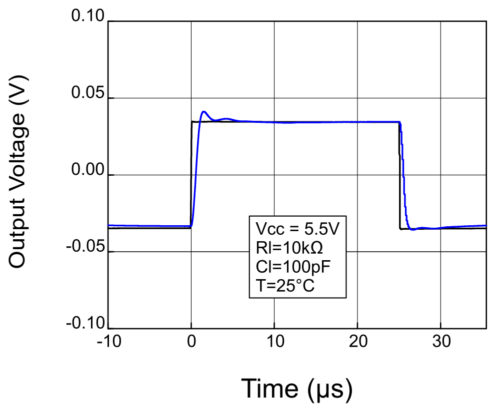


Figure 29: Small signal

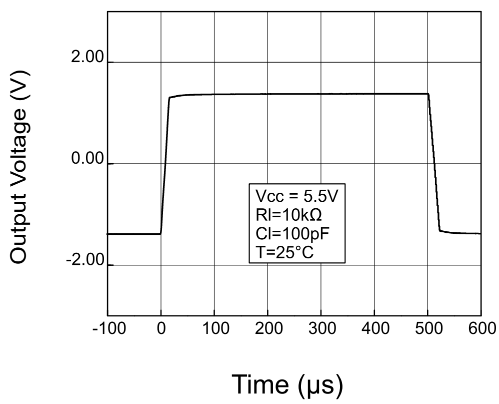


Figure 30: Large signal

8.6 Typical characteristic

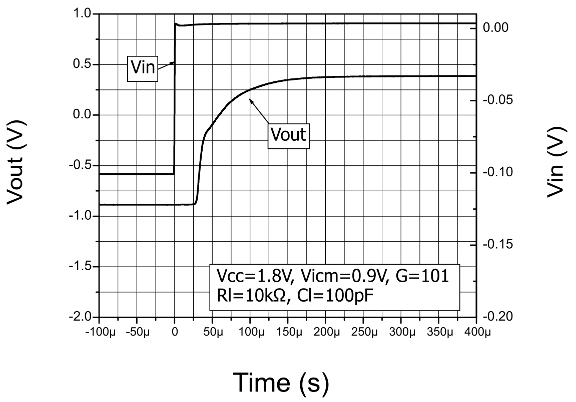


Figure 31: Positive overvoltage recovery at V_{CC} = 1.8 V

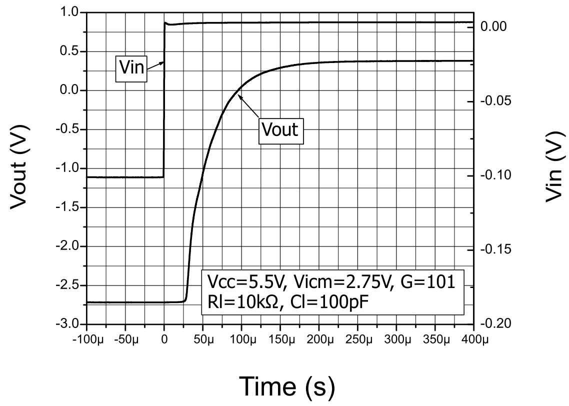


Figure 32: Positive overvoltage recovery at V_{CC} = 5 V

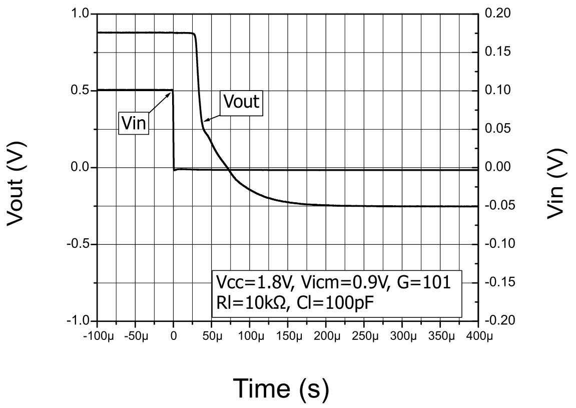


Figure 33: Negative overvoltage recovery at V_{CC} = 1.8 V

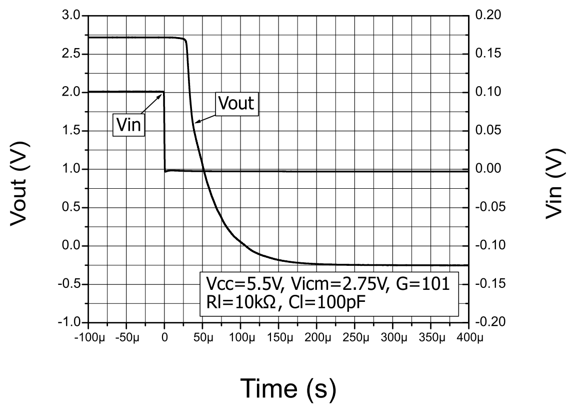


Figure 34: Negative overvoltage recovery at V_{CC} = 5 V

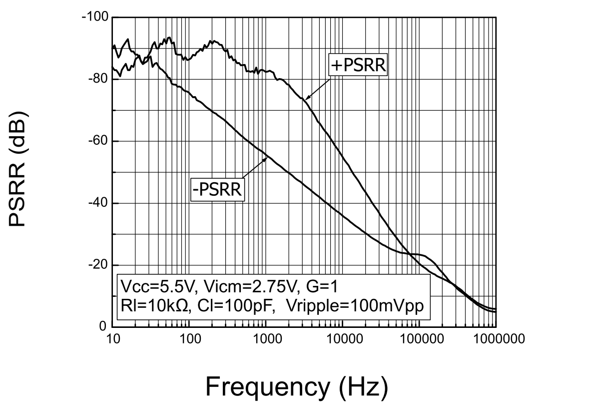


Figure 35: PSRR vs. frequency

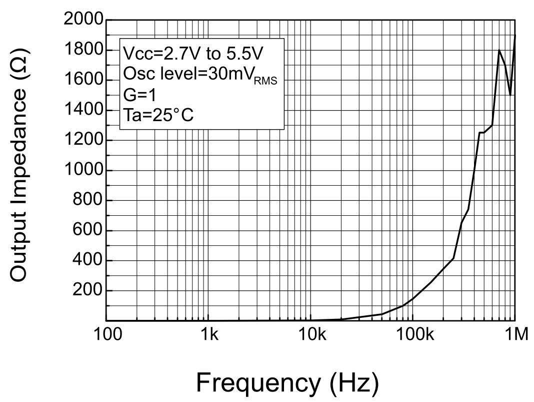
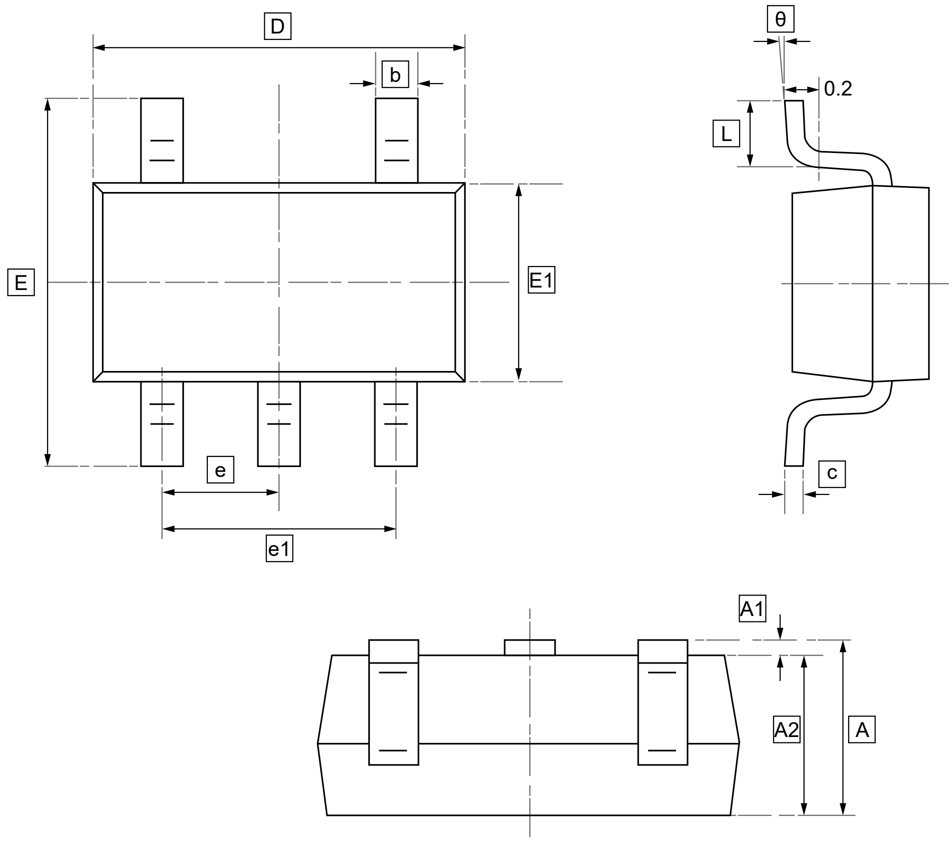


Figure 36: Output impedance vs. frequency

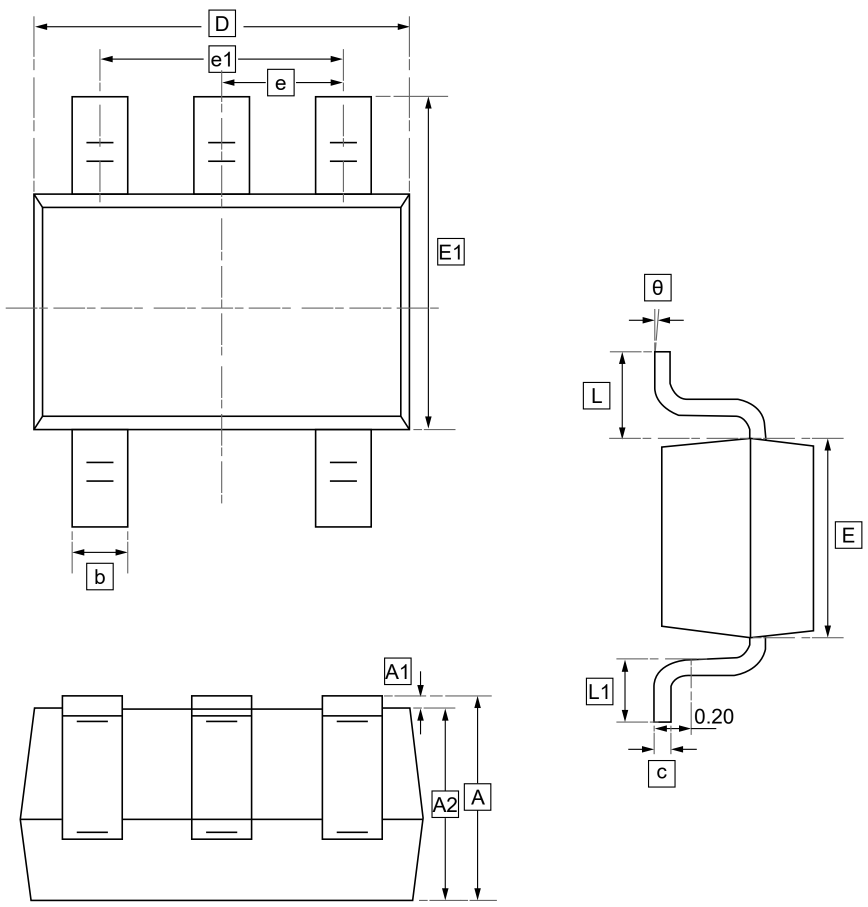
9.1 SOT-23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

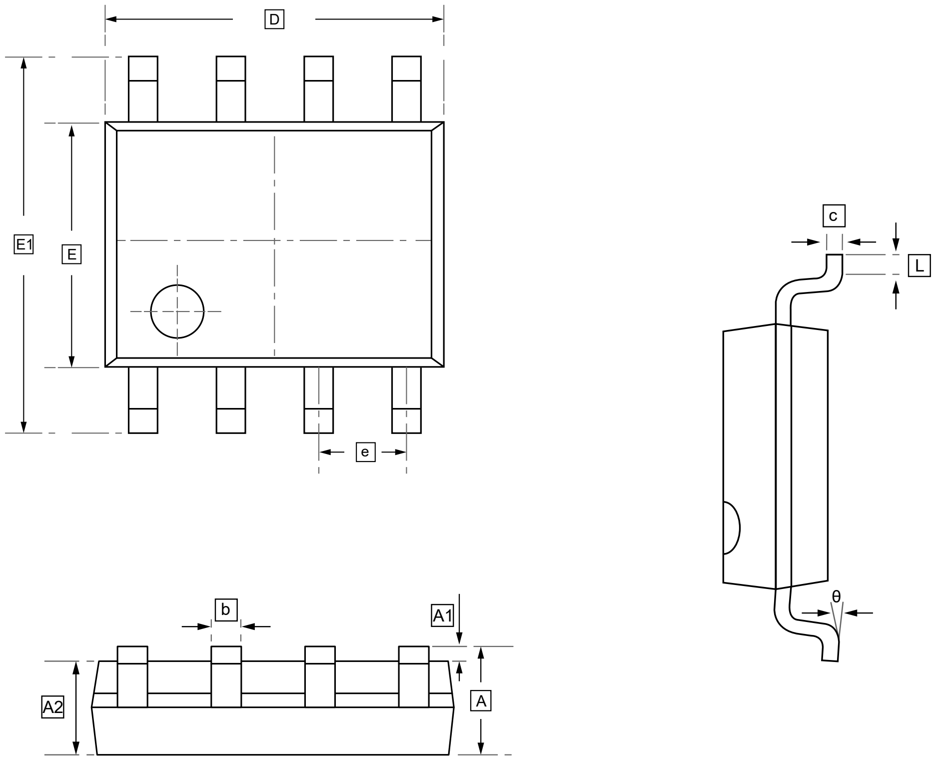
9.2 SC70-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	2.05	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

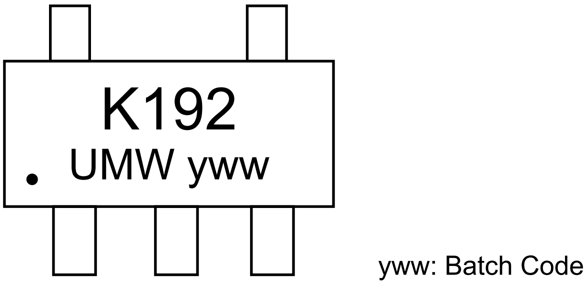
9.3 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

10.Ordering Information



Order Code	Marking	Package	Base QTY	Delivery Mode
UMW TSZ121ICT	K44	SC70-5	3000	Tape and reel
UMW TSZ121IYLT	K192	SOT23-5	3000	Tape and reel
UMW TSZ122IDT	TSZ122	SOP-8	2500	Tape and reel
UMW TSZ122IYDT	TSZ122	SOP-8	2500	Tape and reel

11.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.