1.Description

The UMW UCC27524DR device is a dual-channel, high-speed, low-side, gate-driver device capable of effectively driving MOSFET and IGBT power switches. It has a matching rise and fall time when charging and discharging the gate of the power switch. In addition, UMW UCC27524DR has a high degree of latch resistance under all conditions in its rated power and voltage range. UMW UCC27524DR is not damaged when noise spikes (any polarity) of up to 5V appear on the ground pin.UMW UCC27524DR can accept up to 500mA of reverse current without causing damage or logic confusion. All terminals are fully protected by ESD up to 2.0 kV.

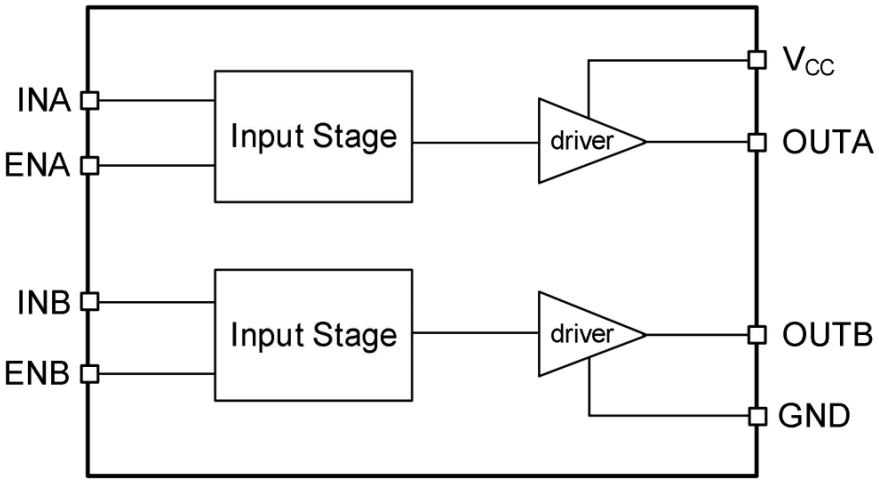
2.Applications

- line drivers
- Pulse transformer driver
- Driving MOSFETs and IGBTs
- Motor drives
- Pulse generator
- Switch-Mode Power Supplies
- DC-to-DC Converters
- Class D switching amplifier

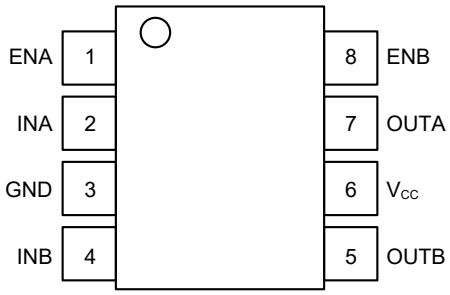
3.Features

- Latch Protection: withstand 0.5 A reverse current
- Ability to Handle Negative Voltages (-10 V) at Inputs
- Low Output Impedance
- Two Independent Gate-Drive Channel
- Independent-Enable Function for Each Output
- 4-A Peak Source and Sink-Drive Current
- 4.5 to 20-V Single-Supply Range
- High Ability of driving capacitive load:
  -- Switch time at 1nF load < 25ns
- Rise/Fall time matching
- Fast Propagation Delays (40-ns Typical)
- Operating Temperature Range of -40 to 125°C
- Turn on/Turn off Delays:
  -- Ton/Toff =70ns/70ns

4.Pin Configuration



5.Pinning Information



SOP8

Pin Functions

Number	Symbol	Description
1	ENA	Enable input for Channel A: ENA is biased LOW to disable the Channel A output regardless of the INA state. ENA is biased HIGH or left floating to enable the Channel A output. ENA is allowed to float; hence the pin-to-pin compatibility with the 27524 N/C pin
2	INA	Input to Channel A: INA is the non-inverting input in the 27524 device. OUTA is held LOW if INA is unbiased or floating
3	GND	Ground: All signals are referenced to this pin
4	INB	Input to Channel B: INA is the non-inverting input in the 27524 device. OUTB is held LOW if INB is unbiased or floating
5	OUTB	Output of Channel B
6	V_{CC}	Bias supply input
7	OUTA	Output of Channel A
8	ENB	Enable input for Channel B: ENB is biased LOW to disable the Channel B output regardless of the INB state. ENB is biased HIGH or left floating to enable the Channel B output. ENB is allowed to float; hence the pin-to-pin compatibility with the 27524 N/C pin

6.Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25°C.

Parameter	Symbol	Min	Max	Units
Supply voltage range	V_{CC}		25	V
INA, INB voltage	V_{IN}	-5	V_{CC}+0.3	V
Human body model (HBM)	ESD		2000	V
Charged device model (CDM)			1000	V
SOIC package power(T_A ≤70°C)	P_D		470	mW
Operating junction temperature	T_J		150	°C
Storage temperature	T_S	-45	150	°C

7.Electrical Characteristics

T_A=25°C, 4.5V≤V_{CC}≤18V (unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input signal high threshold	V_{IH}		2.4			V
Input signal low threshold	V_{IL}				0.8	V
Input curent	I_{IN}	0V≤V_{IN}≤V_{CC}			300	μA
High output voltage	V_{OH}		V_{CC}-0.025			V
Low output voltage	V_{OL}				0.025	V
Output pullup resistance	R_{OH}	V_{CC}=18V, I_O=100mA		0.7		Ω
Output pulldown resistance	R_{OL}	V_{CC}=18V, I_O=100mA		0.4		Ω
Peak output source current	I_{PK}			4		A
Reverse current that latch protection can withstand (Working cycle≤2%)	I_{REV}	t≤300us,V_{CC}=18V		>0.5		A
Rise time	t_R	V_{CC}=18V, C_{LOAD}=100pF			15	ns
Fall time	t_F	V_{CC}=18V, C_{LOAD}=100pF			15	ns
Turn-on propagation delay	t_{ON}	V_{CC}=18V, C_{LOAD}=100pF		25	40	ns
Turn-off propagation delay	t_{OFF}	V_{CC}=18V, C_{LOAD}=100pF		25	40	ns
Enable propagation delay	t_{EN}	V_{CC}=18V, C_{LOAD}=100pF		25	40	ns
V_{CC} quiescent supply current	I_{Q1}	V_{INA}=V_{INB}=HIGH			1.5	mA
V_{CC} quiescent supply current	I_{Q0}	V_{INA}=V_{INB}=LOW			1.5	mA
High level threshold of enable signal	V_{ENx_H}	High output level, INx=HIGH	1.8	2	2.3	V
Low level threshold of enable signal	V_{ENx_L}	Low output level, INx=HIGH	0.8	1	1.2	V
Enable signal delay	V_{ENx_HYS}			1		V
EN pull-up resistor on the pin	R_{ENx}	ENx=0V		200		KΩ

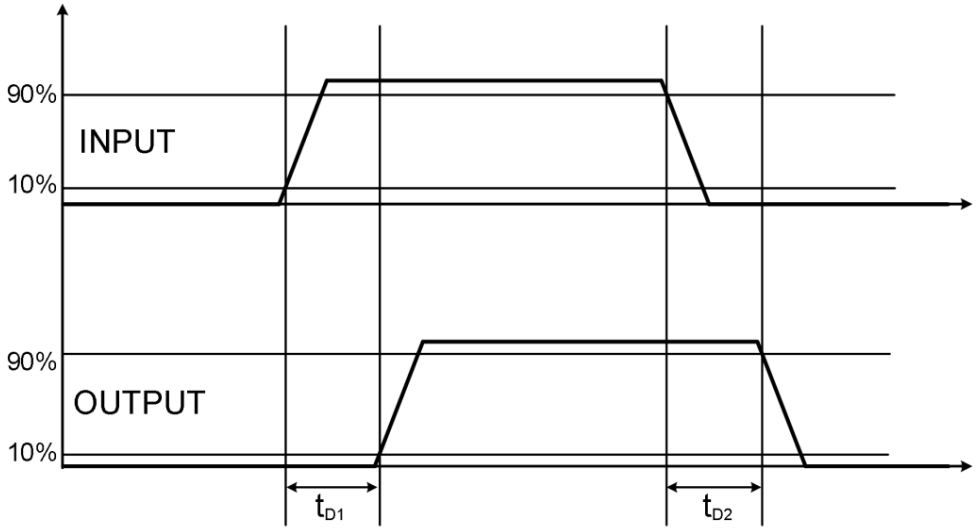


Figure 1. Input-Output waveform(non-inverting)

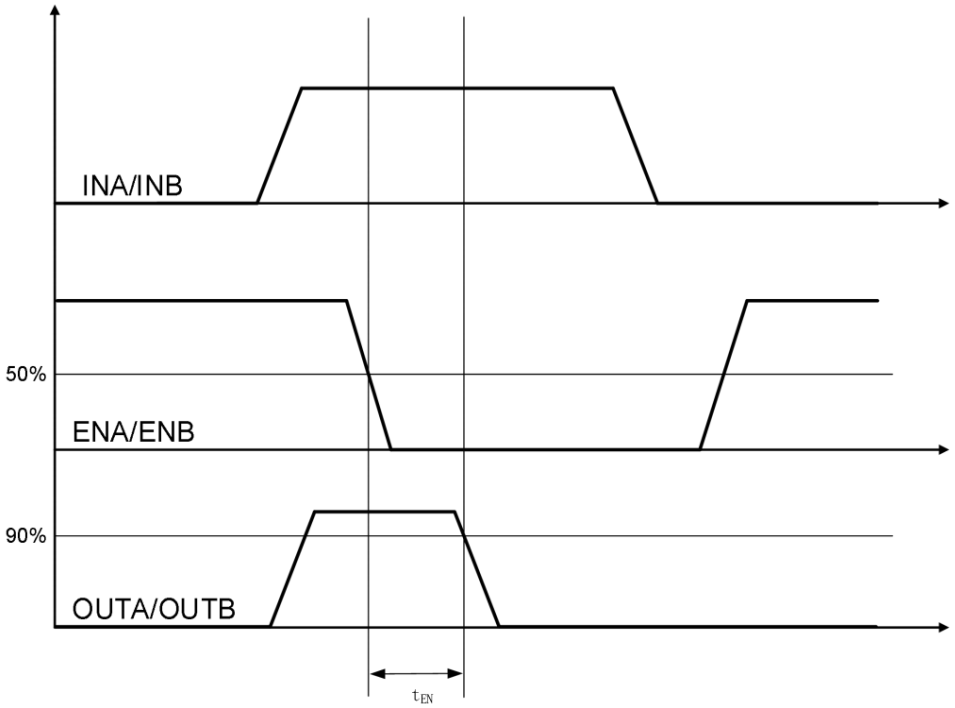


Figure 2. Enable Function waveform

8.1 Typical Characteristic

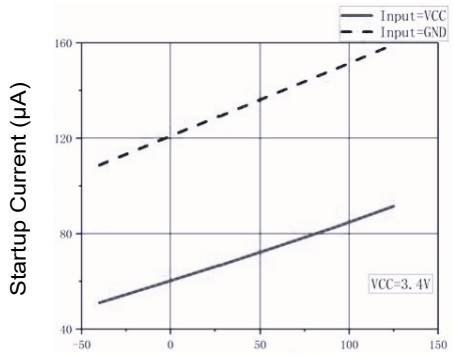


Figure 3: Start-Up Current vs Temperature

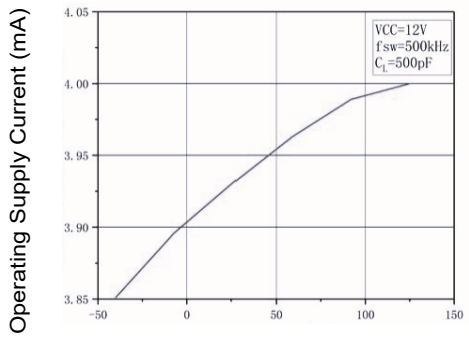


Figure 4: Operating Supply Current vs Temperature (Outputs Switching)

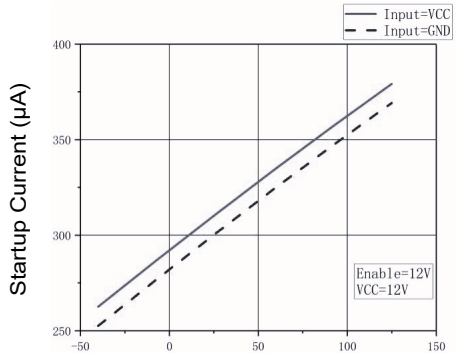


Figure 5: Supply Current vs Temperature (Outputs In DC On/Off Condition)

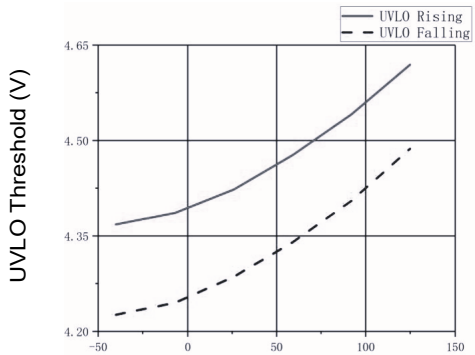


Figure 6: UVLO Threshold vs Temperature

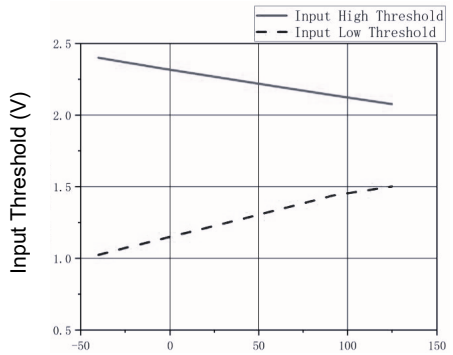


Figure 7: Input Threshold vs Temperature

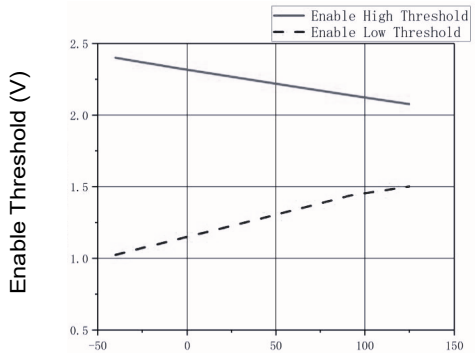


Figure 8: Enable Threshold vs Temperature

8.2 Typical Characteristic

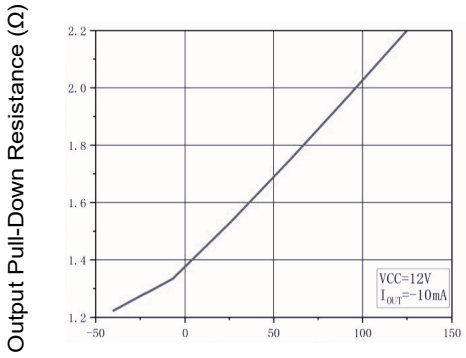


Figure 9: Output Pull-up Resistance vs Temperature

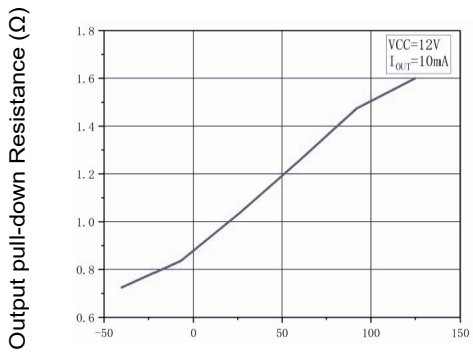


Figure 10: Output Pull-down Resistance vs Temperature

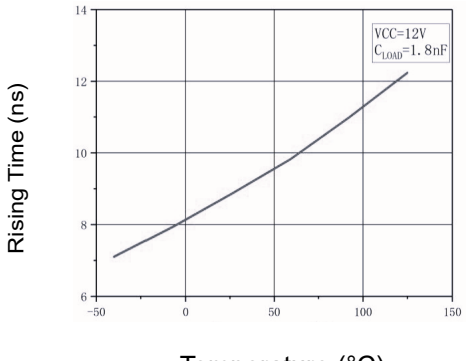


Figure 11: Rise Time vs Temperature

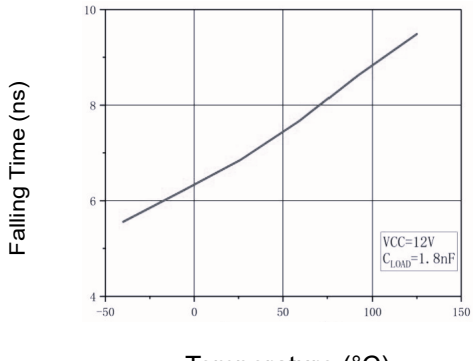


Figure 12: Fall Time vs Temperature

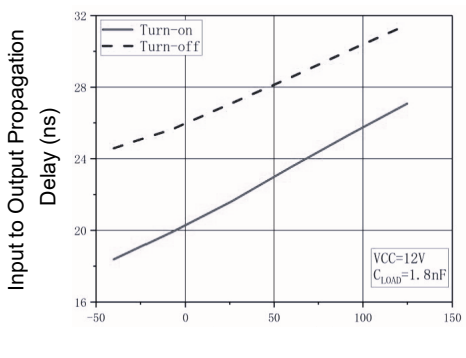


Figure 13: Input to Output Propagation Delay vs Temperature

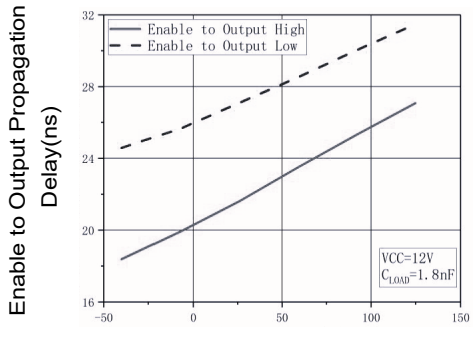


Figure 14: En to Output Propagation Delay vs Temperature

8.3 Typical Characteristic

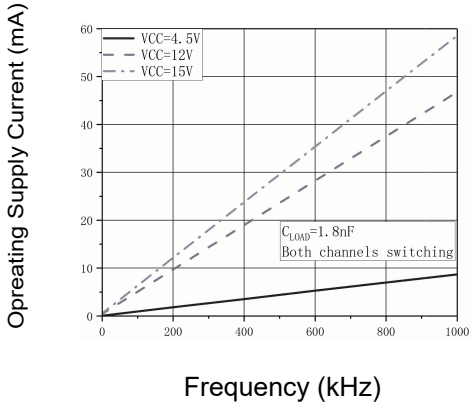


Figure 15: Operating Supply Current vs Frequency

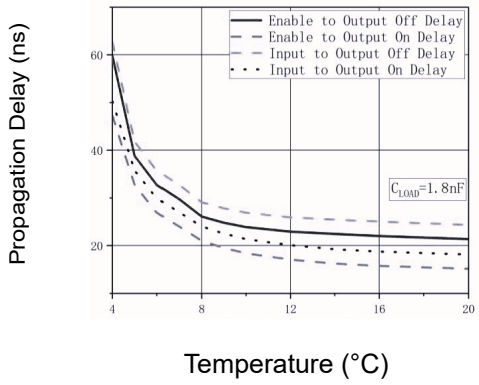


Figure 16: Propagation Delays vs Supply Voltage

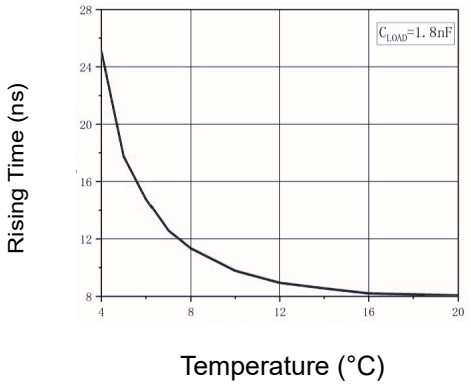


Figure 17: Rise Time vs Supply Voltage

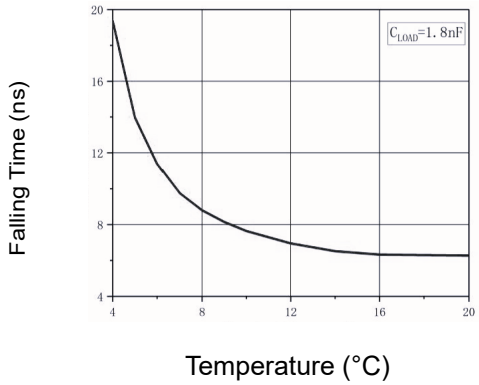


Figure 18: Fall Time vs Supply Voltage

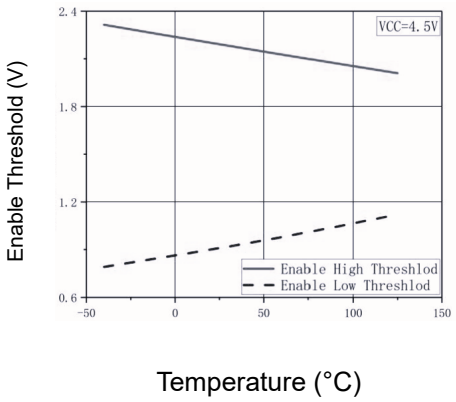
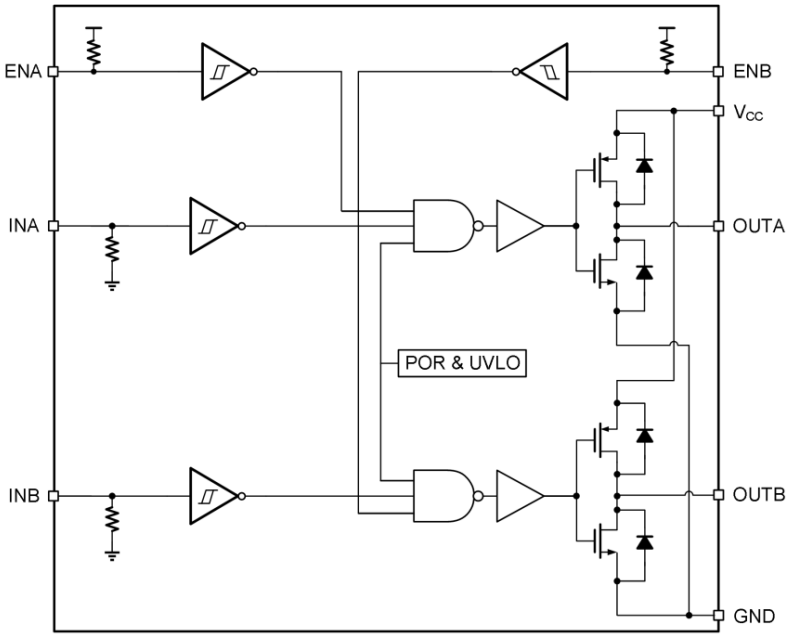


Figure 19: Enable Threshold vs Temperature

9.Functional Block Diagram



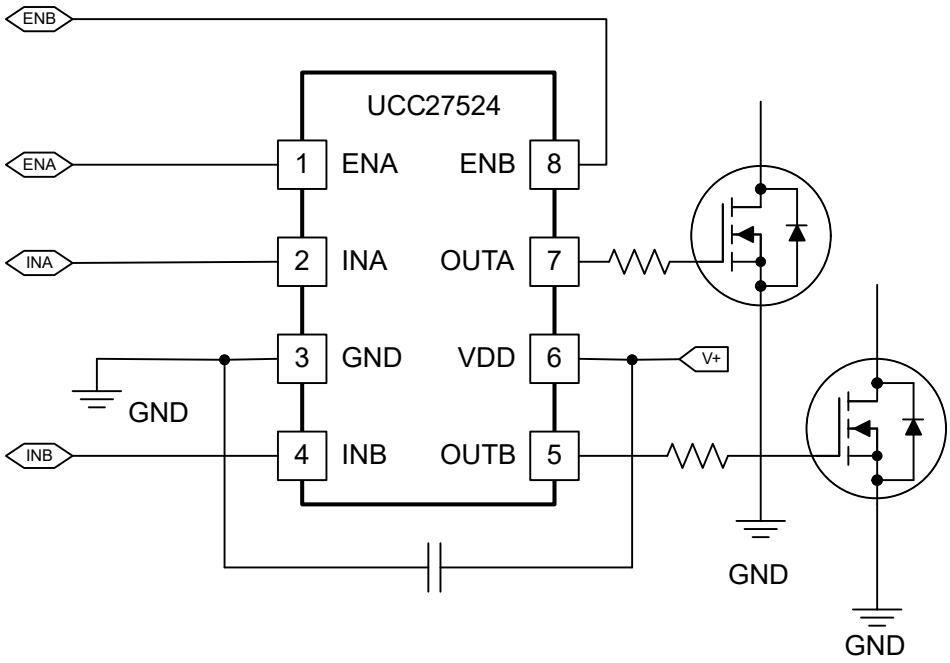
10.Device Functional Modes

Table 1 Device Logic Table

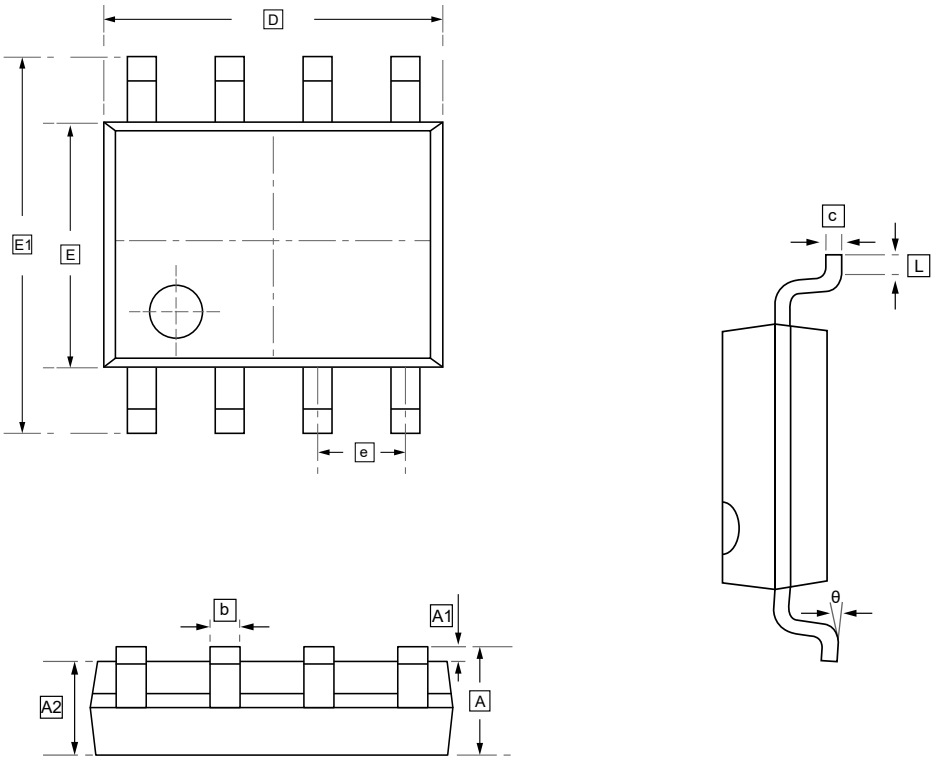
ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
x(1)	x(1)	L	H	L	H
x(1)	x(1)	H	L	H	L
x(1)	x(1)	H	H	H	H

Notes: (1) Floating condition.

11. Typical Application



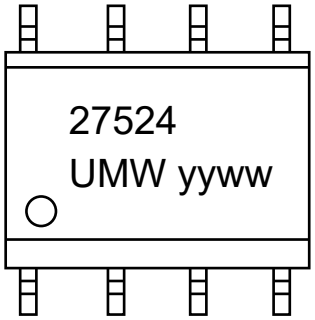
12.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

13.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW UCC27524DR	SOP-8	2500	Tape and reel

14.Disclaimer

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