UMW TSV61x/TSV61xA

Rail-to-rail input/output 10 μA, 120 kHz CMOS operational amplifiers

1.Description

The UMW TSV61x family of single and dual operational amplifiers offers low voltage, low power operation, and rail-to-rail input and output.The devices also feature an ultra-low input bias current as well as a low input offset voltage.The UMW TSV61x have a gain bandwidth product of 120 kHz while consuming only 10μA at 5V. These features make the TSV61x family ideal for sensor interfaces, battery supplied and portable applications, as well as active filtering.

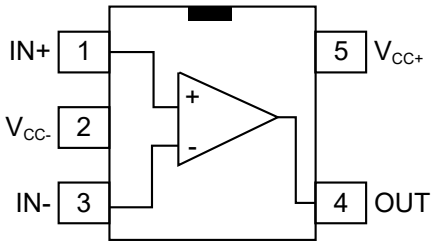
2.Features

- Rail-to-rail input and output
- Low power consumption: 10μA typ at 5V
- Low supply voltage: 1.5 to 5.5V
- Gain bandwidth product: 120kHz typ
- Unity gain stable
- Low input offset voltage: 800μV max (A version)
- Low input bias current: 1 pA typ
- Temperature range: -40 to 85 °C

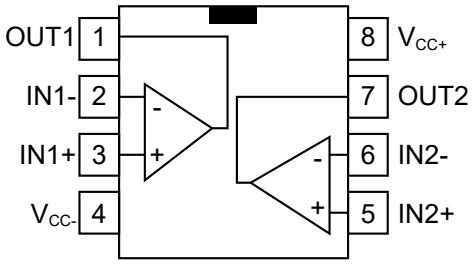
3.Applications

- Battery-powered applications
- Smoke detectors
- Proximity sensors
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

4.Pinning information



TSV611ILT/TSV611AILT/ TSV611AICT SOT23-5/SC70-5



TSV612IDT/TSV612AIDT SOP-8

5.Absolute maximum ratings and operating conditions

Parameter	Symbol	Value	Units
Supply voltage (1)	V_{CC}	6	V
Differential input voltage	V_{id}	$\pm V_{CC}$	V
Input voltage (3)	V_{in}	(V_{CC-})-0.2 to (V_{CC+})+0.2	V
Storage temperature	T_{STG}	-65 to 150	°C
Thermal resistance junction to ambient (4) (5)	R_{thja}		°C/W
SC70-5		205	°C/W
SOT23-5		250	°C/W
SOP8		125	°C/W
Maximum junction temperature	T_J	150	°C
HBM: human body model (6)	ESD	4	kV
MM: machine model (7)		200	V
CDM: charged device model (8)		1.5	kV
Latch-up immunity		200	mA

Notes:

(1) All voltage values, except differential voltage, are with respect to network ground terminal.

(2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3) V_{CC} - V_{in} must not exceed 6 V

(4) Short-circuits can cause excessive heating and destructive dissipation.

(5) Rth are typical values.

(6) Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

(7) Machine mode: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.

(8) Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

6.Operating conditions

Parameter	Symbol	Rating	Units
Supply voltage	V_{CC}	1.5 to 5.5	V
Common mode input voltage range	V_{icm}	(V_{CC-})-0.1 to (V_{CC+})+0.1	V
Operating free air temperature range	T_{oper}	-40 to +85	°C

7.1 Electrical Characteristics

(V_{CC+})=1.8V with (V_{CC-})=0V, V_{icm}=V_{CC}/2, T_{amb}=25°C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC performance						
Offset voltage	V_{io}	UMW TSV61x			4	mV
		UMW TSV61xA			0.8	mV
		T_{min}<T_{op}<T_{max}, UMW TSV61x			5	mV
		T_{min}<T_{op}<T_{max}, UMW TSV61xA			2	mV
Input offset voltage drift	$\Delta V_{io}/\Delta T$			2		µV/°C
Input offset current, V_{out}=V_{CC}/2	I_{io}	T_{min}<T_{op}<T_{max}		1	10(1)	pA
				1	100	pA
Input bias current, V_{out}=V_{CC}/2	I_{ib}	T_{min}<T_{op}<T_{max}		1	10(1)	pA
				1	100	pA
Common mode rejection ratio, 20 log ($\Delta V_{ic}/\Delta V_{io}$)	CMR	0V to 1.8V, V_{out}=0.9V	55	71		dB
		T_{min}<T_{op}<T_{max}	53			dB
Large signal voltage gain	A_{vd}	R_L=10kΩ, V_{out}=0.5V to 1.3V	78	83		dB
		T_{min}<T_{op}<T_{max}	74			dB
High-level output voltage (V_{OH}=V_{CC} - V_{out})	V_{OH}	R_L=10kΩ		4	35	mV
		T_{min}<T_{op}<T_{max}			50	mV
Low-level output voltage	V_{OL}	R_L=10kΩ		7	35	mV
		T_{min}<T_{op}<T_{max}			50	mV
Isink	I_{OUT}	V_{out}=1.8V	9	13		mA
		T_{min}<T_{op}<T_{max}	9			mA
Isource		V_{out}=0V	8	10		mA
		T_{min}<T_{op}<T_{max}	8			mA
Supply current (per operator)	I_{CC}	No load, V_{out}=V_{CC}/2	6.5	9	12	µA
		T_{min}<T_{op}<T_{max}	6		12.5	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AC performance						
Gain bandwidth product	GBP	R_L=10kΩ, C_L=20pF		100		kHz
Phase margin	φm	R_L=10kΩ, C_L=20pF		60		Degrees
Gain margin	G_m	R_L=10kΩ, C_L=20pF		9.5		dB
Slew rate	SR	R_L=10kΩ, C_L=20pF,V_{out}=0.5V to 1.3V		0.03		V/µs
Equivalent input noise voltage	e_n	f=1kHz		110		nV/√Hz
Total harmonic distortion + noise	THD+N	Fin=1kHz, A_v=1 V_{out}=1V_{pp}, RL=100kΩ, BW=22kHz		0.07		%

1. Guaranteed by design.

7.2 Electrical Characteristics

(V_{CC+})=3.3V with (V_{CC-})=0V, V_{icm}=V_{CC}/2, T_{amb}=25°C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC performance						
Offset voltage	V_{io}	UMW TSV61x			4	mV
		UMW TSV61xA			0.8	mV
		T_{min}<T_{op}<T_{max}, UMW TSV61x			5	mV
		T_{min}<T_{op}<T_{max}, UMW TSV61xA			2	mV
Input offset voltage drift	$\Delta V_{io}/\Delta T$			2		µV/°C
Input offset current	I_{io}	T_{min}<T_{op}<T_{max}		1	10(1)	pA
				1	100	pA
Input bias current	I_{ib}	T_{min}<T_{op}<T_{max}		1	10(1)	pA
				1	100	pA
Common mode rejection ratio, 20 log ($\Delta V_{ic}/\Delta V_{io}$)	CMR	0V to 3.3V, V_{out}=1.75V	61	76		dB
		T_{min}<T_{op}<T_{max}	58			dB
Large signal voltage gain	A_{vd}	R_L=10kΩ, V_{out}=0.5V to 2.8V	85	92		dB
		T_{min}<T_{op}<T_{max}	83			dB
High-level output voltage (V_{OH}=V_{CC} - V_{out})	V_{OH}	R_L=10kΩ		5	35	mV
		T_{min}<T_{op}<T_{max}			50	mV
Low-level output voltage	V_{OL}	R_L=10kΩ		10	35	mV
		T_{min}<T_{op}<T_{max}			50	mV
Isink	I_{OUT}	V_O=V_{CC}	37	44		mA
		T_{min}<T_{op}<T_{max}	35			mA
Isource		V_O=0V	32	38		mA
		T_{min}<T_{op}<T_{max}	30			mA
Supply current (per operator)	I_{CC}	No load, V_{out}=V_{CC}/2	6.5	9.5	12.5	µA
		T_{min}<T_{op}<T_{max}	6		13	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AC performance						
Gain bandwidth product	GBP	R_L=10kΩ, C_L=20pF		110		kHz
Phase margin	φm	R_L=10kΩ, C_L=20pF		60		Degrees
Gain margin	G_m	R_L=10kΩ, C_L=20pF		9.5		dB
Slew rate	SR	R_L=10kΩ, C_L=20pF,V_{out}=0.5V to 2.8V		0.035		V/µs
Equivalent input noise voltage	e_n	f=1kHz		110		nV/√Hz

1. Guaranteed by design.

7.3 Electrical Characteristics

(V_{CC+})=5V with (V_{CC-})=0V, V_{icm}=V_{CC}/2, T_{amb}=25°C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset voltage	V_{io}	UMW TSV61x			4	mV
		UMW TSV61xA			0.8	mV
		T_{min}<T_{op}<T_{max}, UMW TSV61x			5	mV
		T_{min}<T_{op}<T_{max}, UMW TSV61xA			2	mV
Input offset voltage drift	$\Delta V_{io}/\Delta T$			2		µV/°C
Input offset current	I_{io}	T_{min}<T_{op}<T_{max}		1	10(1)	pA
				1	100	pA
Input bias current	I_{ib}	T_{min}<T_{op}<T_{max}		1	10(1)	pA
				1	100	pA
Common mode rejection ratio, 20 log ($\Delta V_{ic}/\Delta V_{io}$)	CMR	0V to 5V, V_{out}=2.5V	64	80		dB
		T_{min}<T_{op}<T_{max}	63			dB
Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	SVR	V_{CC}=1.8 to 5V	76	93		dB
		T_{min}<T_{op}<T_{max}	74			dB
Large signal voltage gain	A_{vd}	R_L=10kΩ, V_{out}=0.5V to 4.5V	88	93		dB
		T_{min}<T_{op}<T_{max}	85			dB
High level output voltage V_{OH}=V_{CC}-V_{out}	V_{OH}	R_L=10kΩ		7	35	mV
		T_{min}<T_{op}<T_{max}			50	mV
Low level output voltage	V_{OL}	R_L=10kΩ		16	35	mV
		T_{min}<T_{op}<T_{max}			50	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I_{sink}	I_{OUT}	$V_O=V_{CC}$	52	57		mA
		$T_{min}<T_{op}<T_{max}$	42			mA
I_{source}		$V_O=0V$	58	63		mA
		$T_{min}<T_{op}<T_{max}$	49			mA
Supply current (per operator)	I_{CC}	No load, $V_{out}=V_{CC}/2$	7.5	10.5	14	μA
		$T_{min}<T_{op}<T_{max}$	7		15	μA
AC performance						
Gain bandwidth product	GBP	R_L=10kΩ, C_L=20pF		120		kHz
Phase margin	φm	R_L=10kΩ, C_L=20pF		62		Degrees
Gain margin	G_m	R_L=10kΩ, C_L=20pF		10		dB
Slew rate	SR	R_L=10kΩ,C_L=20pF,V_{out}=0.5V to 4.5V		0.04		V/μs
Equivalent input noise voltage	e_n	f=1kHz		105		nV/√Hz
Total harmonic distortion + noise	THD+N	F_{in}=1kHz, A_v=1 V_{out}=1V_{pp}, RL=100kΩ, BW=22kHz		0.02		%

1. Guaranteed by design.

8.1 Typical characteristic

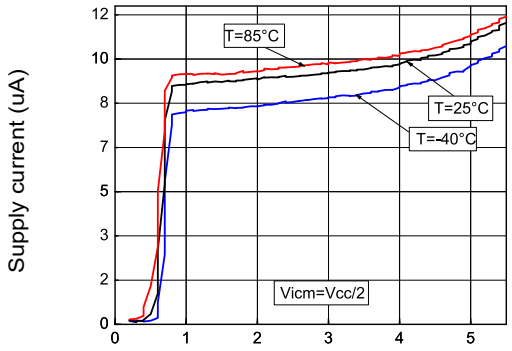


Figure 1: Supply current vs. supply voltage at V_{icm}= V_{CC}/2

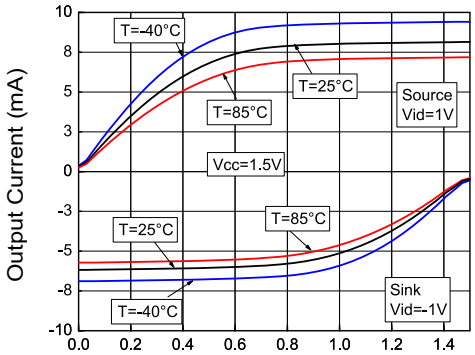


Figure 2: Output current vs. output voltage at V_{CC}=1.5V

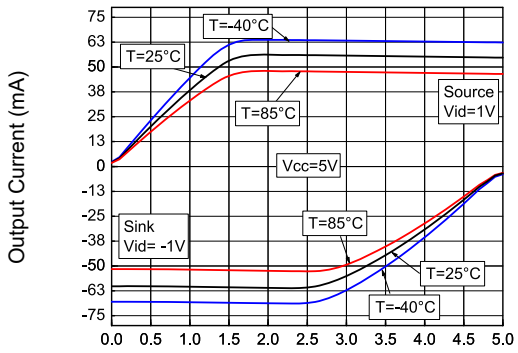


Figure 3: Output current vs. output voltage at V_{CC}=5V

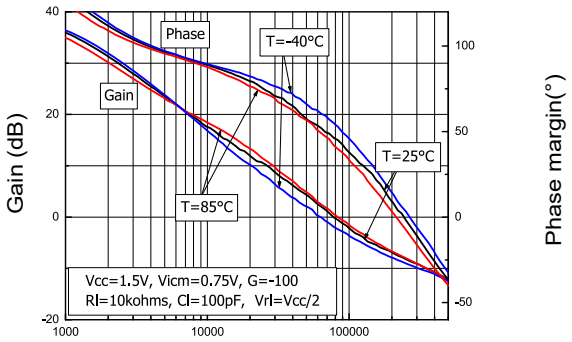


Figure 4: Voltage gain and phase vs. frequency at V_{CC}=1.5V

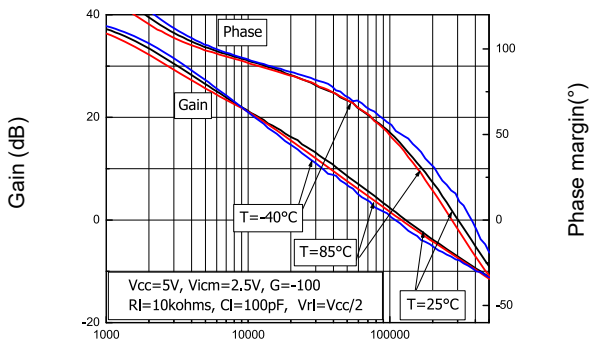


Figure 5: Voltage gain and phase vs. frequency at V_{CC}=5V

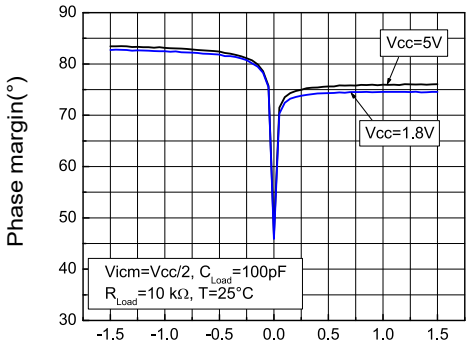


Figure 6: Phase margin vs. output current

8.2 Typical characteristic

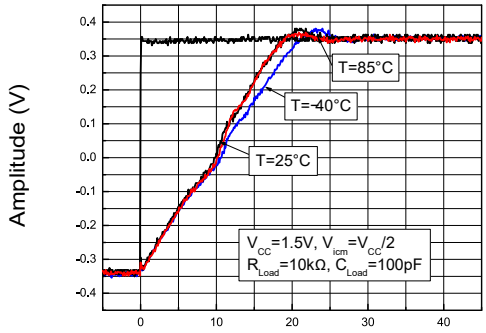


Figure 7: Positive slew rate vs. time, V_{CC}=1.5V, C_{Load}=100pF, R_{Load}=10kΩ

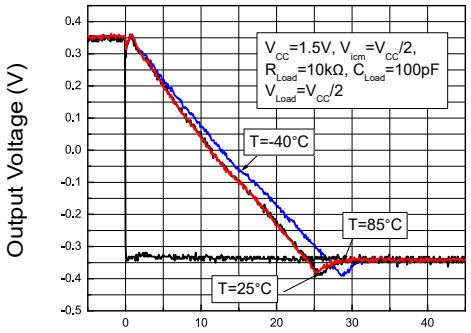


Figure 8: Negative slew rate vs. time, V_{CC}=1.5V, C_{Load}=100pF, R_{Load}=10kΩ

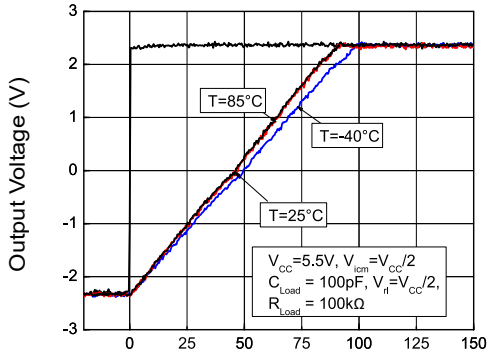


Figure 9: Positive slew rate vs. time, V_{CC}=5.5V, C_{Load}=100pF, R_{Load}=100kΩ

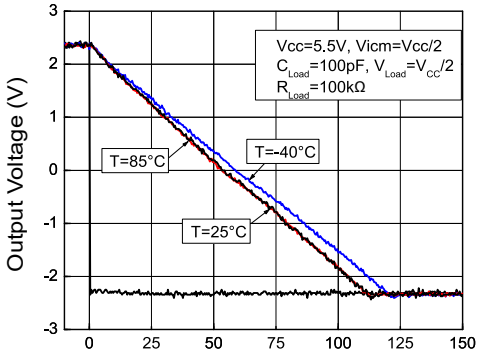


Figure 10: Negative slew rate vs. time, V_{CC}=5.5V, C_{Load}=100pF, R_{Load}=100kΩ

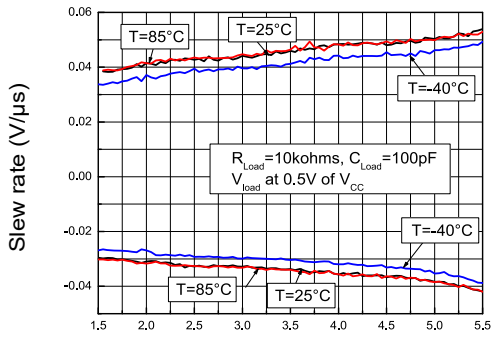


Figure 11: Slew rate vs. supply voltage

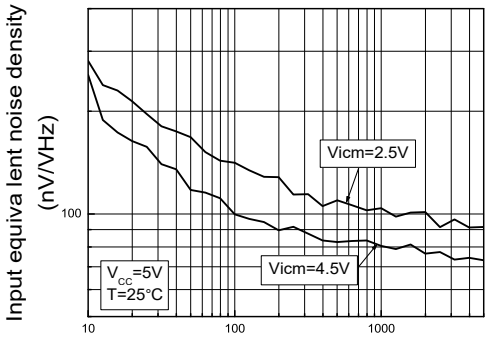


Figure 12: Noise vs. frequency at V_{CC}=5V

8.3 Typical characteristic

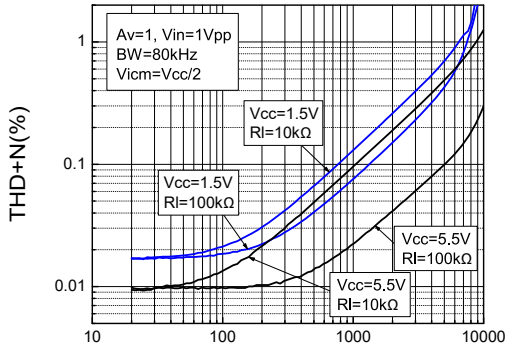


Figure 13: Distortion + noise vs. frequency

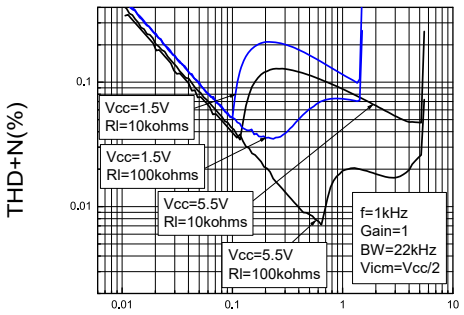


Figure 14: Distortion + noise vs. output voltage

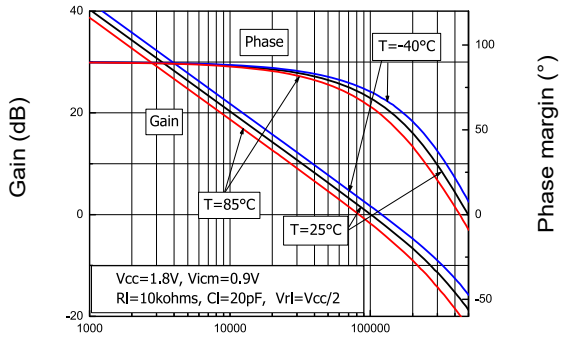


Figure 15: Voltage gain and phase vs. frequency at V_{CC}=1.8V (based on simulation results)

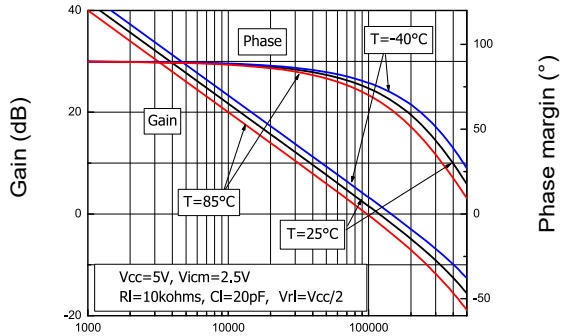


Figure 16: Voltage gain and phase vs. frequency at V_{CC}=5V (based on simulation results)

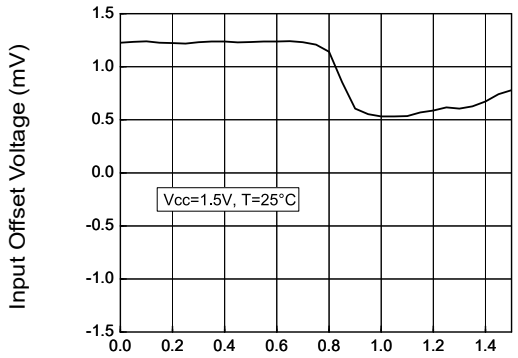


Figure 17: Input offset voltage vs input common mode at V_{CC}=1.5V

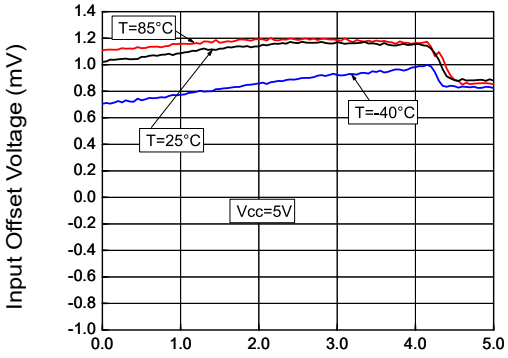
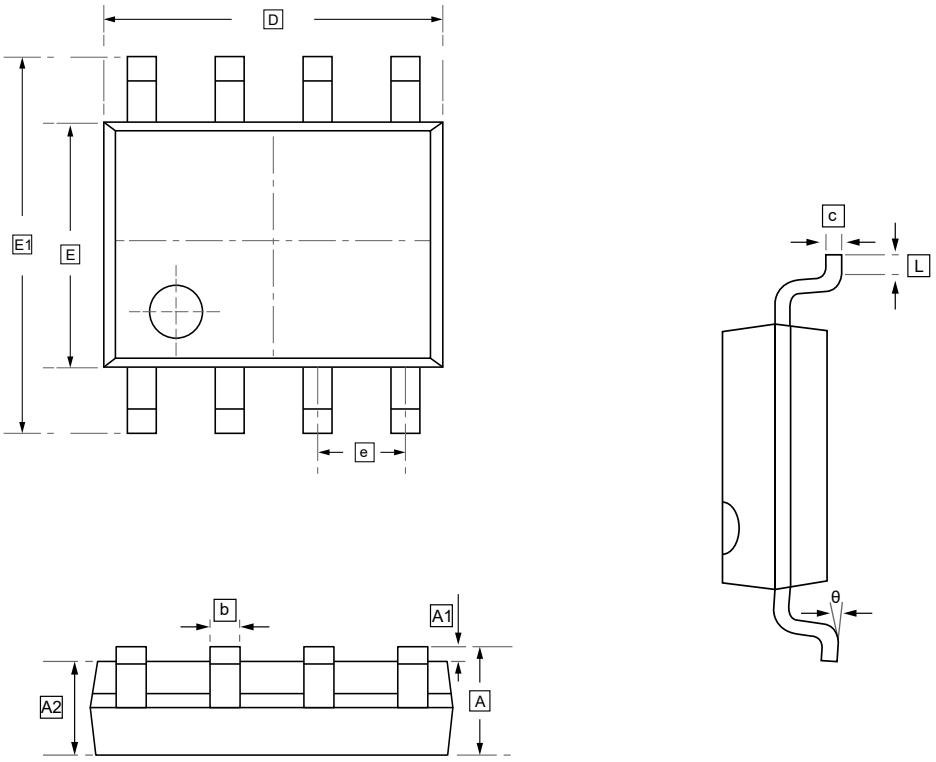


Figure 18: Input offset voltage vs input common mode at V_{CC}=5V

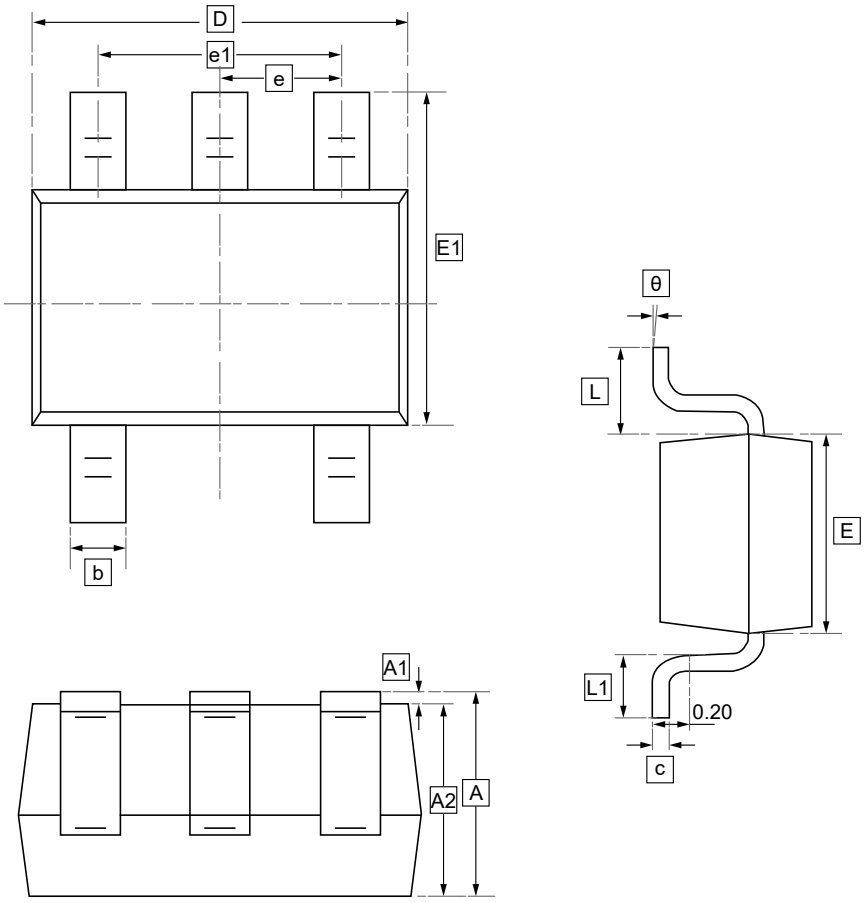
9.1 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

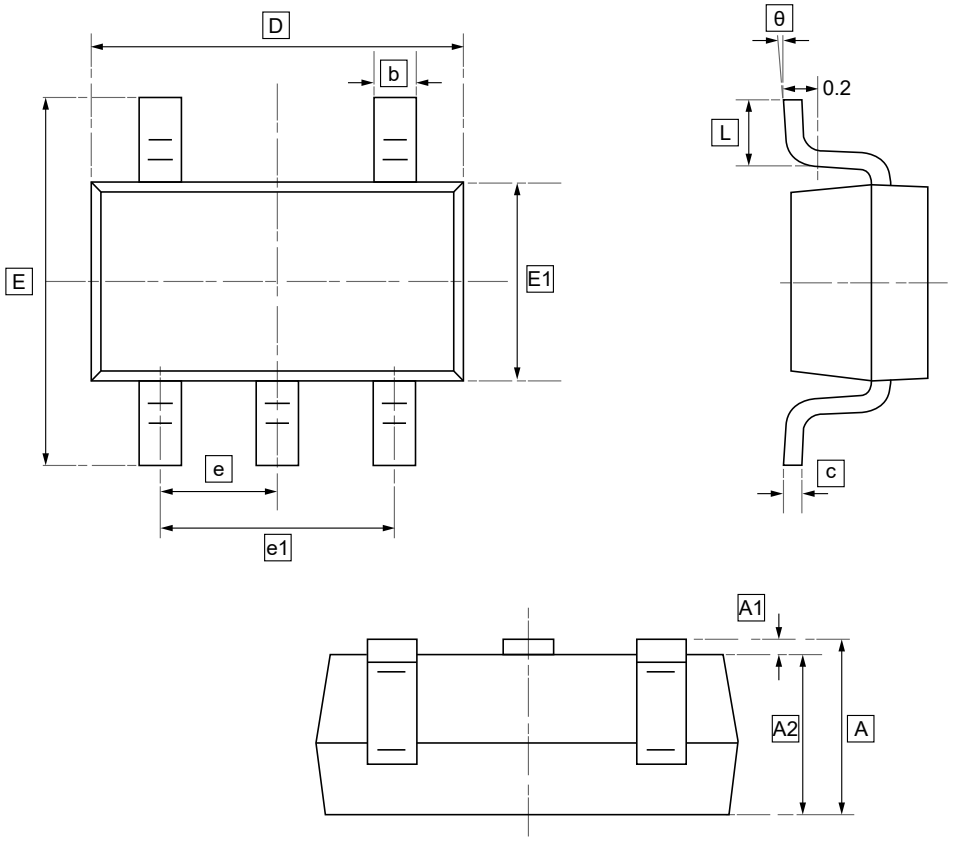
9.2 SC70-5(SOT353) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	2.05	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

9.3 SOT-23-5 Package Outline Dimensions

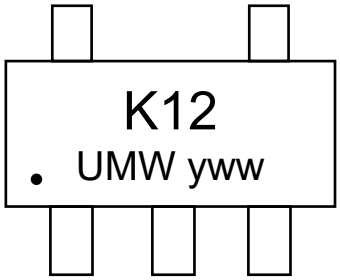


DIMENSIONS (mm are the original dimensions)

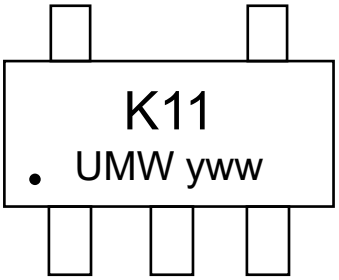
Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

10.Ordering information

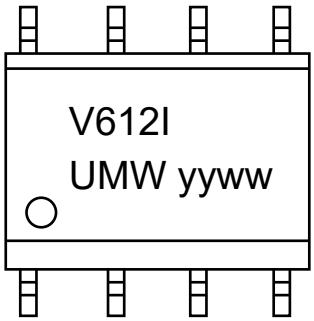
SOT23-5



SC70-5



SOP-8



y: Year Code
yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMWTSV611ILT	K12	SOT23-5	3000	Tape and reel
UMWTSV611AILT	K11	SOT23-5	3000	Tape and reel
UMWTSV611AICT	K11	SC70-5	3000	Tape and reel
UMW TSV612IDT	V612I	SOP-8	2500	Tape and reel
UMWTSV612AIDT	V612AI	SOP-8	2500	Tape and reel

11.Disclaimer

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