# UMW IRFR1018ETR

60V N-Channel MOSFET

## 1.1Features

- $V_{DS(V)}$=60V
- $I_D$=56A
- $R_{DS(ON)}$<8.4mΩ($V_{GS}$=10V)
- Improved Gate, Avalanche and
- Dynamic dv/dt Ruggedness

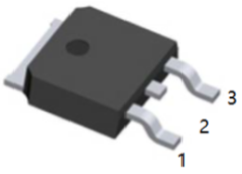
## 1.2Features

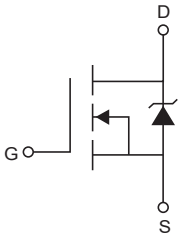
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

## 2.Pinning information

| Pin | Symbol | Description |
|---|---|---|
| 1 | G | GATE |
| 3 | S | SOURCE |
| 2 | D | DRAIN |

**TO-252(DPAK)**
**top view**




## 3.Absolute Maximum Ratings

| Parameter | | Symbol | Rating | Units |
|---|---|---|---|---|
| Continuous Drain Current, $V_{GS}$ @ 10V(Silicon Limited) | $T_C$=25°C | $I_D$ | 79 ① | A |
| Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | $T_C$=100°C | | 56 ① | A |
| Continuous Drain Current, $V_{GS}$ @ 10V (Wire Bond Limited) | $T_C$=25°C | | 56 | A |
| Pulsed Drain Current ② | | $I_{DM}$ | 315 | A |
| Maximum Power Dissipation | $T_C$=25°C | $P_D$ | 110 | W |
| Linear Derating Factor | | | 0.76 | W/°C |
| Gate-to-Source Voltage | | $V_{GS}$ | ±20 | V |
| Peak Diode Recovery ④ | | dv/dt | 21 | V/ns |
| Operating Junction andStorage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 175 | °C |
| Soldering Temperature, for 10 seconds (1.6mm from case) | | | 300 | °C |

| | | | |
|---|---|---|---|
| Single Pulse Avalanche Energy ③ | $E_{AS(Thermally\ limited)}$ | 88 | mJ |
| Avalanche Current ② | $I_{AR}$ | 47 | A |
| Repetitive Avalanche Energy ⑤ | $E_{AR}$ | 11 | mJ |
| Junction-to-Case ⑨ | $R_{\theta JC}$ | 1.32 | °C/W |
| Junction-to-Ambient (PCB Mount) ⑧⑨ | $R_{\theta JA}$ | 50 | °C/W |
| Junction-to-Ambient ⑨ | $R_{\theta JA}$ | 110 | °C/W |

## 4.Electrical Characteristics @ $T_J$= 25°C (unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $I_D$=250μA, $V_{GS}$=0V | 60 | | | V |
| Breakdown Voltage Temp. Coefficient | $\Delta V_{(BR)DSS}/\Delta T_J$ | Reference to 25°C,$I_D$=5mA② | | 0.073 | | V/°C |
| Static Drain-to-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=47A ⑤ | | 7.1 | 8.4 | mΩ |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=100μA | | | 4 | V |
| Drain-to-Source Leakage Current | $I_{DSS}$ | $V_{DS}$=60V, $V_{GS}$=0V | 2 | | 20 | μA |
| | | $V_{DS}$=48V, $V_{GS}$=0V, $T_J$=125°C | | | 250 | μA |
| Gate-to-Source Forward Leakage | $I_{GSS}$ | $V_{GS}$=20V | | | 100 | nA |
| Gate-to-Source Reverse Leakage | | $V_{GS}$=-20V | | | -100 | nA |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=50V, $I_D$=47A | 110 | | | S |
| Total Gate Charge | $Q_g$ | $I_D$=47A, $V_{DS}$=30V, $V_{GS}$=10V⑤ | | 46 | 69 | nC |
| Gate-to-Source Charge | $Q_{gs}$ | | | 10 | | nC |
| Gate-to-Drain ("Miller") Charge | $Q_{gd}$ | | | 12 | | nC |
| Total Gate Charge Sync.($Q_g$-$Q_{gd}$) | $Q_{sync}$ | $I_D$=47A, $V_{DS}$=30V, $V_{GS}$=10V | | 34 | | nC |
| Internal Gate Resistance | $R_{G(int)}$ | | | 0.73 | | Ω |
| Tum-On Delay Time | $t_{D(on)}$ | $V_{DD}$=39V, $I_D$=47A<br>$R_G$=10Ω, $V_{GS}$=10V ⑤ | | 13 | | ns |
| Rise Time | $t_r$ | | | 35 | | ns |
| Turn-Off Delay Time | $t_{D(off)}$ | | | 55 | | ns |
| Fall Time | $t_f$ | | | 46 | | ns |
| Input Capacitance | $C_{iss}$ | $V_{GS}$=0V, $V_{DS}$=50V<br>$f$=1MHz | | 2290 | | pF |
| Output Capacitance | $C_{oss}$ | | | 270 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 130 | | pF |
| Effective Output Capacitance (Energy Related) | $C_{oss}$eff.(ER) | $V_{GS}$=0V, $V_{DS}$=0V to 60V ⑦ | | 390 | | pF |
| Effective Output Capacitance (Time Related) | $C_{oss}$eff.(TR) | $V_{GS}$=0V, $V_{DS}$=0V to 60V ⑥ | | 630 | | pF |

| Diode Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| Continuous Source Current (Body Diode) | $I_S$ | MOSFET symbol showing the integral reverse p-n junction diode. | | | 79① | A |
| Pulsed Source Current (Body Diode) ② | $I_{SM}$ | | | | 315 | A |
| Diode Forward Voltage | $V_{SD}$ | $T_J$=25°C,$I_S$=47A,$V_{GS}$=0V ⑤ | | | 1.3 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J$=25°C, $V_R$=51V | | 26 | 39 | ns |
| | | $T_J$=125°C, $I_F$=47A | | 31 | 47 | ns |
| Reverse Recovery Charge | $Q_{rr}$ | $T_J$=25°C, di/dt=100A/μs ⑤ | | 24 | 36 | nC |
| | | $T_J$=125°C | | 35 | 53 | nC |
| Reverse Recovery Current | $I_{RRM}$ | $T_J$=25°C | | 1.8 | | A |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by $T_{Jmax}$, starting $T_J$=25°C, L=0.08mH, $R_G$=25Ω, $I_{AS}$=47A, $V_{GS}$=10V. Part not recommended for use above this value.

④ $I_{SD}$ ≤ 47A, di/dt ≤ 1668A/μs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recom mended footprint and soldering techniques refer to application note #AN-994.

⑨ $R_\theta$ is measured at $T_J$ approximately 90°C.

## 6.1Typical Characterisitics

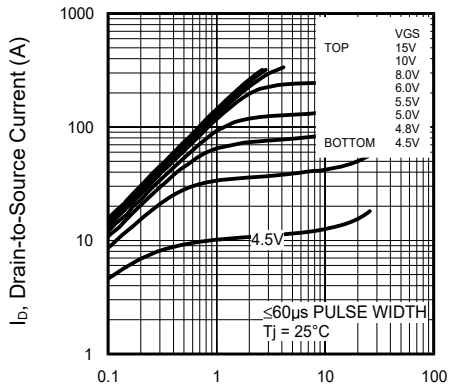



Figure 1: Typical On-Resistance vs. Gate Voltage

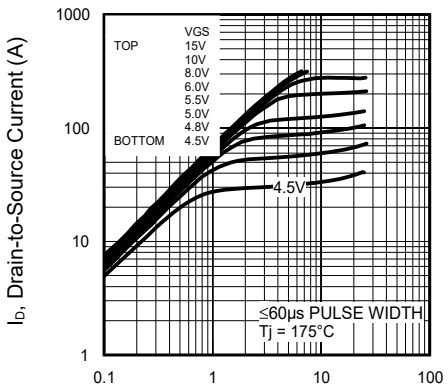



Figure 2: Typical Output Characteristics

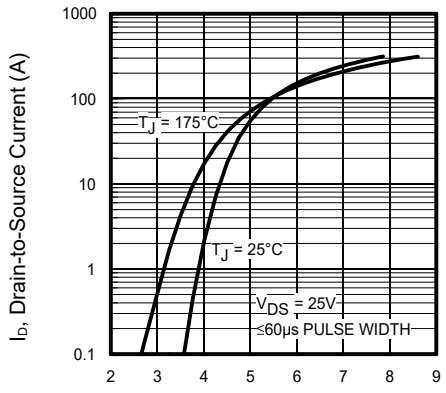



Figure 3: Typical Output Characteristics

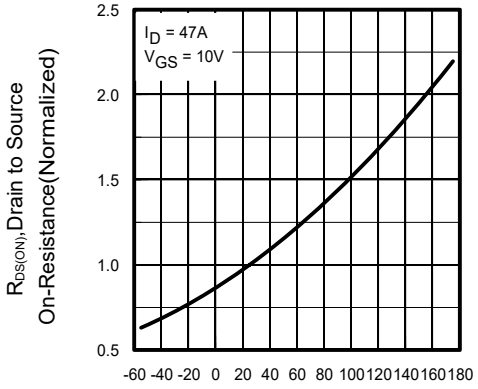



Figure 4: Normalized On-Resistance vs. Temperature

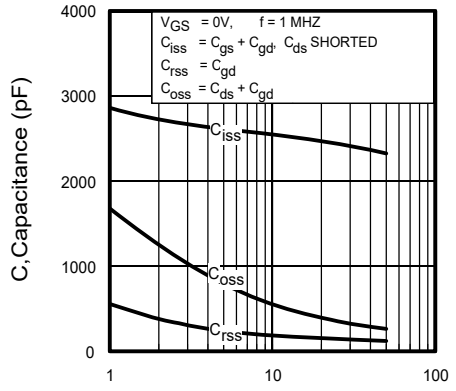



Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

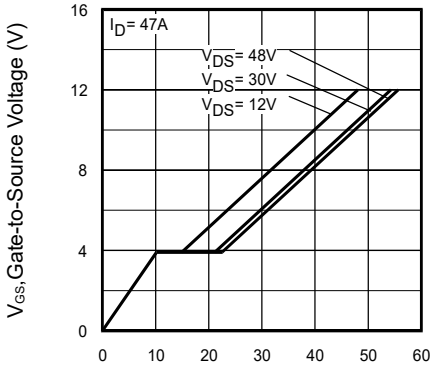



Figure 6: Typical Gate Charge vs.

## 6.2Typical Characterisitics

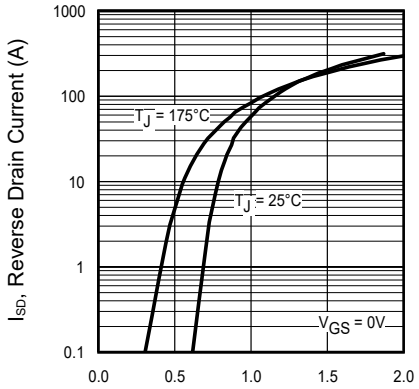



Figure 7: Typical Capacitance vs. Drain-to-Source Voltage

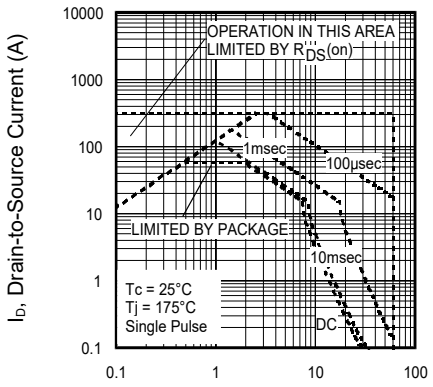



Figure 8: Maximum Safe Operating Area

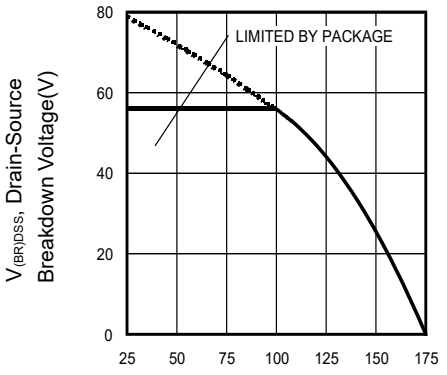



Figure 9: Drain-to-Source Breakdown Voltage

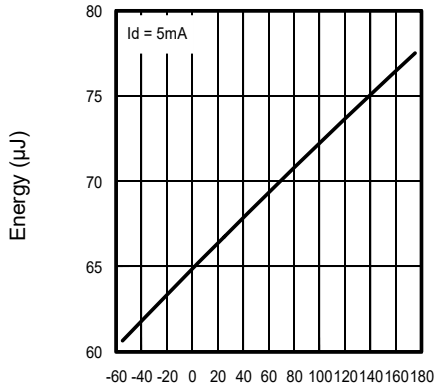



Figure 10: Typical $C_{oss}$ Stored Energy

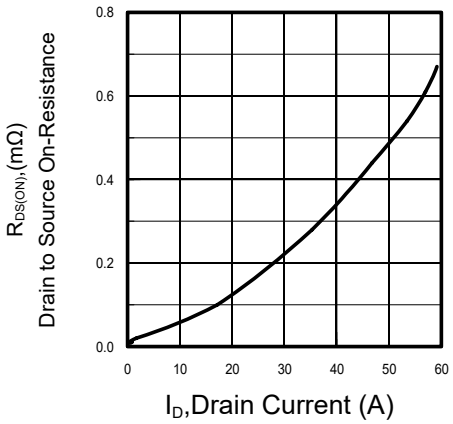



Figure 11: Typical On-Resistance vs. Drain Current

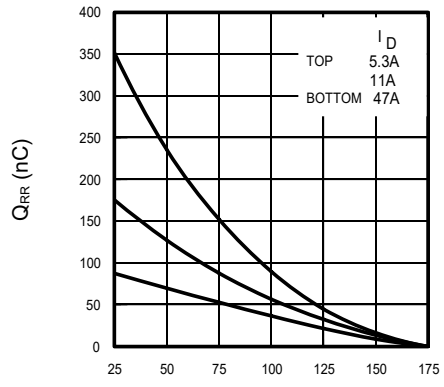



Figure 12: Typical Stored Charge vs. dif/dt

## 6.3Typical Characterisitics

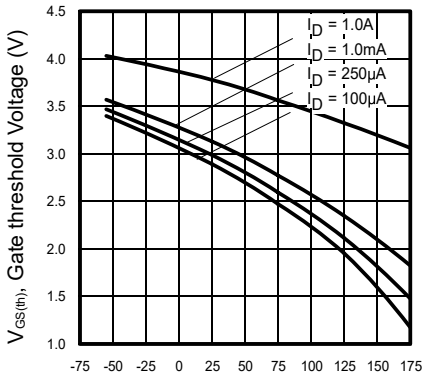



Figure 13: Threshold Voltage vs. Temperature

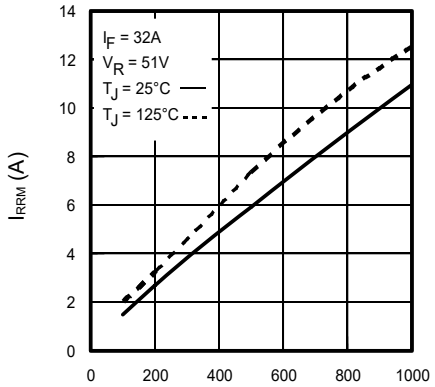



Figure 14: Typical Recovery Current vs. dif/dt

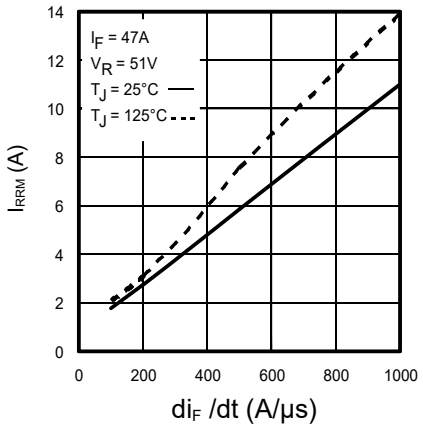



Figure 15: Typical Recovery Current vs. dif/dt

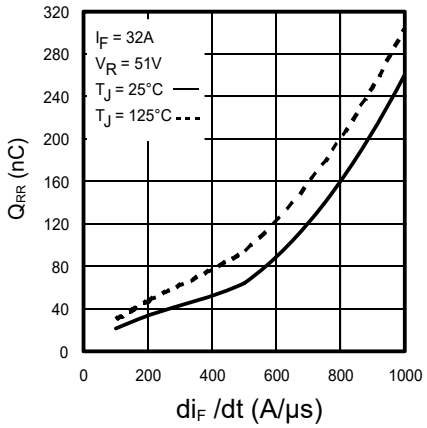



Figure 16: Typical Stored Charge vs. dif/dt

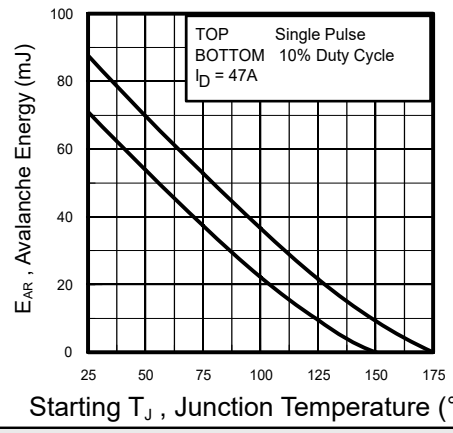



Figure 17: Typical On-Resistance vs. Drain Current

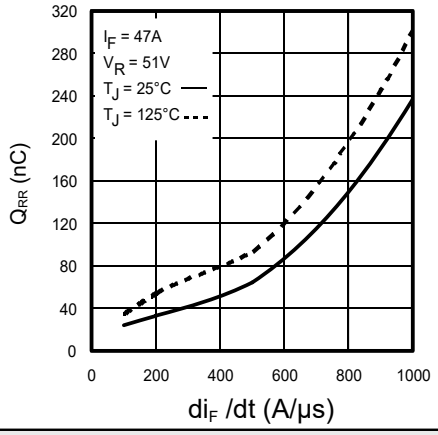



Figure 18: Typical Stored Charge vs. $di_f$/dt

## 6.4Typical Characterisitics

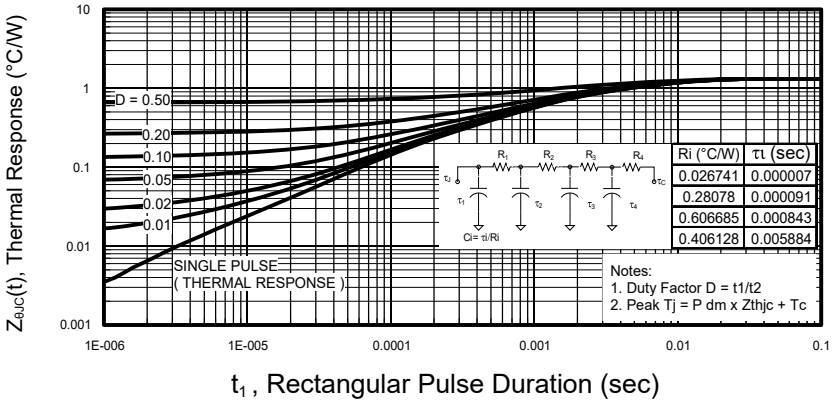



Figure 19: Maximum Effective Transient Thermal Impedance, Junction-to-Case

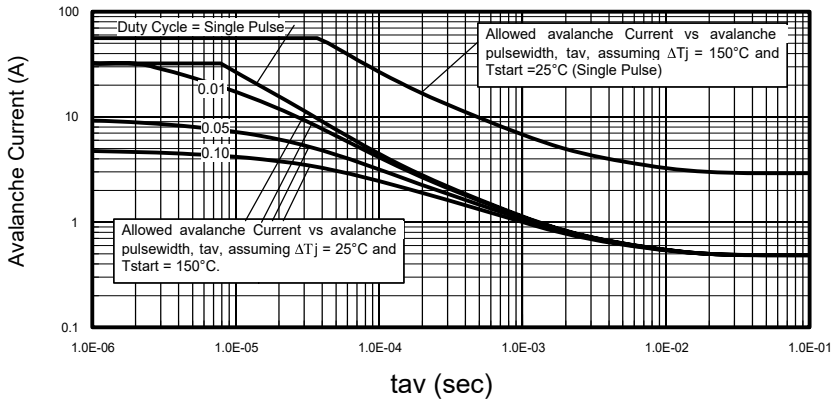
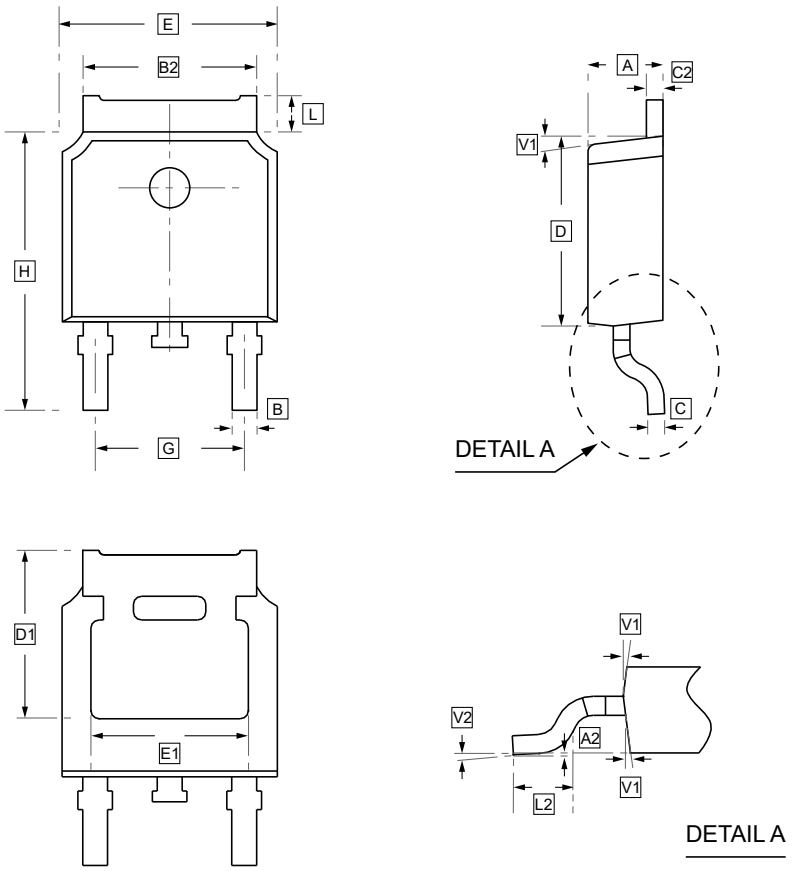



Figure 20: Typical Avalanche Current vs.Pulse width

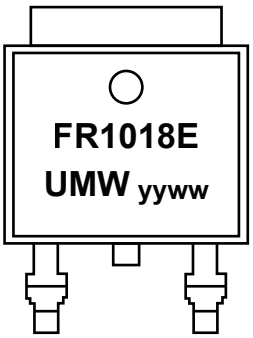
## 7.TO-252 PACKAGE OUTLINE DIMENSIONS




**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A2 | B | B2 | C | C2 | D | D1 | E | E1 | G | H | L | L2 | V1 | V2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | 2.10 | 0 | 0.66 | 5.18 | 0.40 | 0.44 | 5.90 | 5.30 | 6.40 | 4.63 | 4.47 | 9.50 | 1.09 | 1.35 | | 0° |
| Max | 2.50 | 0.10 | 0.86 | 5.48 | 0.60 | 0.58 | 6.30 | REF | 6.80 | | 4.67 | 10.70 | 1.21 | 1.65 | | 6° |

## 8.Ordering information




yy: Year Code
ww: Week Code

| Order Code | Package | Base QTY | Delivery Mode |
|---|---|---|---|
| UMW IRFR1018ETR | TO-252 | 2500 | Tape and reel |

## 9.Disclaimer

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