

## 1. Description

The UMW IR2110STR is a high voltage, high speed power MOSFET drivers with dependent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 600V.

## 3. Features

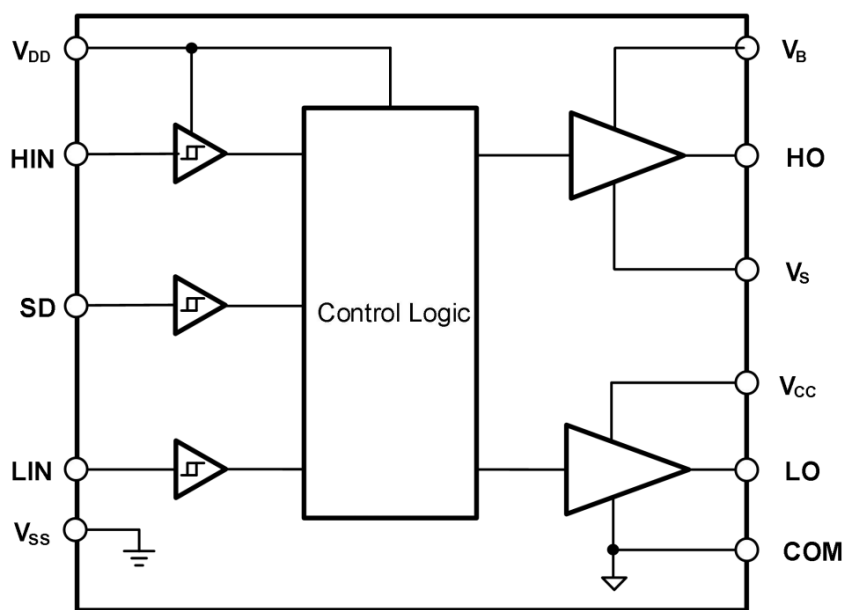
- Floating channel designed for bootstrap operation
- Fully operational to +600V
- 3.3V, 5V and 15V input logic compatible
- Tolerant to negative transient voltage dV/dt immune
- Allowable negative  $V_s$  capability: -9V
- Gate drive supply range from 10V to 20V
- Separate logic supply range from 3.3V to 20V  
Logic and power ground  $\pm 5V$  offset

## 2. Application

- UPS Universal inverter
- Half-bridge and full-bridge converters in AC and DC power supplies
- High-density switching power supplies for servers, telecommunications, IT and industrial infrastructure
- Solar inverter and motor driver
- Undervoltage lockout for both channels
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Wide operating temperature range  
-40°C ~125°C
- Typically output Source/Sink current capability: 4A/4A

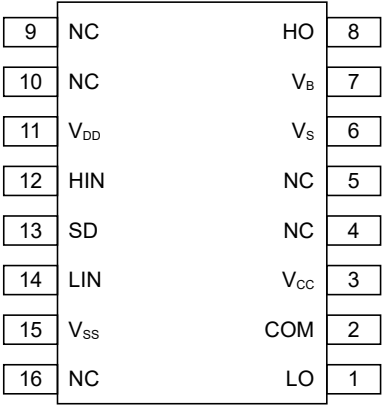


#### 4.Functional Block Diagram





5.Pinning Information



SOP-16-300mil

Table6-1 Lead Definitions

Number	Symbol	Description
1	LO	Low side gate drive output
2	COM	Low side return
3	VCC	Low side supply
6	VS	High side floating supply return
7	VB	High side floating supply
8	HO	High side gate drive output
11	VDD	Logic supply
12	HIN	Logic input for high side gate driver output (HO), in phase
13	SD	Logic input for shutdown
14	LIN	Logic input for low side gate driver output (LO), in phase
15	VSS	Logic ground



## 6. Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to  $V_{SS}$  and an ambient temperature of 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	$V_B$	-0.3	625	V
High side floating supply return	$V_S$	$V_B-25$	$V_B+0.3$	V
High side gate drive output	$V_{HO}$	$V_S-0.3$	$V_B+0.3$	V
Low side and main power supply	$V_{CC}$	-0.3	25	V
Low side gate drive output	$V_{LO}$	-0.3	$V_{CC}+0.3$	V
Logic supply	$V_{DD}$	-0.3	$V_{SS}+25$	V
Logic ground	$V_{SS}$	$V_{CC}-25$	$V_{SS}+0.3$	V
Logic input of HIN & LIN	$V_{IN}$	-0.3	$V_{CC}+0.3$	V
Allowable Offset Supply Voltage Transient	$dV_S/dt$		50	V/ns
HBM Model	ESD	1500		V
Machine Model		500		V
Package Power Dissipation @ $T_A \leq 25^\circ\text{C}$	$P_D$		625	mW
Thermal Resistance., Junction to Ambient	$R_{thJA}$		200	W/°C
Junction Temperature	$T_J$		150	°C
Storage Temperature	$T_S$	-55	150	°C
Lead Temperature (Soldering, 10 seconds)	$T_L$		300	°C



## 7. Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of  $V_S$  and  $V_{SS}$  are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to  $V_{SS}$  and the ambient temperature is 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	$V_B$	$V_S+10$	$V_S+20$	V
High side floating supply return	$V_S$	-9	600	V
High side gate drive output	$V_{HO}$	$V_S$	$V_B$	V
Low side and main power supply	$V_{CC}$	10	20	V
Low side gate drive output	$V_{LO}$	0	VCC	V
Logic supply	$V_{DD}$	$V_{SS}+3$	$V_{SS}+20$	V
Logic ground	$V_{SS}$	-5	5	V
Logic input of HIN & LIN	$V_{IN}$	0	VCC	V
Ambient temperature	$T_A$	-40	125	°C

Note1: Transient negative  $V_S$  can be used for  $V_{SS}-50V$  with a pulse width of 50ns, guaranteed by design.

Note2: When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .



## 8. Electrical Characteristic

Valid for temperature range at  $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=V_{CC}=V_B=15\text{V}$ ,  $C_L=1\text{nF}$ , unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Turn-on propagation delay	$t_{ON}$	$V_S=0\text{V}$		130	200	ns
Turn-off propagation delay	$t_{OFF}$	$V_S=700\text{V}$		130	200	ns
Shutdown propagation delay	$t_{sd}$	$V_S=700\text{V}$		130	200	ns
Turn-on rise time	$t_R$			25	35	ns
Turn-off fall time	$t_F$			17	25	ns
Matched propagation time delay	MT				10	ns
$V_{CC}$ supply UVLO threshold	$V_{CCUV+}$		8	8.9	9.8	V
	$V_{CCUV-}$		7.4	8.2	9	V
hysteresis of $V_{CC}$ UVLO	$V_{CCUVHYS}$			0.7		V
$V_{BS}$ supply UVLO threshold	$V_{BSUV+}$		8	8.9	9.8	V
	$V_{BSUV-}$		7.4	8.2	9	V
hysteresis of $V_{BS}$ UVLO	$V_{BSUVHYS}$			0.7		V
High-side floating supply leakage current	$I_{LK}$	$V_B=V_S=700\text{V}$			50	$\mu\text{A}$
Quiescent VB supply current	$I_{QBS}$	$V_{IN}=0\text{V}$ or $V_{DD}$		70	120	$\mu\text{A}$
Quiescent $V_{CC}$ supply current	$I_{QCC}$	$V_{IN}=0\text{V}$ or $V_{DD}$		120	240	$\mu\text{A}$
Quiescent VDD supply current	$I_{QDD}$	$V_{IN}=0\text{V}$ or $V_{DD}$		15	30	$\mu\text{A}$
Logic "1"(HIN&LIN) input voltage	$V_{IH}$	$V_{CC}=10\text{V}$ to $20\text{V}$	9.5			V
Logic "0"(HIN&LIN) input voltage	$V_{IL}$	$V_{CC}=10\text{V}$ to $20\text{V}$			6	V
High level output voltage, VBIAS -VO	$V_{OH}$	$I_O=0\text{A}$			1.4	V
Low level output voltage, VO	$V_{OL}$	$I_O=0\text{A}$			0.1	V
Logic "1" Input bias current	$I_{IN+}$	$V_{IN}=V_{DD}$		20	40	$\mu\text{A}$
Logic "0" input bias current	$I_{IN-}$	$V_{IN}=0\text{V}$			2	$\mu\text{A}$
Output high short circuit pulsed current	$I_{O+}$	$V_O=0\text{V}$ , $V_{IN}=V_{DD}$ , $PW\leq 10\mu\text{s}$	3	4		A
Output low short circuit pulsed current	$I_{O-}$	$V_O=15\text{V}$ , $V_{IN}=V_{DD}$ , $PW\leq 10\mu\text{s}$	3	4		A



## 9.Function Description

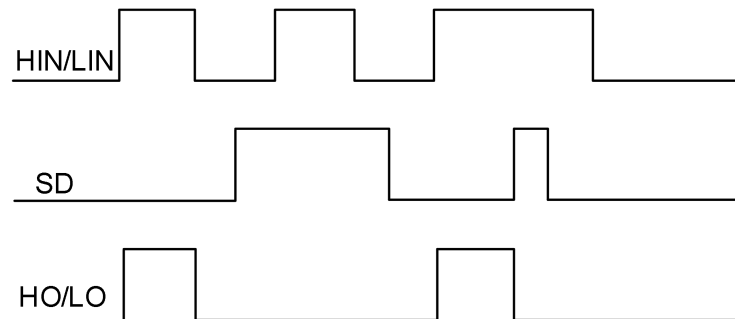


Figure 8-1 IR2110STR Input and output timing waveform

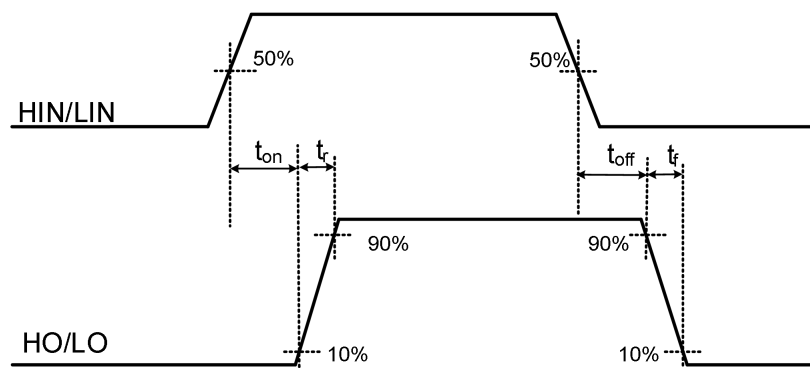


Figure 8-2 Propagation Time Waveform Definition

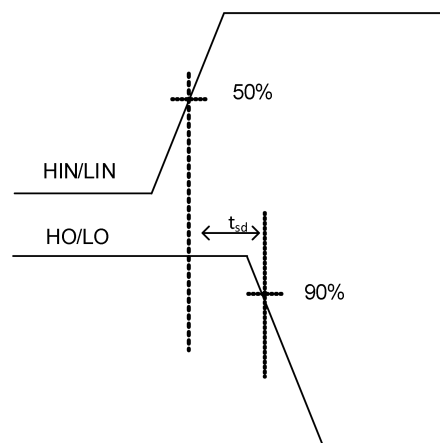


Figure 8-3 Shutdown Propagation Time Waveform Definition

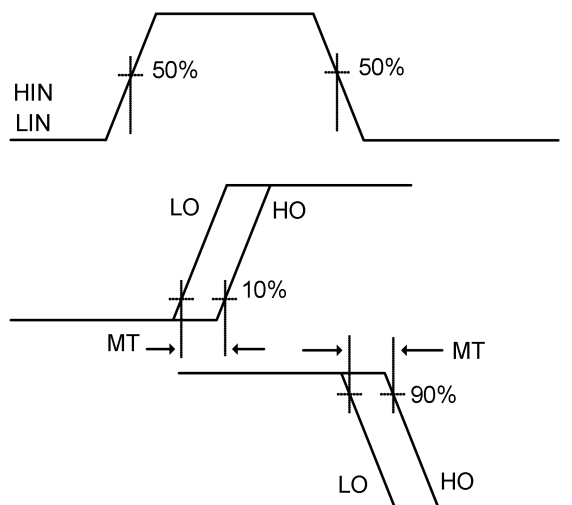


Figure 8-4 Matched propagation time delay Waveform Definition

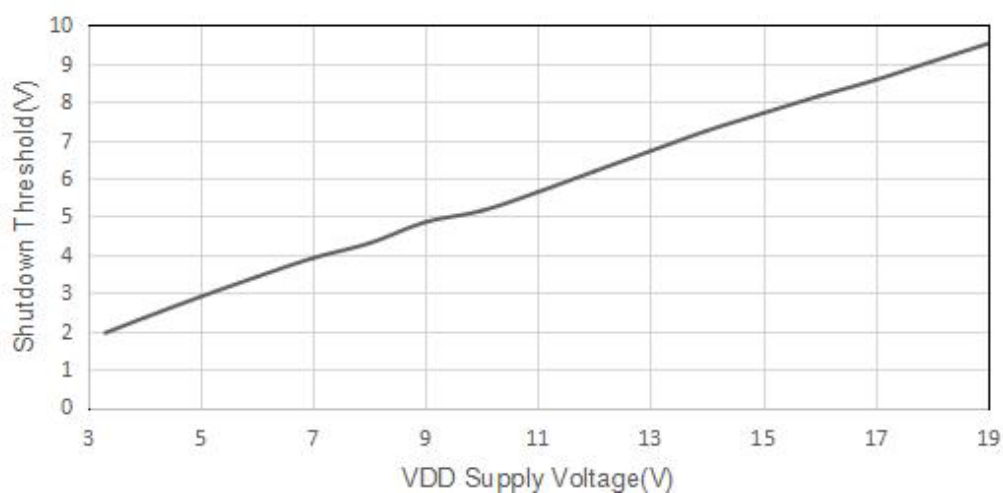


Figure 8-5 Mapping between input threshold voltage and VDD voltage (Typical)



## 10.Function Block Diagram

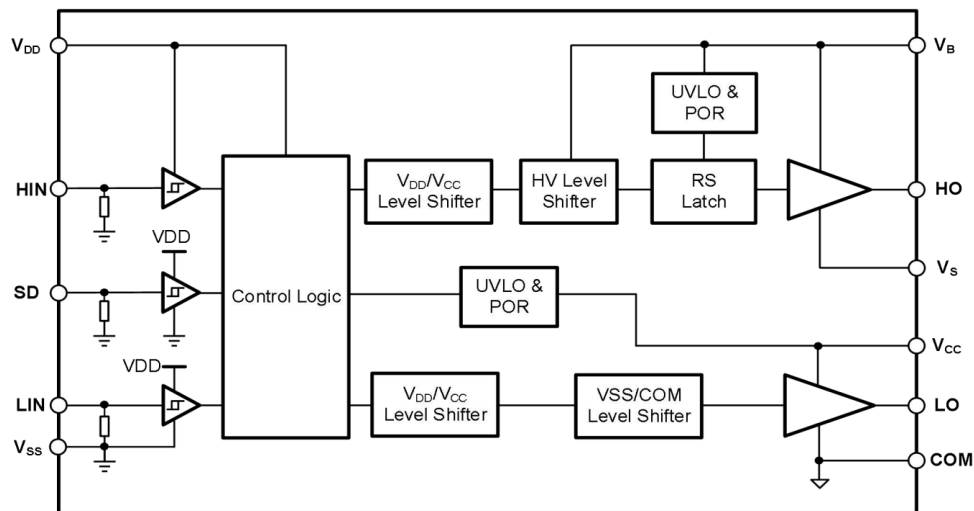


Figure9-1 Function Block Diagram of UMW IR2110STR

## 11.Application message

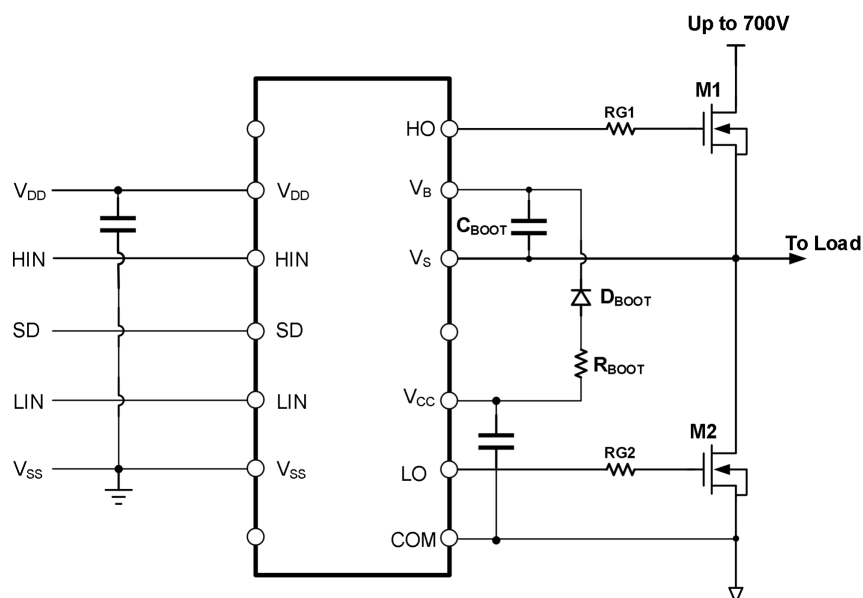
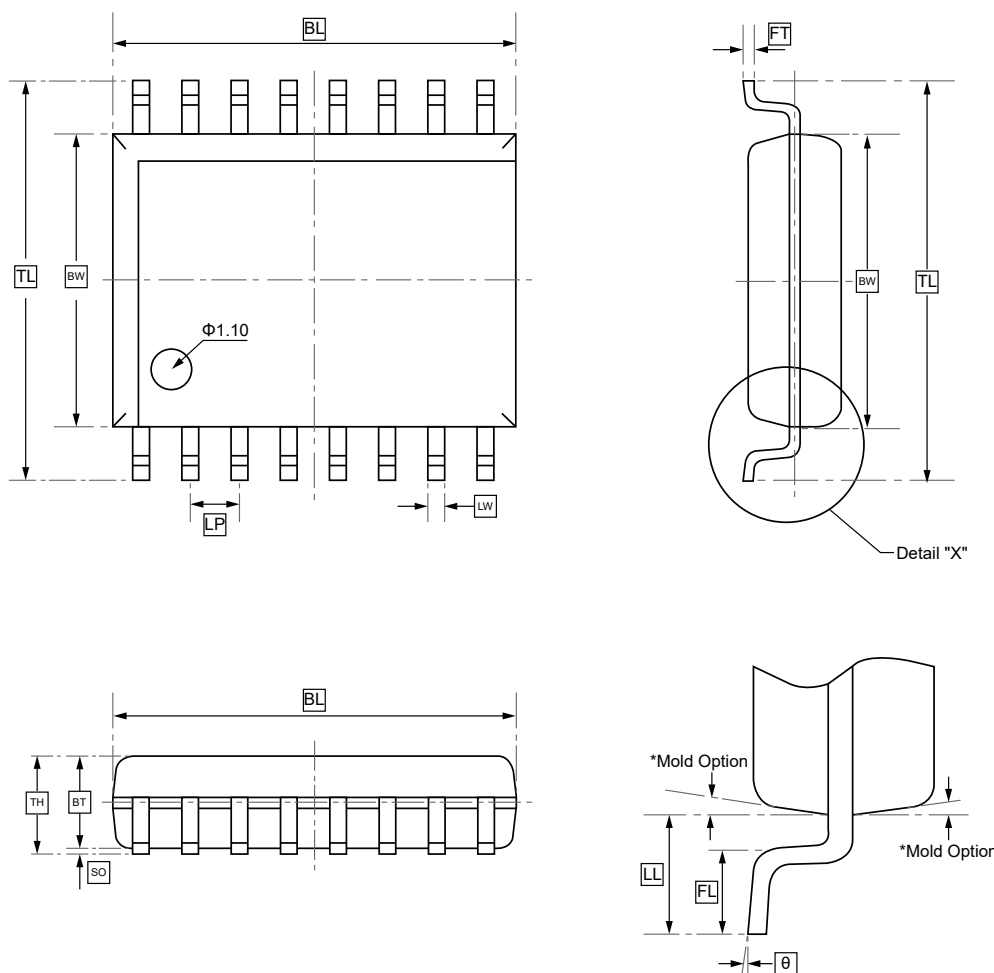


Figure9-2 Typical application circuit of UMW UMW IR2110STR



## 12.SOP-16-300mil Package Outline Dimensions

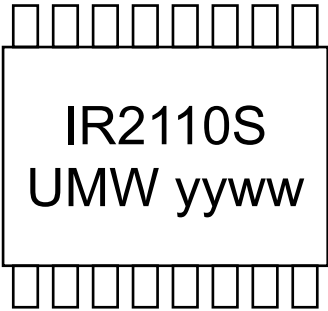


### DIMENSIONS (mm are the original dimensions)

Symbol	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
Min	10.20	7.30	10.10	0.400	1.270	0.170	2.24	0.100	2.590	1.30	0.60	0°
Max	10.45	7.70	10.50	TYP	TYP	0.300	2.44	0.250	Max.	1.50	1.00	8°



13.Ordering information



yy: Year Code  
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IR2110STR	SOP-16-300mil	2500	Tape and reel



## **14.Disclaimer**

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