

1.Description

This P-Channel Logic Level MOSFET is produced using FairchildSemiconductor advancedPower Trenchprocess that hasbeen especiallytailored to minimizethe on-state resistance and yet maintain low gatecharge for superior switchingperformance.

2.Features

- $V_{DS(V)} = -20V$
- $I_D = -2A$
- $R_{DS(ON)} < 70m\Omega (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 110m\Omega (V_{GS} = -2.5V)$
- $R_{DS(ON)} < 210m\Omega (V_{GS} = -1.8V)$

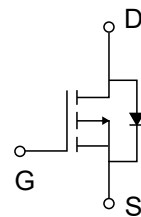
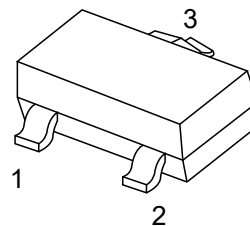
3.Application

- Battery protection
- Load switch
- Battery management

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23



5.Maximum ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current	I_D	-2	A
Pulsed Drain Current	I_{DM}	-10	A
Power Dissipation	P_D	1.1	W
Thermal Resistance from Junction to Ambient ($t \leq 10s$)	$R_{\theta JA}$	250	$^\circ C/W$
Operating Junction	T_J	150	$^\circ C$
Storage Temperature	T_{STG}	-55~+150	$^\circ C$



6. Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4		-1.5	V
Gate-source leakage	I_{GSS}	$V_{GS}=\pm 8V, V_{DS}=0V$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V$			-1	μA
Drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-2A$		52	70	m Ω
		$V_{GS}=-2.5V, I_D=-1.7A$		78	110	m Ω
		$V_{GS}=-1.8V, I_D=-1.2A$			210	m Ω
Forward transconductance	g_{FS}	$V_{DS}=-4.5V, I_D=-2A$		8		S
Diode forward voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$		600		pF
Output Capacitance	C_{oss}			175		pF
Reverse Transfer Capacitance	C_{rss}			80		pF
Total gate charge	Q_g	$V_{DS}=-10V, V_{GS}=-4.5V$ $I_D=-2A$		8		nC
Gate-source charge	Q_{gs}			1.3		nC
Gate-drain charge	Q_{gd}			2.2		nC
Gate resistance	R_g	$f=1MHz$	0.5		3.2	Ω
Switchingbtr						
Turn-on delay time	$t_{D(on)}$	$V_{DS}=-10V, R_L=3.5\Omega, I_D\approx -1A$ $V_{GEN}=-4.5V, R_G=3\Omega$		6		ns
Rise time	t_r			9		ns
Turn-off delay time	$t_{D(off)}$			31		ns
Fall time	t_f			26		ns
Drain-source body diode characteristicstr						
Continuous Source-Drain Diode Current	I_S	$T_C=25^{\circ}C$			-1.2	A
Pulsed Diode forward Current	I_{SM}				-10	A



Note :

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t < 10$ sec.
3. Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production testing.



7.1Typical Characteristics

Figure 1: On-Region Characteristics.	Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.
Figure 3: On-Resistance Variation with Temperature.	Figure 4: On-Resistance Variation with Gate-to-Source Voltage.
Figure 5: Transfer Characteristics.	Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.



7.2 Typical Characteristics

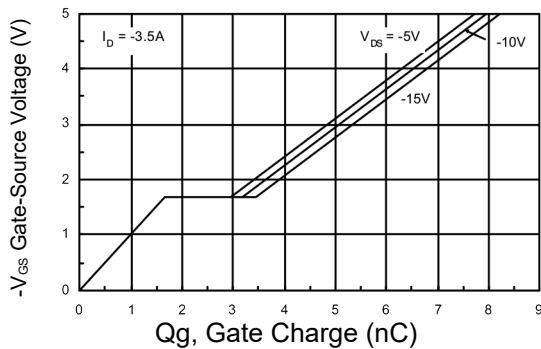


Figure 7: Gate-Charge Characteristics

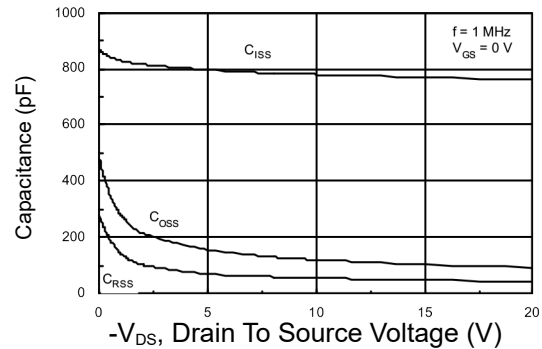


Figure 8: Capacitance Characteristics

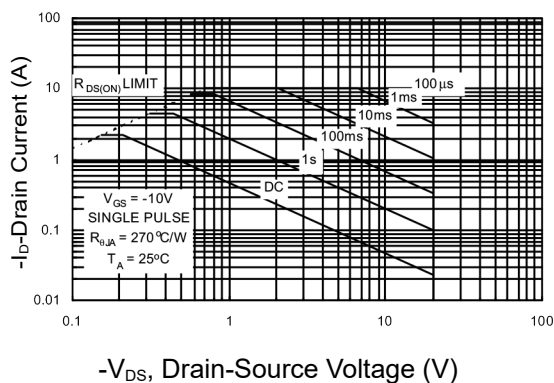


Figure 9: Maximum Safe Operating Area.

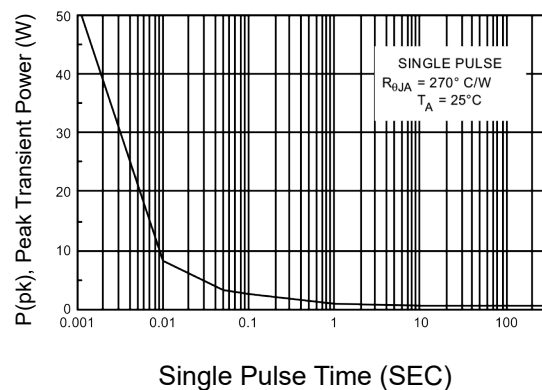


Figure 10: Single Pulse Maximum Power Dissipation.

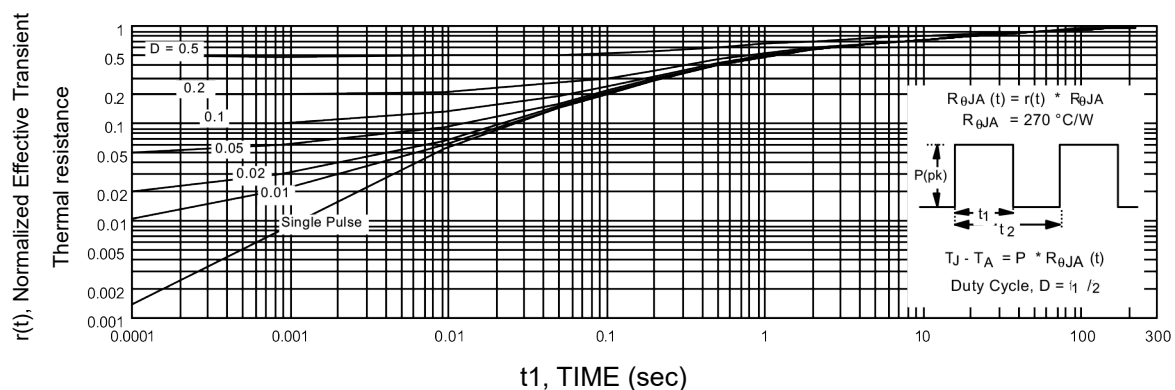
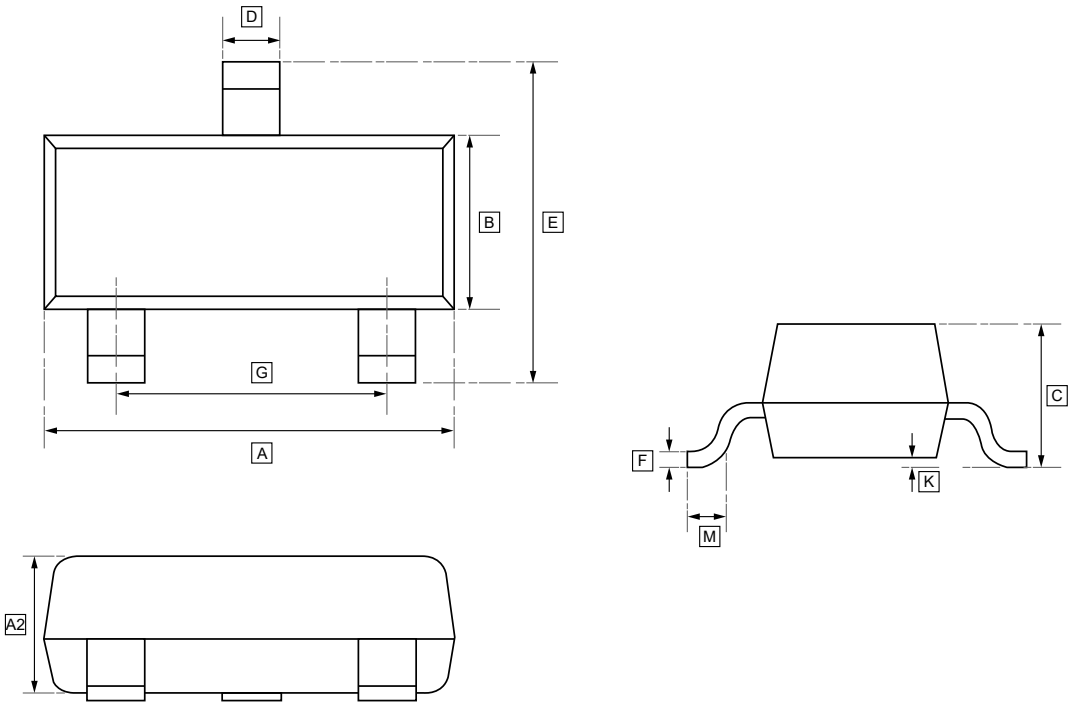


Figure 11: Transient Thermal Response Curve.



8.SOT-23 Package Outline Dimensions

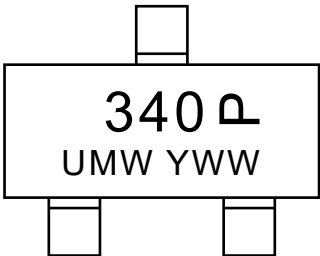


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	D	E	G	K	M	A2	F
Min	2.85	1.20	0.90	0.40	2.25	1.80	0.00	0.30	0.95	0.095
Max	3.04	1.40	1.10	0.50	2.55	2.00	0.10	-	1.05	0.115



9.Ordering information



YWW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDN340P	SOT-23	3000	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.